Project 1

Design Code:

```
module DSP48A1 (A,B,C,D,CARRYIN,BCIN,M,P,CARRYOUT,CARRYOUTF,CLK,OPMODE,CEA,CEB,CEC,CECARRYIN,CED,CEM,CEOPMODE,CEP,RSTA,
input[17:0]A,B,D;
input[7:0]OPMODE;
input[17:0]BCIN;
input[47:0]C,PCIN;
input CARRYIN,CLK,CEA,CEB,CEC,CECARRYIN,CED,CEM,CEOPMODE,CEP,RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTOPMODE,RSTP;
output[47:0]PCOUT,P;
output[17:0]BCOUT;
output[35:0]M;
output CARRYOUT,CARRYOUTF;

parameter A0REG=1 ,A1REG=1 ,B0REG=1 ,B1REG=1;
parameter CREG=1, DREG=1, MREG=1, PREG=1, CARRYINREG=1, CARRYOUTREG=1, OPMODEREG=1;
parameter CARRYINSEL="OPMODE5";
parameter B_INPUT="DIRECT";
parameter RSTTYPE="SYNC";

wire CIN,cout;
reg CINbegin;
wire[7:0]out_OPMODEmux;
wire[35:0]out_multiplier;
wire [17:0]out_Dmux,out_Bmux,out_Amux,out_adder1,out_adder_mux,multiplierin1_mux,out_Amux2;
wire [47:0]out_Cmux,X,Z,out_adder2;
//stage 1
reg_mux_8 m0(OPMODE,CLK,CEOPMODE,RSTOPMODE,out_OPMODEmux);
reg_mux_18 m1(D,CLK,CED,RSTD,out_Dmux);

generate
if(B_INPUT=="DIRECT")
reg_mux_18 m2(B,CLK,CEB,RSTB,out_Bmux);
else if(B_INPUT=="CASCADE")
reg_mux_18 m3(BCIN,CLK,CEB,RSTB,out_Bmux);
else
assign out_Bmux=0;
endgenerate
```

```
36
37  reg_mux_18 m4(A,CLK,CEA,RSTA,out_Amux);
38  reg_mux_48 m5(C,CLK,CEC,RSTC,out_Cmux);
39
40  //stage 2
41  Pre_Adder_Subtracter n1(out_Dmux,out_Bmux,out_OPMODEmux[6],out_adder1);
42  mux_2in n2(out_Bmux,out_adder1,out_OPMODEmux[4],out_adder_mux);
43
44  //stage 3
45  reg_mux_18 r1(out_adder_mux,CLK,CEA,RSTA,multiplierin1_mux);
46  reg_mux_18 r2(out_Amux,CLK,CEA,RSTA,out_Amux2);
47  multiplier r3(multiplierin1_mux,out_Amux2,out_multiplier);
48  assign BCOUT=multiplierin1_mux;
49
50  //stage 4
51  reg_mux_36 e1(out_multiplier,CLK,CEM,RSTM,M);
52  always@(*)begin
53  if(CARRYINSEL=="OPMODE5")
54  CINbegin=out_OPMODEmux[5];
55  else
56  CINbegin=CARRYIN;
57  end
58  reg_mux_1 e2(CINbegin,CLK,CECARRYIN,RSTCARRYIN,CIN);
59
60  //stage 5
61  mux_4in s1(48'h000000000000,{12'h0000,M},P,{D[11:0],A[17:0],B[17:0]},out_OPMODEmux[1:0],X);
62  mux_4in s2(48'h000000000000,PCIN,P,out_Cmux,out_OPMODEmux[3:2],Z);
63
64  //stage 6
65  Post_Adder_Subtracter_48 z1(Z,X,CIN,out_OPMODEmux[7],cout,out_adder2);
66  reg_mux_1 z2(cout,CLK,CECARRYIN,RSTCARRYIN,CARRYOUT);
67  assign CARRYOUTF=CARRYOUT;
68  reg_mux_48 z3(out_adder2,CLK,CEP,RSTP,P);
69  assign PCOUT=P;
70
71  endmodule
```

```
1  module Pre_Adder_Subtracter(in1,in2,opmode,out);
2  input [17:0]in1,in2;
3  input opmode;
4  output [17:0]out;
5
6  assign out =(opmode==1)?(in1-in2):(in1+in2);
7  endmodule
```

```
1   module multiplier(in1,in2,out);
2   input [17:0]in1,in2;
3   output [35:0]out;
4
5   assign out = in1*in2;
6   endmodule
```

```
1   module Post_Adder_Subtracter_48(in1,in2,cin,opmode,cout,out);
2   input [47:0]in1,in2;
3   input cin;
4   input opmode;
5   output [47:0]out;
6   output cout;
7
8   assign {cout,out}=(opmode==1)?(in1-(in2+cin)):(in1+in2+cin);
9   endmodule
```

Note:there are multiple variations of the following modules for each bitwidth instead of using a parameter to make tracing easier

```
module reg_mux_18(in,CLK,CE,RST,out);
input [17:0]in;
input CLK,CE,RST;
output [17:0]out;
reg [17:0]REG_out;
parameter REG=1;
parameter RSTTYPE="SYNC";

assign out =(REG==1)?REG_out:in;

generate
if(RSTTYPE=="SYNC")begin
  always@(posedge CLK)begin
  if(CE==1)begin
    if(RST==1)
    REG_out<=0;
    else
    REG_out<=in;
 end
 end
end
else begin
always@(posedge CLK or posedge RST)begin
    if(RST==1)
    REG_out<=0;
    else begin
     if(CE==1)
     REG_out<=in;
    end
end
end
endgenerate
endmodule
```

```
module mux_4in(in1,in2,in3,in4,opmode,out);
input[47:0]in1,in2,in3,in4;
input[1:0]opmode;
output reg [47:0]out;

always@(*)begin
 case(opmode)
 2'b00:out=in1;
 2'b01:out=in2;
 2'b10:out=in3;
 2'b11:out=in4;
 endcase
end
endmodule
```

Testbench code:

```
module DSP48A1_tb ();
reg[17:0]A,B,D;
reg[7:0]OPMODE;
reg[17:0]BCIN;
reg[47:0]C,PCIN;
reg CARRYIN,CLK,CEA,CEB,CEC,CECARRYIN,CED,CEM,CEOPMODE,CEP,RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTOPMODE,RSTP;
wire[47:0]PCOUT,P;
wire[17:0]BCOUT;
wire[35:0]M;
wire CARRYOUT,CARRYOUTF;


initial begin
 CLK=0;
 forever
    #1 CLK=~CLK;
end

DSP48A1 dut(A,B,C,D,CARRYIN,BCIN,M,P,CARRYOUT,CARRYOUTF,CLK,OPMODE,CEA,CEB,CEC,CECARRYIN,CED,CEM,CEOPMODE,CEP,RSTA,RSTB,RSTC,RSTCARR

initial begin
{A,B,D,OPMODE,BCIN,C,PCIN,CARRYIN,CEA,CEB,CEC,CECARRYIN,CED,CEM,CEOPMODE,CEP,RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTOPMODE,RSTP}=0;
@(negedge CLK);
//clk enable effect
{CEA,CEB,CEC,CECARRYIN,CED,CEM,CEOPMODE,CEP}=8'b00000000;
repeat(10)
@(negedge CLK);
```

```
29  //rst effect
30  {CEA,CEB,CEC,CECARRYIN,CED,CEM,CEOPMODE,CEP}=8'b11111111;
31  {RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTOPMODE,RSTP}=8'b11111111;
32  A=$random;
33  B=$random;
34  D=$random;
35  OPMODE=$random;
36  BCIN=$random;
37  C=$random;
38  PCIN=$random;
39  CARRYIN=$random;
40  repeat(10)
41  @(negedge CLK);
42
43  //OPMODE effect
44  {CEA,CEB,CEC,CECARRYIN,CED,CEM,CEOPMODE,CEP}=8'b11111111;
45  {RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTOPMODE,RSTP}=8'b00000000;
46  //value examples
47  A=24;
48  B=35;
49  D=56;
50  BCIN=1;
51  C=1463;
52  PCIN=1238;
53  CARRYIN=1;
54  OPMODE=8'b11111101;
55  //P=Z(C)-(X((B-D)*A)+CIN)
56  repeat(10)
57  @(negedge CLK);
58
59  OPMODE=8'b01111111;
60  //P=Z(C)+(X(concatenation result)+CIN)
61  repeat(10)
62  @(negedge CLK);
63
```

```
@(negedge CLK);

OPMODE=8'b01001101;
//P=Z(C)+(X(B*A)+CIN(0))
repeat(10)
@(negedge CLK);

//testing carryout
OPMODE=8'b00111110;
C=48'hffffffffffff;
//P=Z(C)+(X((B+D)*A)+CIN(1))
repeat(10)
@(negedge CLK);

$stop;
end
endmodule
```

Do file:

project1.do - Notepad

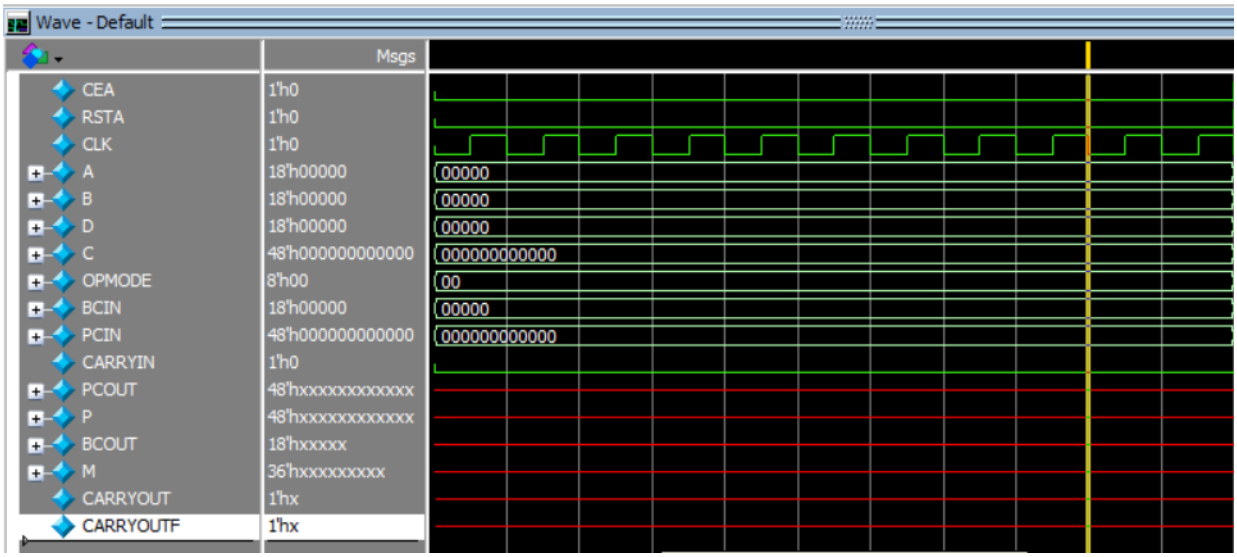
File Edit Format View Help

```
vlog DSPR.v DSPR_tb.v
vsim -voptargs=+acc DSP48A1_tb
add wave -position insertpoint\
sim:/DSP48A1_tb/A\
sim:/DSP48A1_tb/B\
sim:/DSP48A1_tb/D\
sim:/DSP48A1_tb/OPMODE\
sim:/DSP48A1_tb/BCIN\
sim:/DSP48A1_tb/C\
sim:/DSP48A1_tb/PCIN\
sim:/DSP48A1_tb/CARRYIN\
sim:/DSP48A1_tb/CLK\
sim:/DSP48A1_tb/CEA\
sim:/DSP48A1_tb/RSTA\
sim:/DSP48A1_tb/PCOUT\
sim:/DSP48A1_tb/P\
sim:/DSP48A1_tb/BCOUT\
sim:/DSP48A1_tb/M\
sim:/DSP48A1_tb/CARRYOUT\
sim:/DSP48A1_tb/CARRYOUTF
run -all
#quit -sim
```

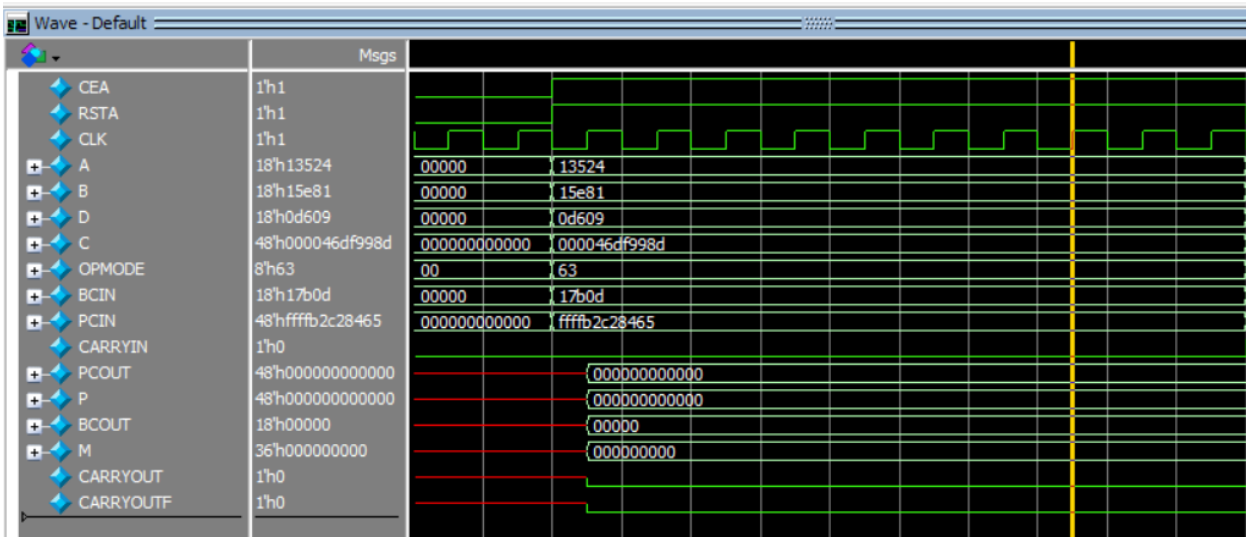
simulation:

note:I have shown only CEA and RSTA as all other CE and RST signals have the same value to make tracing easier

CE=0 for all signals



CE=1 and RST=1 for all signals

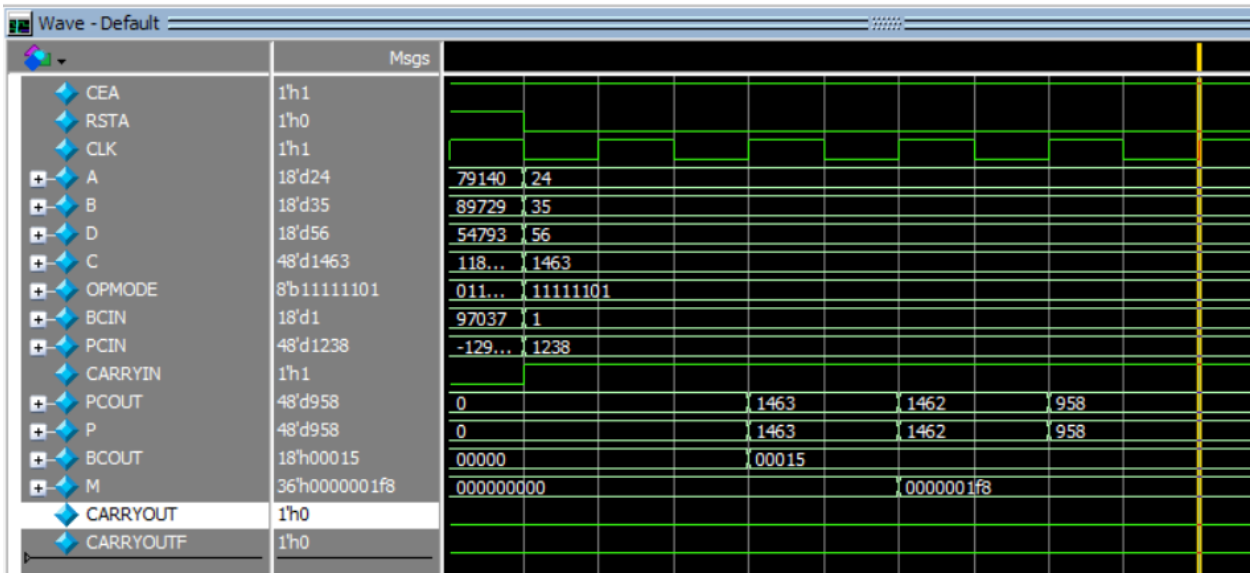


CE=1 and RST=0 for all signals

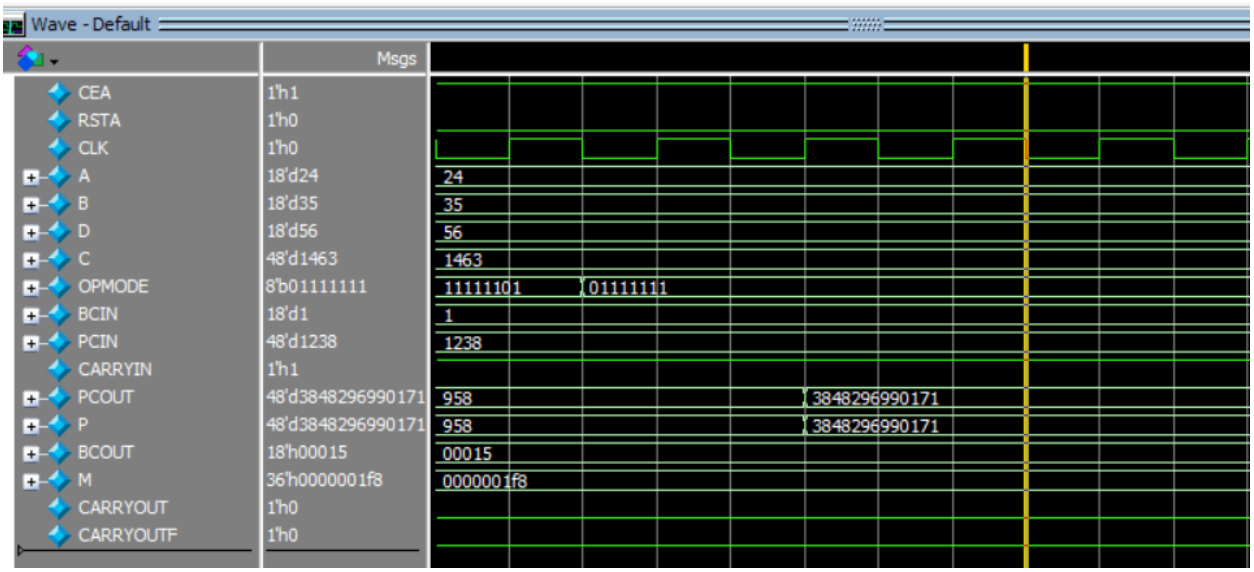
A=24;B=35;D=56;BCIN=1;C=1463;PCIN=1238;CARRYIN=1;

OPMODE=8'b11111101;

//P=Z(C)-(X((B-D)*A)+CIN) ,note:correct output after 4 clk cycles equal to the number of flipflops

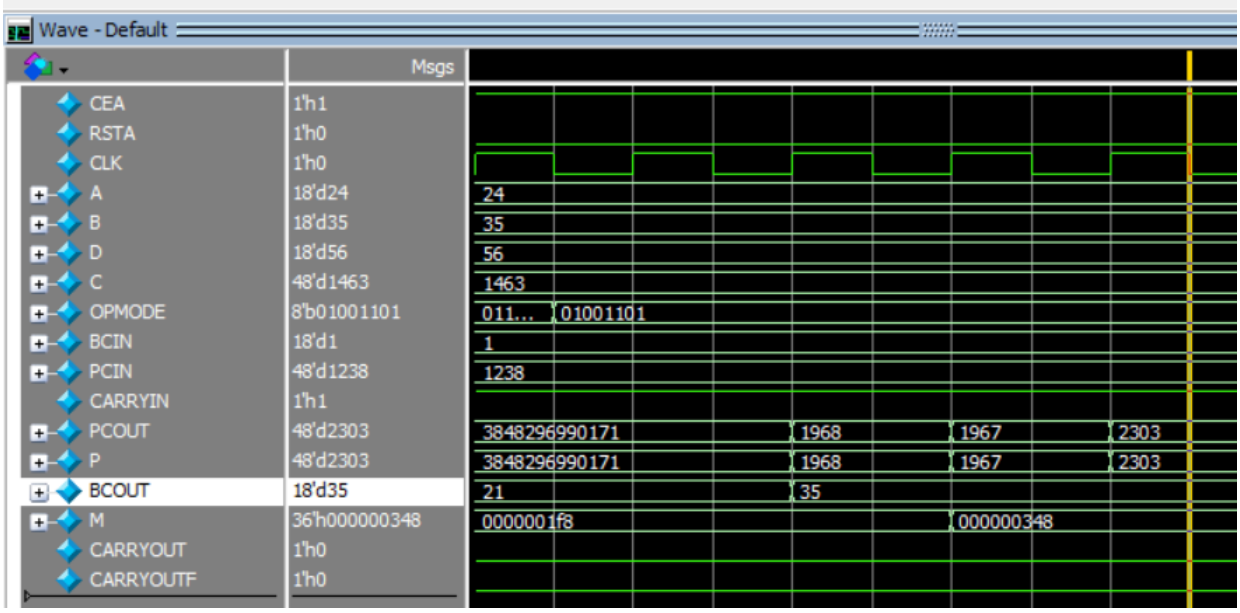


OPMODE=8'b01111111; //P=Z(C)+(X(concatenation result)+CIN)



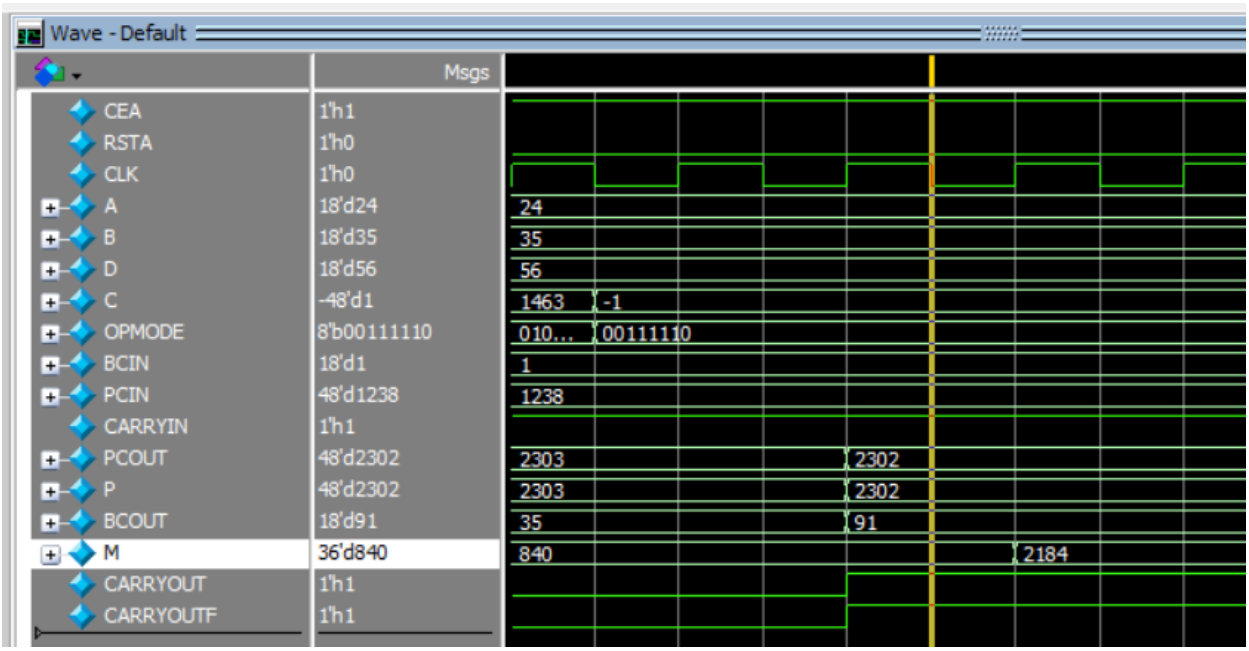
OPMODE=8'b01001101;

//P=Z(C)+(X(B*A)+CIN(0))



OPMODE=8'b00111110;C=48'hffffffffffff;

//P=Z(C)+(X((B+D)*A)+CIN(1))



Vivadoo:

Constraints file:

```
## Clock signal
set_property -dict {PACKAGE_PIN W5 IOSTANDARD LVCMOS33} [get_ports CLK]
create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add [get_ports CLK]
```

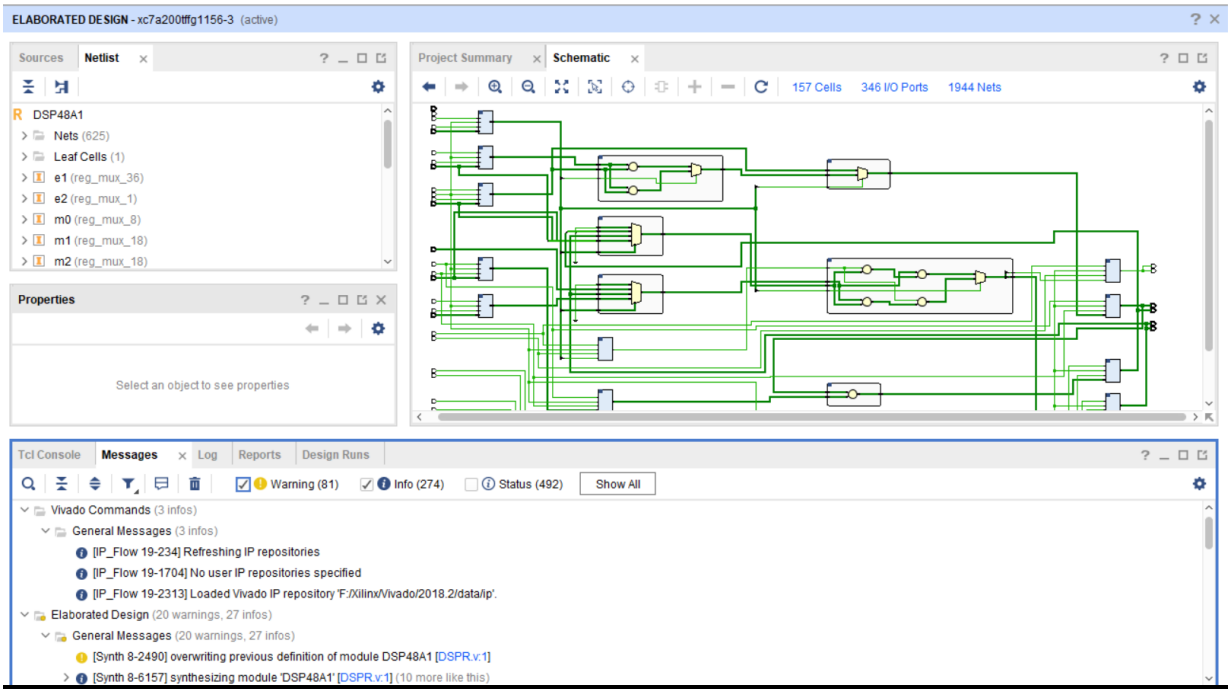
```
151
152  ## Configuration options, can be used for all designs
153  set_property CONFIG_VOLTAGE 3.3 [current_design]
154  set_property CFGBVS VCCO [current_design]
155
156  ## SPI configuration mode options for QSPI boot, can be used for all designs
157  set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
158  set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
159  set_property CONFIG_MODE SPIx4 [current_design]
160
161  create_debug_core u_ila_0 ila
162  set_property ALL_PROBE_SAME_MU true [get_debug_cores u_ila_0]
163  set_property ALL_PROBE_SAME_MU_CNT 1 [get_debug_cores u_ila_0]
164  set_property C_ADV_TRIGGER false [get_debug_cores u_ila_0]
165  set_property C_DATA_DEPTH 1024 [get_debug_cores u_ila_0]
166  set_property C_EN_STRG_QUAL false [get_debug_cores u_ila_0]
167  set_property C_INPUT_PIPE_STAGES 0 [get_debug_cores u_ila_0]
168  set_property C_TRIGIN_EN false [get_debug_cores u_ila_0]
169  set_property C_TRIGOUT_EN false [get_debug_cores u_ila_0]
170  set_property port_width 1 [get_debug_ports u_ila_0/clk]
171  connect_debug_port u_ila_0/clk [get_nets [list CLK_IBUF_BUFG]]
172  set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe0]
173  set_property port_width 18 [get_debug_ports u_ila_0/probe0]
174  connect_debug_port u_ila_0/probe0 [get_nets [list {BCOUT_OBUF[0]} {BCOUT_OBUF[1]} {BCOUT_OBUF[2]} {BCOUT_OBUF[3]} {BCOUT_
175  create_debug_port u_ila_0 probe
176  set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe1]
177  set_property port_width 48 [get_debug_ports u_ila_0/probe1]
178  connect_debug_port u_ila_0/probe1 [get_nets [list {C_IBUF[0]} {C_IBUF[1]} {C_IBUF[2]} {C_IBUF[3]} {C_IBUF[4]} {C_IBUF[5]}
179  create_debug_port u_ila_0 probe
180  set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe2]
181  set_property port_width 18 [get_debug_ports u_ila_0/probe2]
182  connect_debug_port u_ila_0/probe2 [get_nets [list {A_IBUF[0]} {A_IBUF[1]} {A_IBUF[2]} {A_IBUF[3]} {A_IBUF[4]} {A_IBUF[5]}
183  create_debug_port u_ila_0 probe
184  set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe3]
185  set_property port_width 18 [get_debug_ports u_ila_0/probe3]
186  connect_debug_port u_ila_0/probe3 [get_nets [list {B_IBUF[0]} {B_IBUF[1]} {B_IBUF[2]} {B_IBUF[3]} {B_IBUF[4]} {B_IBUF[5]}
187  create_debug_port u_ila_0 probe
```

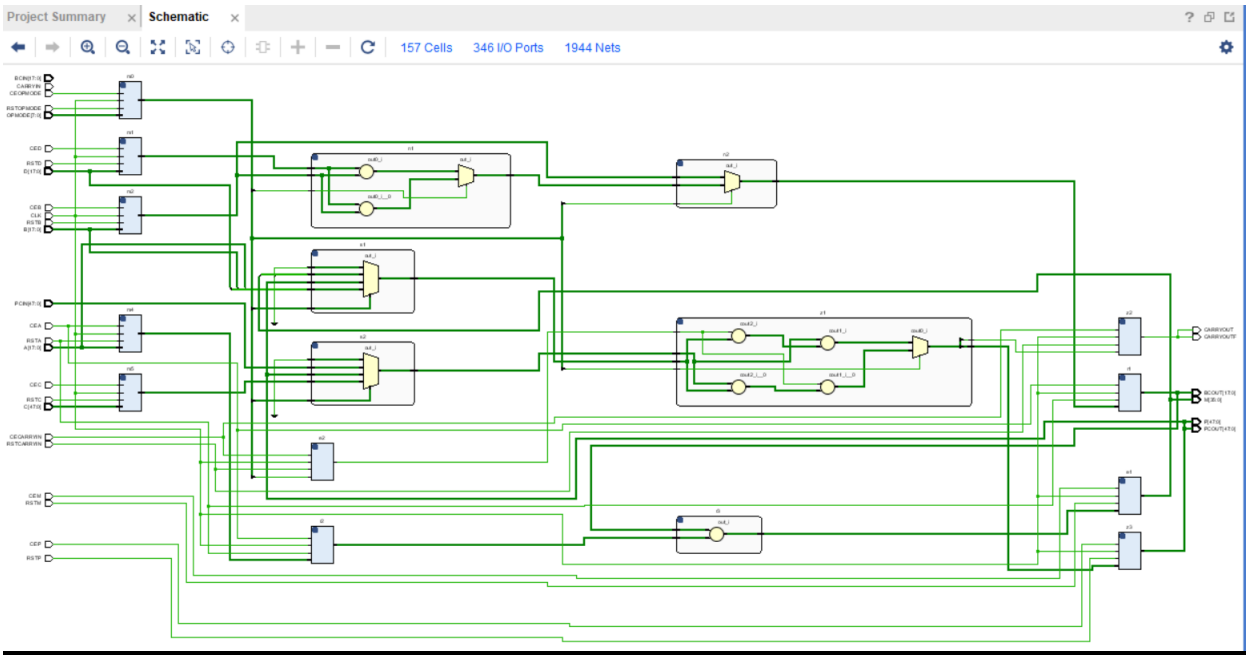
```
connect_debug_port u_ila_0/probe3 [get_nets [list {B_IBUF[0]} {B_IBUF[1]} {B_IBUF[2]} {B_IBUF[3]} {B_IBUF[4]} {B_IBUF[5]} {B_
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe4]
set_property port_width 18 [get_debug_ports u_ila_0/probe4]
connect_debug_port u_ila_0/probe4 [get_nets [list {D_IBUF[0]} {D_IBUF[1]} {D_IBUF[2]} {D_IBUF[3]} {D_IBUF[4]} {D_IBUF[5]} {D_
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe5]
set_property port_width 36 [get_debug_ports u_ila_0/probe5]
connect_debug_port u_ila_0/probe5 [get_nets [list {M_OBUF[0]} {M_OBUF[1]} {M_OBUF[2]} {M_OBUF[3]} {M_OBUF[4]} {M_OBUF[5]} {M_
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe6]
set_property port_width 48 [get_debug_ports u_ila_0/probe6]
connect_debug_port u_ila_0/probe6 [get_nets [list {PCIN_IBUF[0]} {PCIN_IBUF[1]} {PCIN_IBUF[2]} {PCIN_IBUF[3]} {PCIN_IBUF[4]}
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe7]
set_property port_width 8 [get_debug_ports u_ila_0/probe7]
connect_debug_port u_ila_0/probe7 [get_nets [list {OPMODE_IBUF[0]} {OPMODE_IBUF[1]} {OPMODE_IBUF[2]} {OPMODE_IBUF[3]} {OPMODE
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe8]
set_property port_width 48 [get_debug_ports u_ila_0/probe8]
connect_debug_port u_ila_0/probe8 [get_nets [list {PCOUT_OBUF[0]} {PCOUT_OBUF[1]} {PCOUT_OBUF[2]} {PCOUT_OBUF[3]} {PCOUT_OBUF
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe9]
set_property port_width 1 [get_debug_ports u_ila_0/probe9]
connect_debug_port u_ila_0/probe9 [get_nets [list CARRYOUTF_OBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe10]
set_property port_width 1 [get_debug_ports u_ila_0/probe10]
connect_debug_port u_ila_0/probe10 [get_nets [list CEA_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe11]
set_property port_width 1 [get_debug_ports u_ila_0/probe11]
connect_debug_port u_ila_0/probe11 [get_nets [list CEB_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe12]
set_property port_width 1 [get_debug_ports u_ila_0/probe12]
```

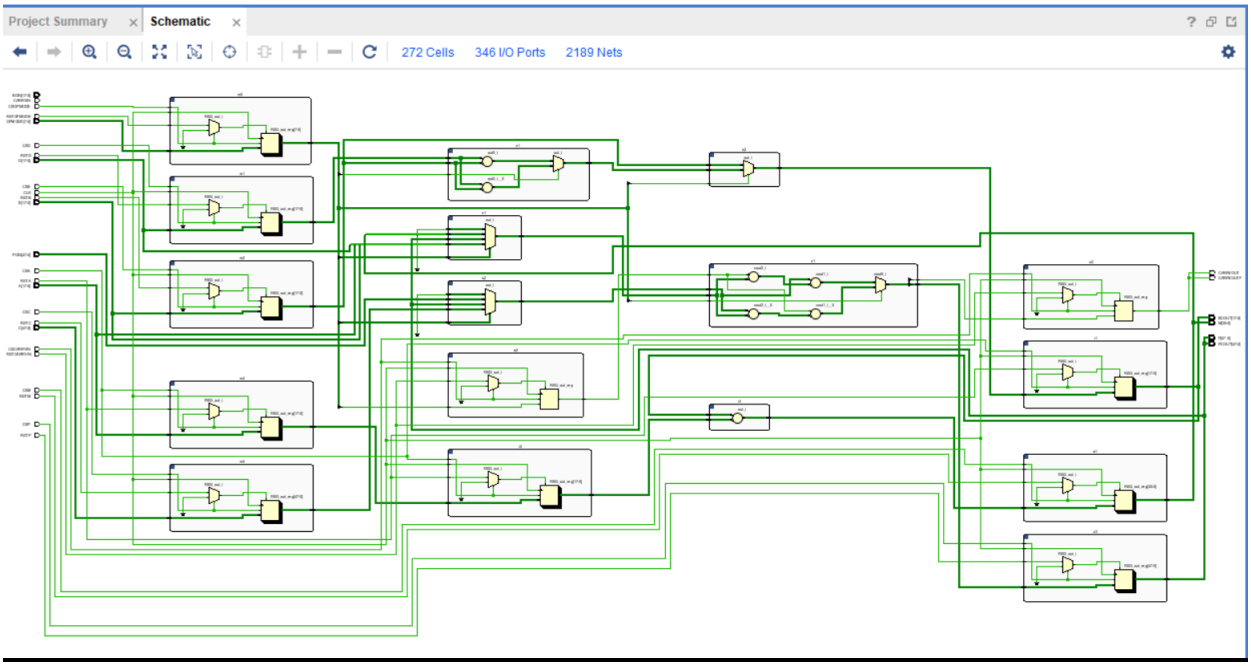
```
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe12]
set_property port_width 1 [get_debug_ports u_ila_0/probe12]
connect_debug_port u_ila_0/probe12 [get_nets [list CEC_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe13]
set_property port_width 1 [get_debug_ports u_ila_0/probe13]
connect_debug_port u_ila_0/probe13 [get_nets [list CECARRYIN_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe14]
set_property port_width 1 [get_debug_ports u_ila_0/probe14]
connect_debug_port u_ila_0/probe14 [get_nets [list CED_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe15]
set_property port_width 1 [get_debug_ports u_ila_0/probe15]
connect_debug_port u_ila_0/probe15 [get_nets [list CEM_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe16]
set_property port_width 1 [get_debug_ports u_ila_0/probe16]
connect_debug_port u_ila_0/probe16 [get_nets [list CEOPMODE_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe17]
set_property port_width 1 [get_debug_ports u_ila_0/probe17]
connect_debug_port u_ila_0/probe17 [get_nets [list CEP_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe18]
set_property port_width 1 [get_debug_ports u_ila_0/probe18]
connect_debug_port u_ila_0/probe18 [get_nets [list CLK_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe19]
set_property port_width 1 [get_debug_ports u_ila_0/probe19]
connect_debug_port u_ila_0/probe19 [get_nets [list RSTA_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe20]
set_property port_width 1 [get_debug_ports u_ila_0/probe20]
connect_debug_port u_ila_0/probe20 [get_nets [list RSTB_IBUF]]
create_debug_port u_ila_0 probe
```

```
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe21]
set_property port_width 1 [get_debug_ports u_ila_0/probe21]
connect_debug_port u_ila_0/probe21 [get_nets [list RSTC_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe22]
set_property port_width 1 [get_debug_ports u_ila_0/probe22]
connect_debug_port u_ila_0/probe22 [get_nets [list RSTCARRYIN_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe23]
set_property port_width 1 [get_debug_ports u_ila_0/probe23]
connect_debug_port u_ila_0/probe23 [get_nets [list RSTD_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe24]
set_property port_width 1 [get_debug_ports u_ila_0/probe24]
connect_debug_port u_ila_0/probe24 [get_nets [list RSTM_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe25]
set_property port_width 1 [get_debug_ports u_ila_0/probe25]
connect_debug_port u_ila_0/probe25 [get_nets [list RSTOPMODE_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe26]
set_property port_width 1 [get_debug_ports u_ila_0/probe26]
connect_debug_port u_ila_0/probe26 [get_nets [list RSTP_IBUF]]
set_property C_CLK_INPUT_FREQ_HZ 300000000 [get_debug_cores dbg_hub]
set_property C_ENABLE_CLK_DIVIDER false [get_debug_cores dbg_hub]
set_property C_USER_SCAN_CHAIN 1 [get_debug_cores dbg_hub]
connect_debug_port dbg_hub/clk [get_nets CLK_IBUF_BUFG]
```

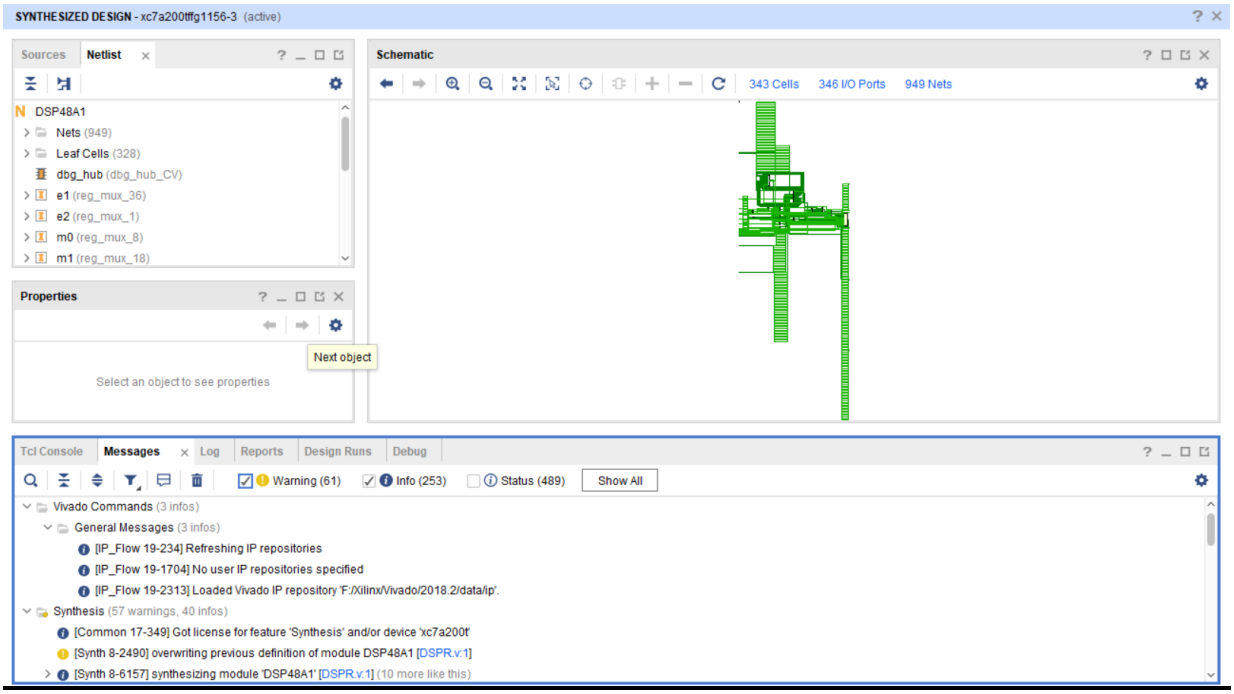
Elaborated design:

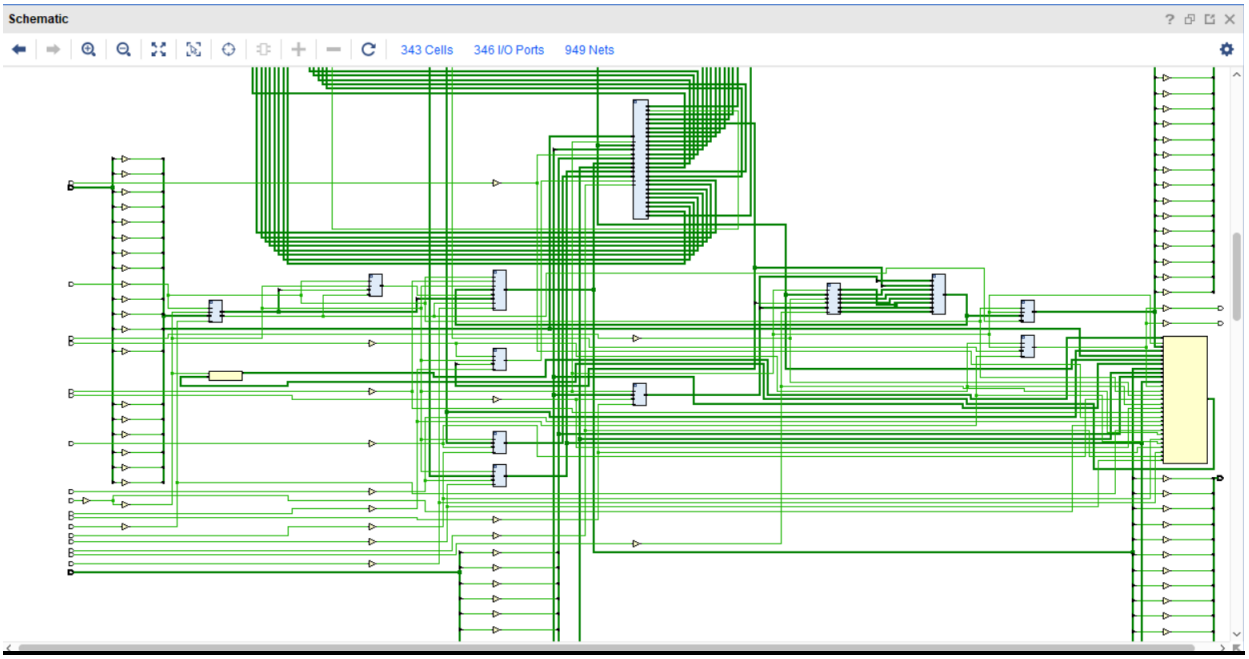

ELABORATED DESIGN - xc7a200tffg1156-3 (active)
Sources
Netlist
DSP48A1
Nets (625)
Leaf Cells (1)
e1 (reg_mux_36)
e2 (reg_mux_1)
m0 (reg_mux_8)
m1 (reg_mux_18)
m2 (reg_mux_18)
Properties
Select an object to see properties
Project Summary
Schematic
157 Cells
346 I/O Ports
1944 Nets
Tcl Console
Messages
Log
Reports
Design Runs
Warning (81)
Info (274)
Status (492)
Show All
Vivado Commands (3 infos)
General Messages (3 infos)
[IP_Flow 19-234] Refreshing IP repositories
[IP_Flow 19-1704] No user IP repositories specified
[IP_Flow 19-2313] Loaded Vivado IP repository 'F:/Xilinx/Vivado/2018.2/data/ip'.
Elaborated Design (20 warnings, 27 infos)
General Messages (20 warnings, 27 infos)
[Synth 8-2490] overwriting previous definition of module DSP48A1 [DSPR.v:1]
[Synth 8-6157] synthesizing module 'DSP48A1' [DSPR.v:1] (10 more like this)


Project Summary
Schematic
157 Cells
346 I/O Ports
1944 Nets


Project Summary
Schematic
272 Cells
346 I/O Ports
2189 Nets

Synthesis:


SYNTHESIZED DESIGN - xc7a200tffg1156-3 (active)
Sources
Netlist
DSP48A1
Nets (949)
Leaf Cells (328)
dbg_hub (dbg_hub_CV)
e1 (reg_mux_36)
e2 (reg_mux_1)
m0 (reg_mux_8)
m1 (reg_mux_18)
Properties
Select an object to see properties
Next object
Schematic
343 Cells
346 I/O Ports
949 Nets
Tcl Console
Messages
Log
Reports
Design Runs
Debug
Warning (61)
Info (253)
Status (489)
Show All
Vivado Commands (3 infos)
General Messages (3 infos)
[IP_Flow 19-234] Refreshing IP repositories
[IP_Flow 19-1704] No user IP repositories specified
[IP_Flow 19-2313] Loaded Vivado IP repository 'F:/Xilinx/Vivado/2018.2/data/ip'.
Synthesis (57 warnings, 40 infos)
[Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
[Synth 8-2490] overwriting previous definition of module DSP48A1 [DSPR.v:1]
[Synth 8-6157] synthesizing module 'DSP48A1' [DSPR.v:1] (10 more like this)

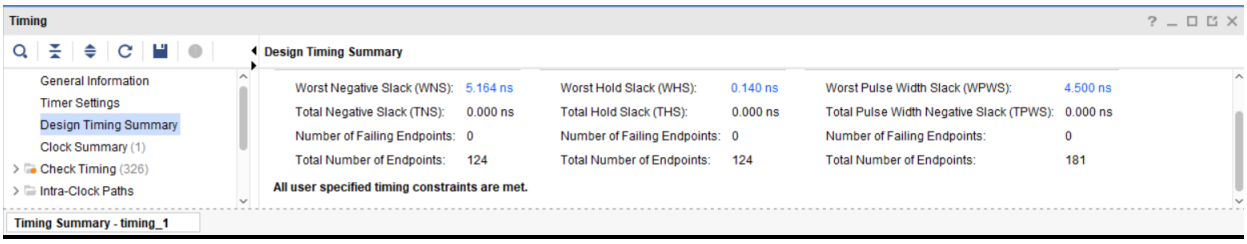


Timing | **Utilization**

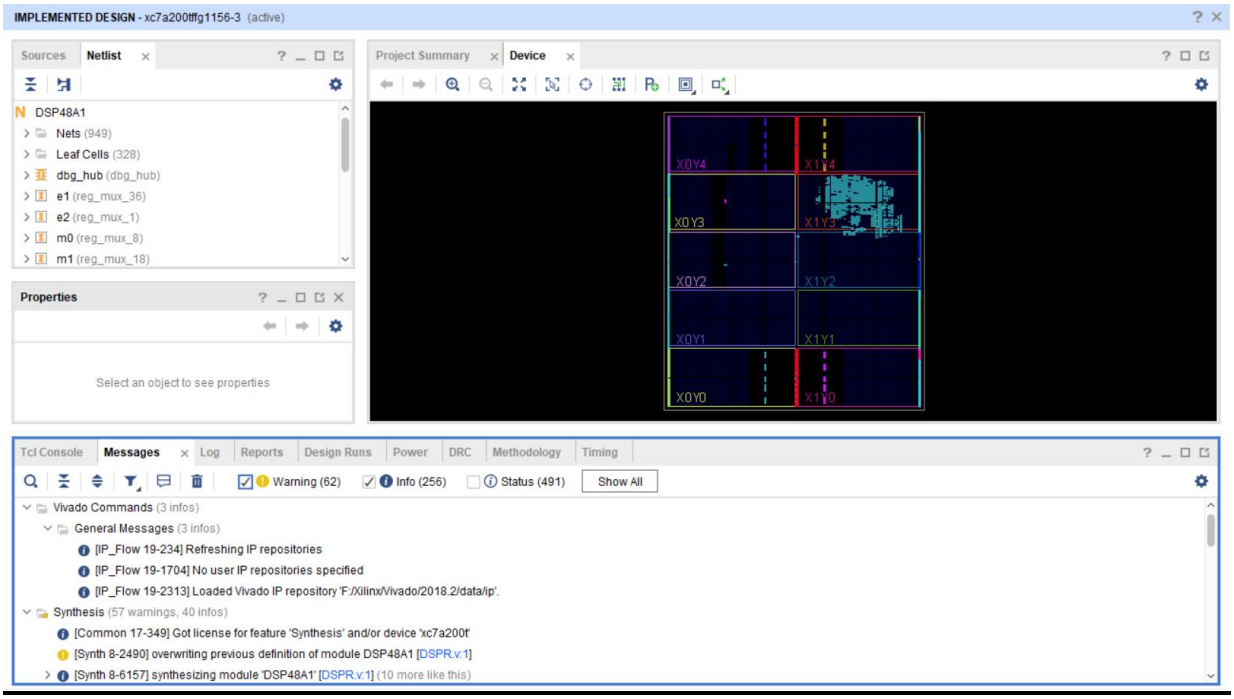
Hierarchy

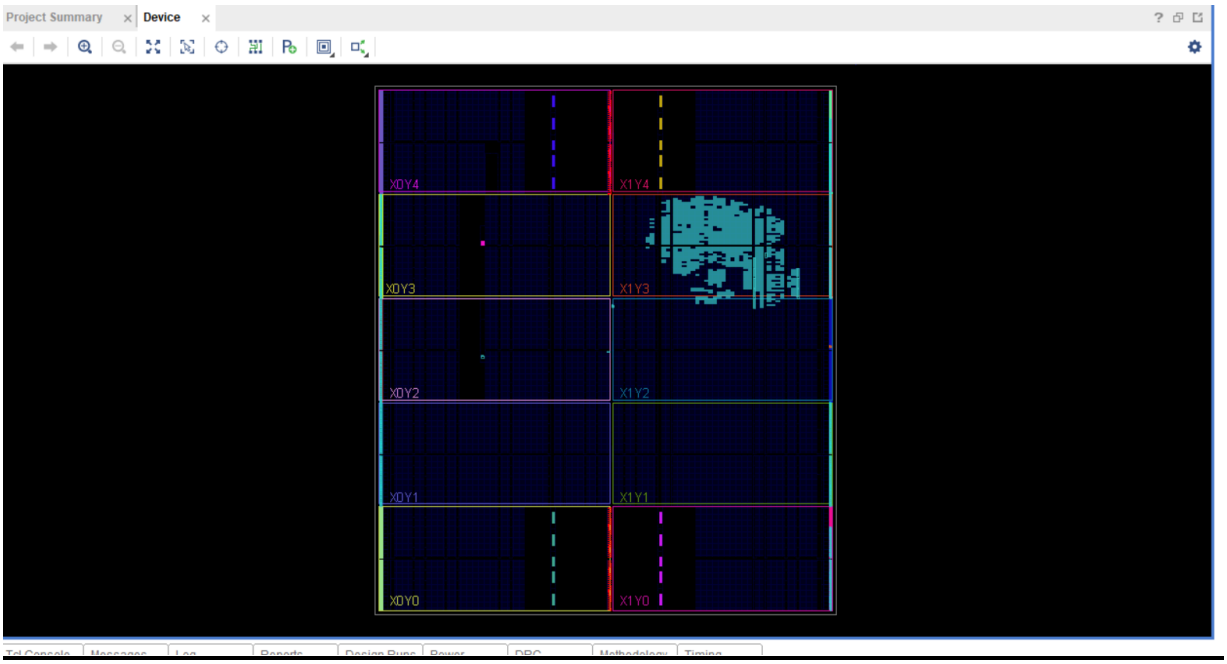
- Hierarchy
- Summary
- Slice Logic
  - Slice LUTs (<1%)
    - LUT as Logic (<1%)
  - Slice Registers (<1%)
    - Register as Flip Flop (<
- Memory
- DSP
  - DSPs (<1%)
    - DSP48E1 only
- IO and GT Specific
  - Bonded IOB (65%)
    - IOB Master Pads
- Clocking
  - BUFGCTRL (3%)
- Specific Feature
- Primitives
- Black Boxes
  - u_ila_0_CV
  - dbg_hub_CV
- Instantiated Netlists

Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
N DSP48A1	238	179	1	327	1
dbg_hub (dbg_hub_CV)	0	0	0	0	0
e1 (reg_mux_36)	1	0	1	0	0
e2 (reg_mux_1)	1	1	0	0	0
m0 (reg_mux_8)	194	8	0	0	0
m1 (reg_mux_18)	1	18	0	0	0
m2 (reg_mux_18_0)	19	18	0	0	0
m4 (reg_mux_18_1)	1	18	0	0	0
m5 (reg_mux_48)	1	48	0	0	0
n2 (mux_2in)	18	0	0	0	0
r1 (reg_mux_18_2)	0	18	0	0	0
r2 (reg_mux_18_3)	0	1	0	0	0
u_ila_0 (u_ila_0_CV)	0	0	0	0	0
z1 (Post_Adder_Subtra...	0	0	0	0	0
z2 (reg_mux_1_4)	1	1	0	0	0
z3 (reg_mux_48_5)	1	48	0	0	0



implementation:





IMPLEMENTED DESIGN - xc7a200tffg1156-3 (active)

Utilization

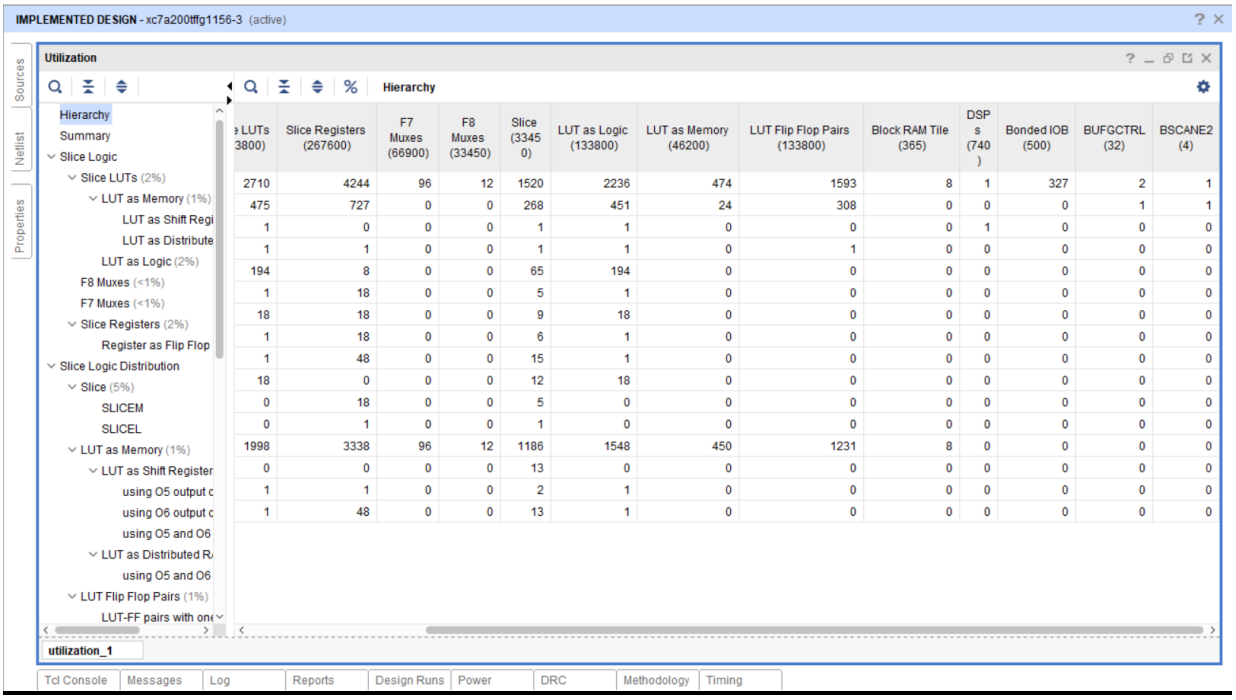
Hierarchy

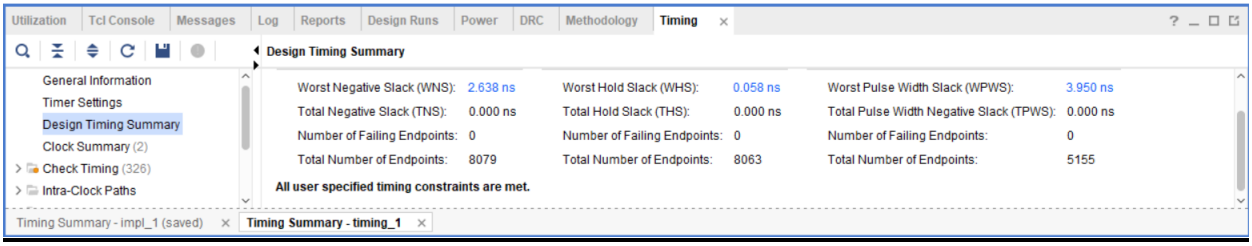
Sources | Netlist | Properties

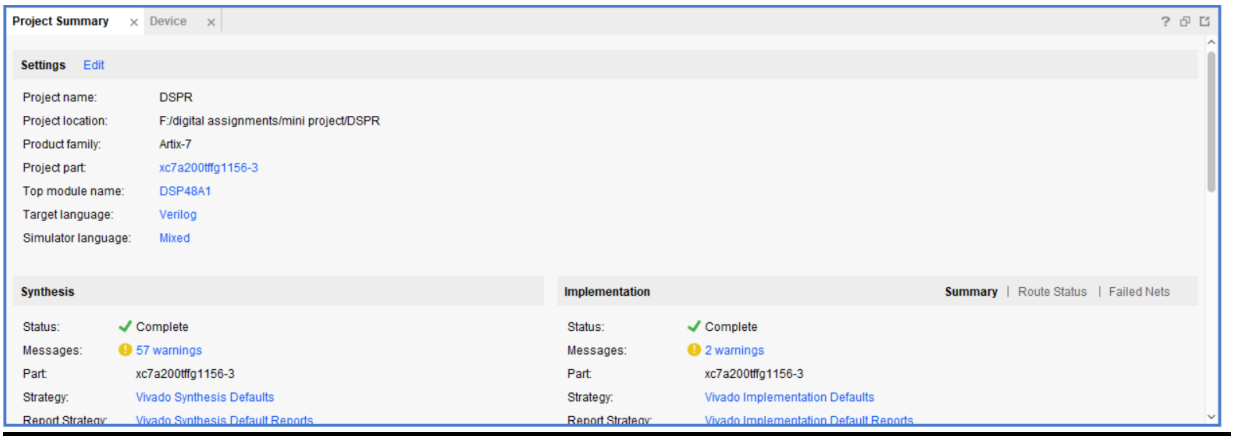
- Hierarchy
- Summary
- Slice Logic
  - Slice LUTs (2%)
    - LUT as Memory (1%)
      - LUT as Shift Regi
      - LUT as Distribute
    - LUT as Logic (2%)
  - F8 Muxes (<1%)
  - F7 Muxes (<1%)
  - Slice Registers (2%)
    - Register as Flip Flop
- Slice Logic Distribution
  - Slice (5%)
    - SLICEM
    - SLICEL
  - LUT as Memory (1%)
    - LUT as Shift Register
      - using O5 output c
      - using O6 output c
      - using O5 and O6
    - LUT as Distributed R
      - using O5 and O6
  - LUT Flip Flop Pairs (1%)
    - LUT-FF pairs with on

Name	Slice LUTs (133800)	Slice Registers (267600)	F7 Muxes (66900)	F8 Muxes (33450)	Slice (33450)	LUT as Logic (133800)	LUT as Memory (46200)	LUT Flip Flop Pairs (133800)	Block RAM Tile (365)	DSPs (740)
DSP48A1	2710	4244	96	12	1520	2236	474	1593	8	1
dbg_hub (dbg_hub)	475	727	0	0	268	451	24	308	0	0
e1 (reg_mux_36)	1	0	0	0	1	1	0	0	0	1
e2 (reg_mux_1)	1	1	0	0	1	1	0	1	0	0
m0 (reg_mux_8)	194	8	0	0	65	194	0	0	0	0
m1 (reg_mux_18)	1	18	0	0	5	1	0	0	0	0
m2 (reg_mux_18_0)	18	18	0	0	9	18	0	0	0	0
m4 (reg_mux_18_1)	1	18	0	0	6	1	0	0	0	0
m5 (reg_mux_48)	1	48	0	0	15	1	0	0	0	0
n2 (mux_2in)	18	0	0	0	12	18	0	0	0	0
r1 (reg_mux_18_2)	0	18	0	0	5	0	0	0	0	0
r2 (reg_mux_18_3)	0	1	0	0	1	0	0	0	0	0
u_ila_0 (u_ila_0)	1998	3338	96	12	1186	1548	450	1231	8	0
z1 (Post_Adder_Subtra...	0	0	0	0	13	0	0	0	0	0
z2 (reg_mux_1_4)	1	1	0	0	2	1	0	0	0	0
z3 (reg_mux_48_5)	1	48	0	0	13	1	0	0	0	0

utilization_1


IMPLEMENTED DESIGN - xc7a200tffg1156-3 (active)
Utilization
Hierarchy
Summary
Slice Logic
Slice LUTs (2%)
LUT as Memory (1%)
LUT as Shift Regi
LUT as Distribute
LUT as Logic (2%)
F8 Muxes (<1%)
F7 Muxes (<1%)
Slice Registers (2%)
Register as Flip Flop
Slice Logic Distribution
Slice (5%)
SLICEM
SLICEL
LUT as Memory (1%)
LUT as Shift Register
using O5 output c
using O6 output c
using O5 and O6
LUT as Distributed R
using O5 and O6
LUT Flip Flop Pairs (1%)
LUT-FF pairs with one
Hierarchy
LUTs (3800)
Slice Registers (267600)
F7 Muxes (66900)
F8 Muxes (33450)
Slice (33450)
LUT as Logic (133800)
LUT as Memory (46200)
LUT Flip Flop Pairs (133800)
Block RAM Tile (365)
DSPs (740)
Bonded IOB (500)
BUFGCTRL (32)
BSCANE2 (4)
2710 4244 96 12 1520 2236 474 1593 8 1 327 2 1
475 727 0 0 268 451 24 308 0 0 0 1 1
1 0 0 0 1 1 0 0 0 1 0 0 0
1 1 0 0 1 1 0 1 0 0 0 0 0
194 8 0 0 65 194 0 0 0 0 0 0 0
1 18 0 0 5 1 0 0 0 0 0 0 0
18 18 0 0 9 18 0 0 0 0 0 0 0
1 18 0 0 6 1 0 0 0 0 0 0 0
1 48 0 0 15 1 0 0 0 0 0 0 0
18 0 0 0 12 18 0 0 0 0 0 0 0
0 18 0 0 5 0 0 0 0 0 0 0 0
0 1 0 0 1 0 0 0 0 0 0 0 0
1998 3338 96 12 1186 1548 450 1231 8 0 0 0 0
0 0 0 0 13 0 0 0 0 0 0 0 0
1 1 0 0 2 1 0 0 0 0 0 0 0
1 48 0 0 13 1 0 0 0 0 0 0 0
utilization_1
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing


Utilization
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Clock Summary (2)
Check Timing (326)
Intra-Clock Paths
Worst Negative Slack (WNS): 2.638 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 8079
Worst Hold Slack (WHS): 0.058 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 8063
Worst Pulse Width Slack (WPWS): 3.950 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 5155
All user specified timing constraints are met.
Timing Summary - impl_1 (saved)
Timing Summary - timing_1


Project Summary
Device
Settings Edit
Project name: DSPR
Project location: F:/digital assignments/mini project/DSPR
Product family: Artix-7
Project part: xc7a200tffg1156-3
Top module name: DSP48A1
Target language: Verilog
Simulator language: Mixed
Synthesis
Status: Complete
Messages: 57 warnings
Part: xc7a200tffg1156-3
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Implementation
Summary | Route Status | Failed Nets
Status: Complete
Messages: 2 warnings
Part: xc7a200tffg1156-3
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports