1 Verilog-A Behavioral Models

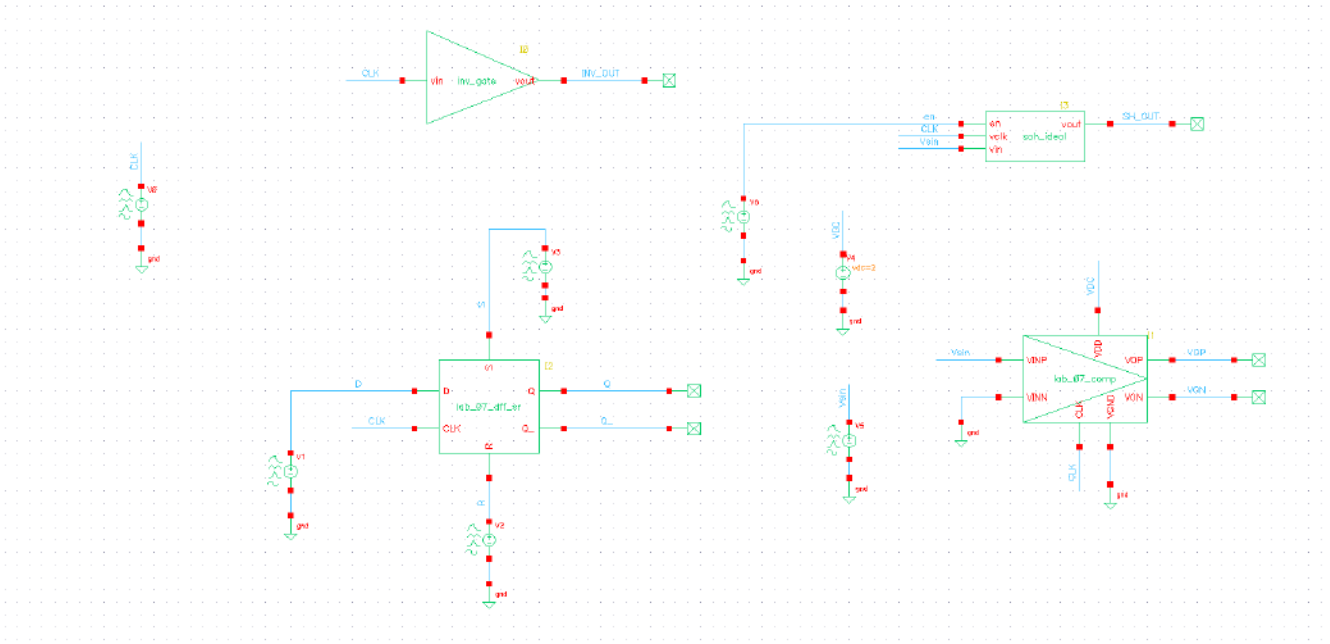

Figure 1: Test circuit schematic

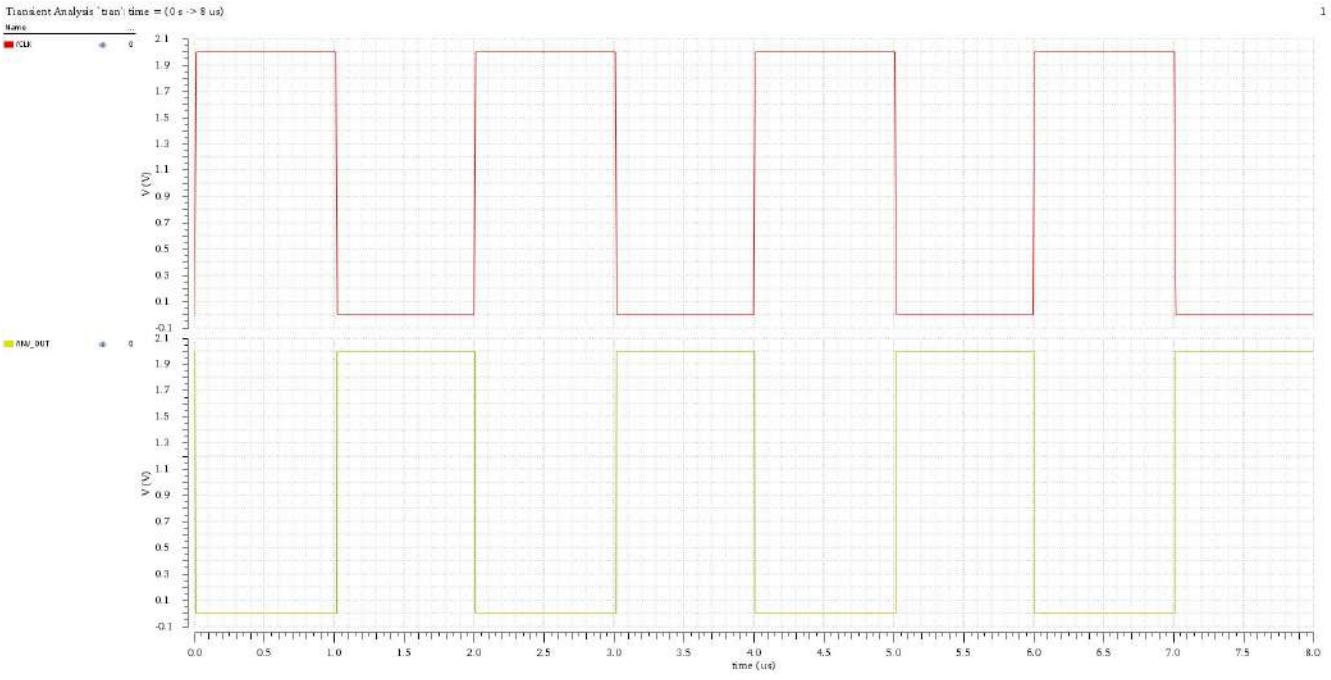

Figure 2: Inverter test-bench

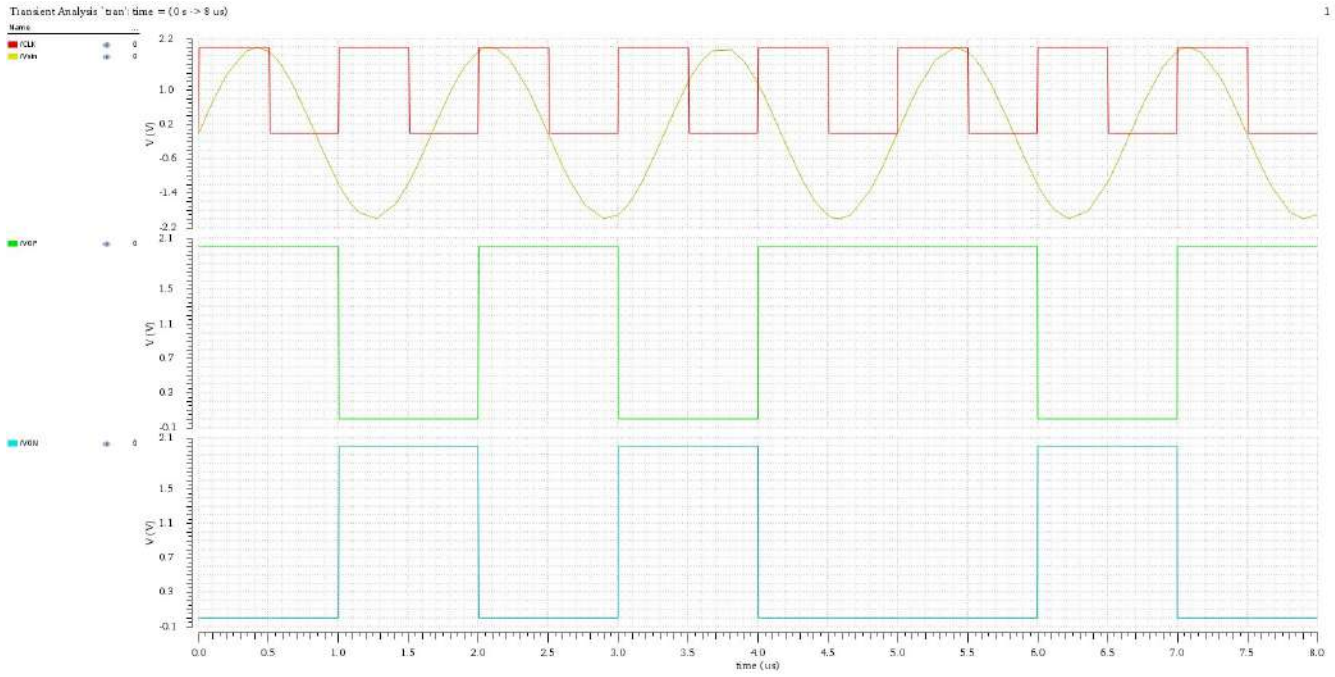

Figure 3: Comparator test-bench

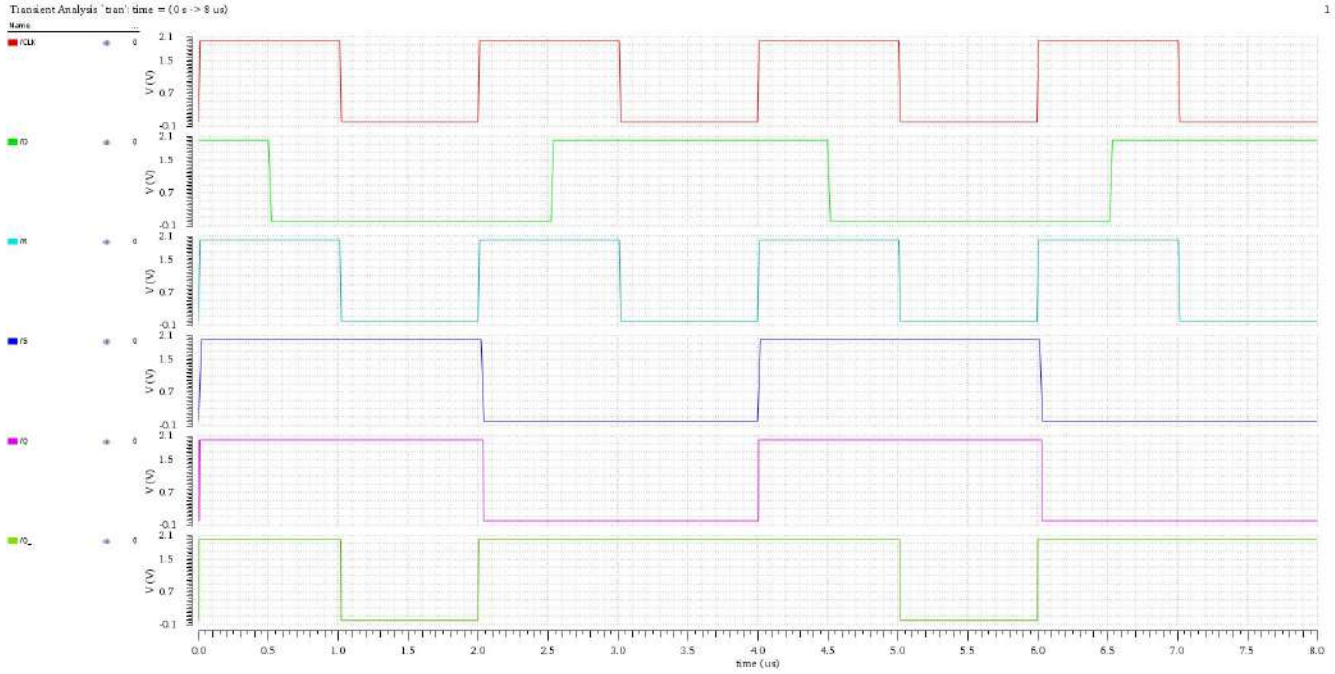

Figure 4: D F/F with S/R test-bench

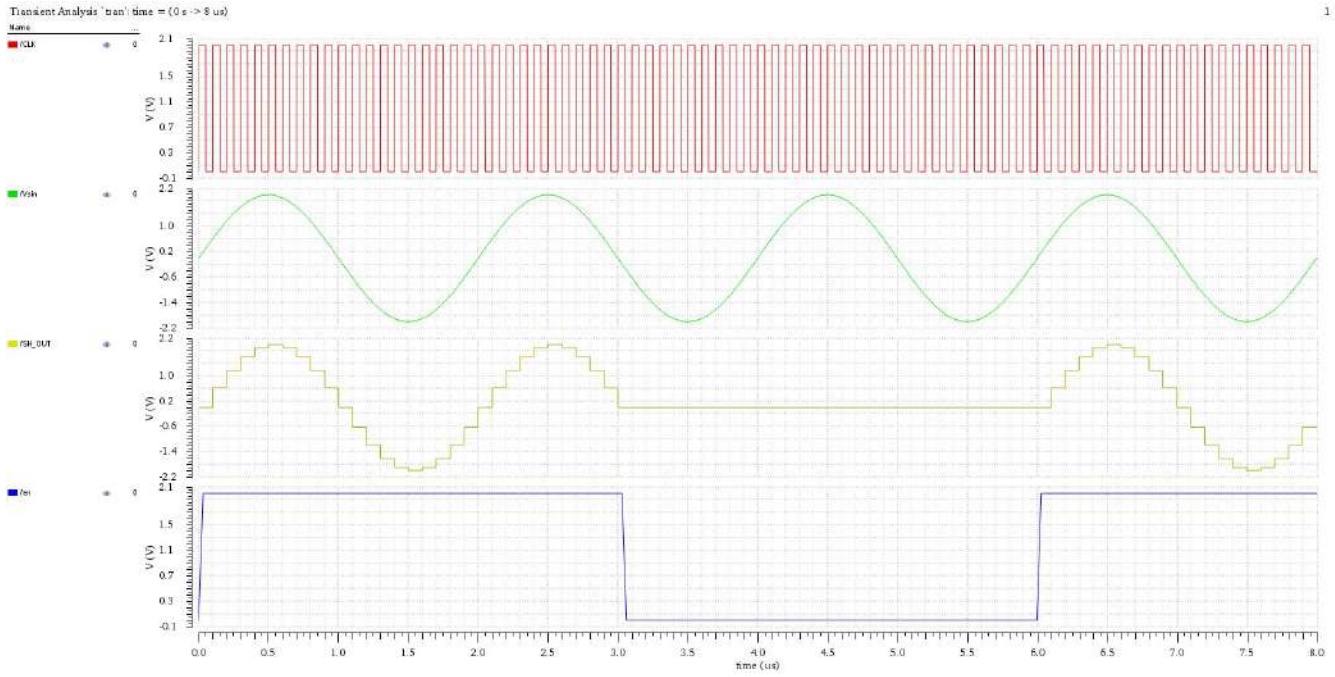

Figure 5: S/H test-bench

- We will carry on with these blocks and use the the NAND and NOR gates of the ahdllib.

2 SAR Logic

2.1 Implementation

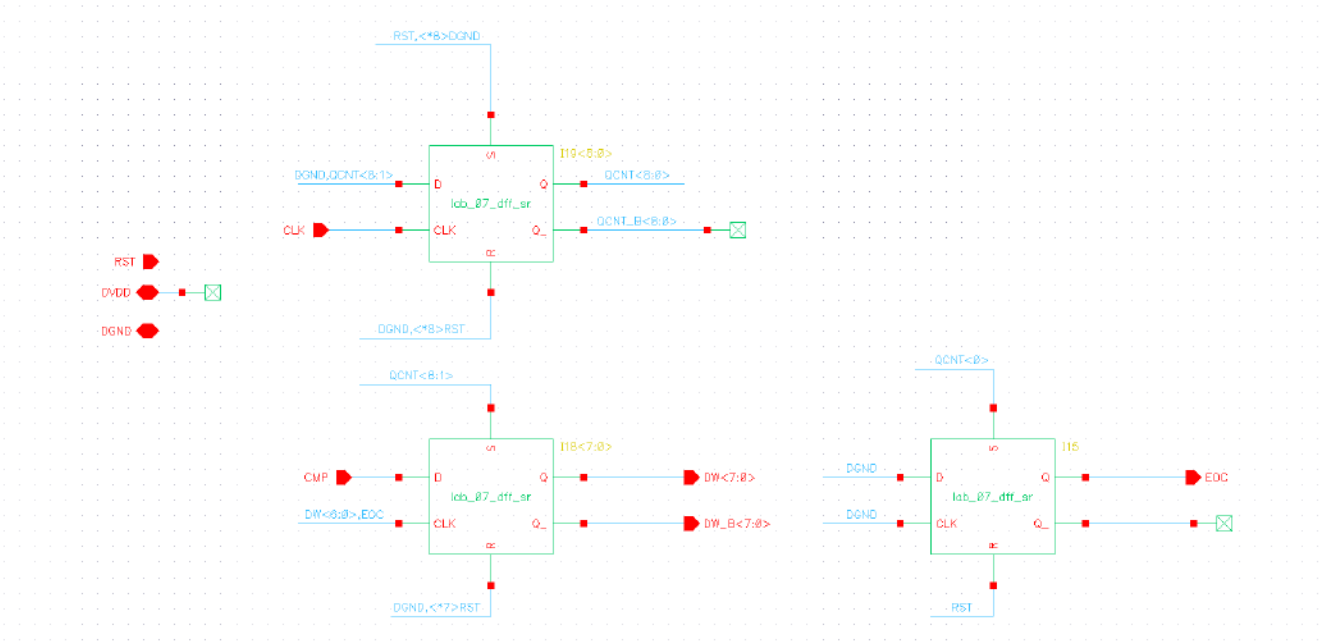

Figure 6: SAR Logic block diagram

- The design of SAR logic consists of two register, one is a code register which outputs the digital code that is being successively approximated each clock cycle. The other is a ring counter which is used to set the code register.
- The RST pin - which will be connected to the sampling clock - is connected to the SET pin for the first F/F in the ring register and to the RESET pin for the rest of the F/Fs. This is done in order to reset all ring register outputs when the sampling clock is high, except for the first F/F. On the next clock cycle, the second F/F will have logical 1 on its D input. So, it will output logical one, while the first F/F output will be reset to zero since its D input is connected to ground. The same applies for all F/Fs in the ring register.
- The SET pin of the code register is connected to the output of the ring register. This is done in order to set the code register F/Fs successively. The register code output is then passed to the capacitive DAC in order to be compared with the sampled signal. On the next cycle, the comparator output will be available at the D input of the F/Fs, it will be captured by connecting CLK input to the Q output of the next F/F. This is done because we need to capture the value once throughout the whole conversion process. so, we can not connect it to the clock.

2.2 Simulation

2.2.1 CMP is all zeros

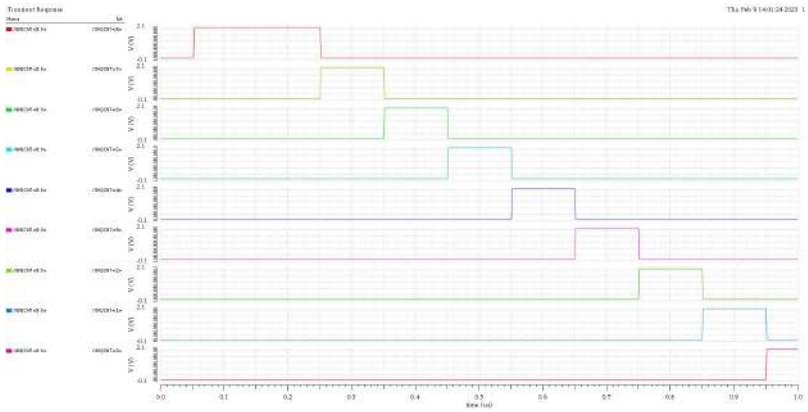

Figure 7: Counter output

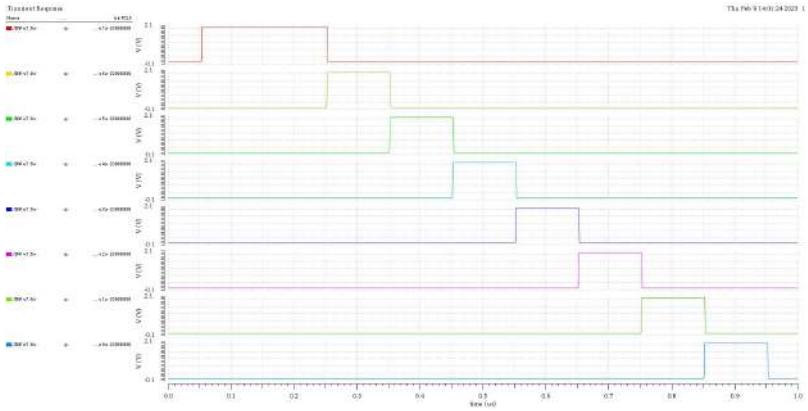

Figure 8: Code register output

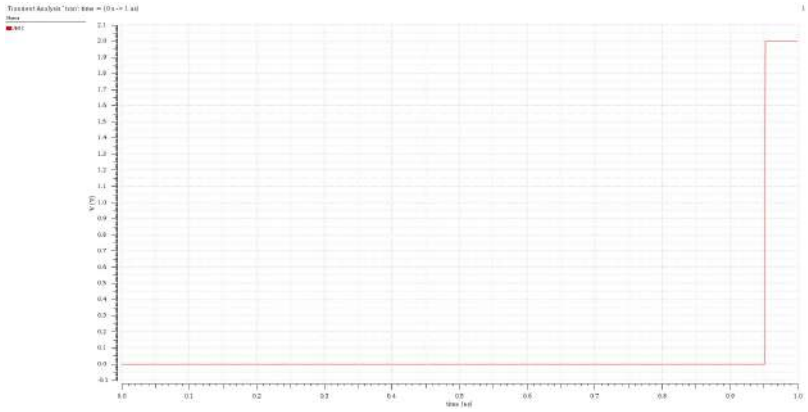

Figure 9: EOC

2.2.2 CMP is all ones

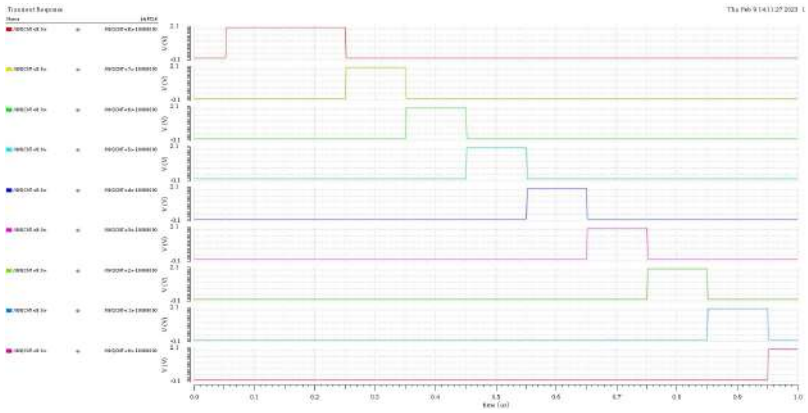

Figure 10: Counter output

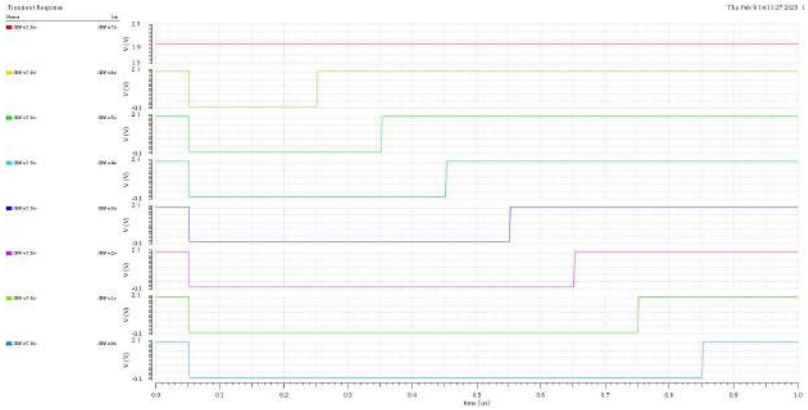

Figure 11: Code register output

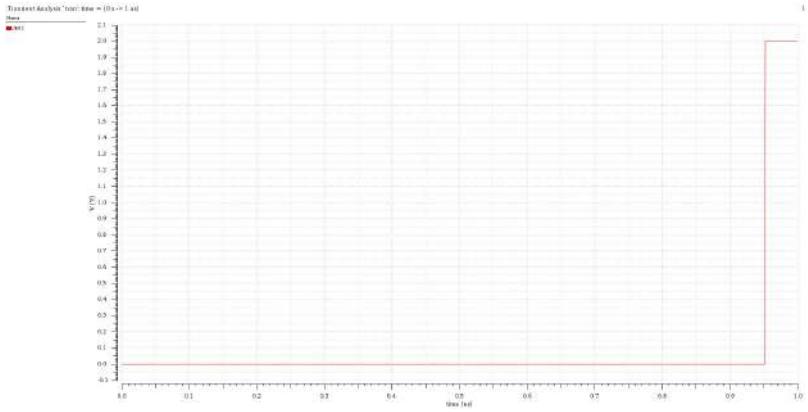

Figure 12: EOC

2.2.3 CMP is alternating ones and zeros

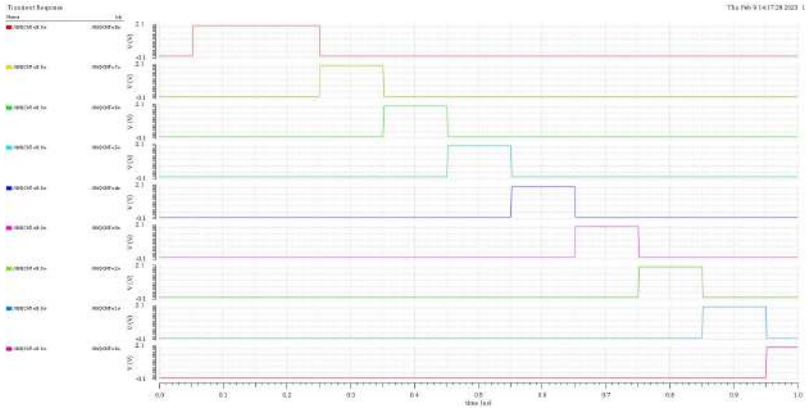

Figure 13: Counter output

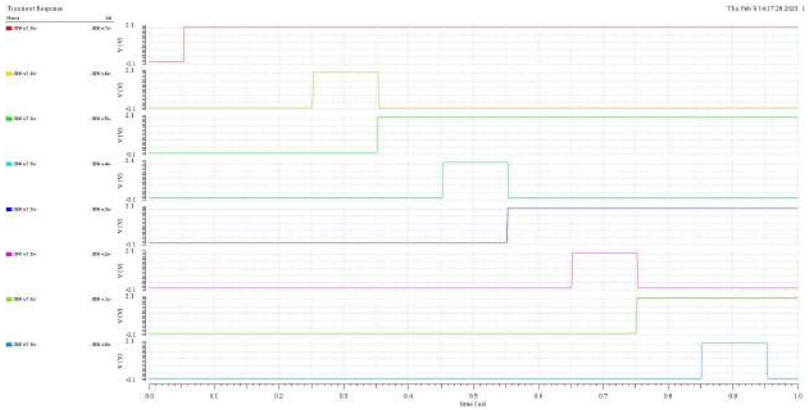

Figure 14: Code register output

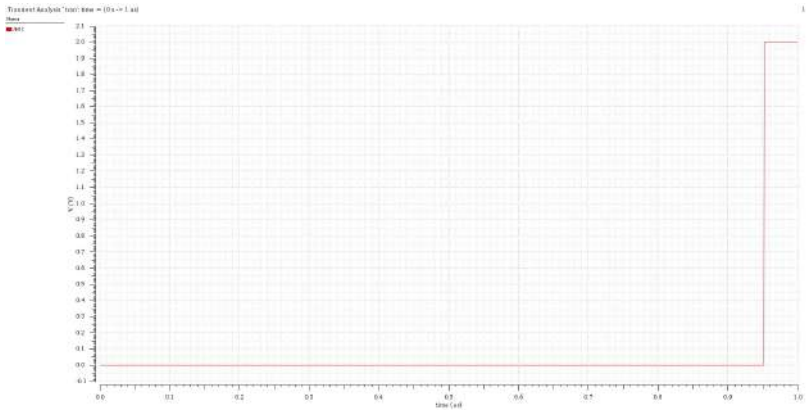

Figure 15: EOC

Clock cycle	DW7	DW6	DW5	DW4	DW3	DW2	DW1	DW0	CMP
1	0	0	0	0	0	0	0	0	-
2	1	0	0	0	0	0	0	0	C9
3	C7	1	0	0	0	0	0	0	C8
4	C7	C6	1	0	0	0	0	0	C7
5	C7	C6	C5	1	0	0	0	0	C6
6	C7	C6	C5	C4	1	0	0	0	C5
7	C7	C6	C5	C4	C3	1	0	0	C4
8	C7	C6	C5	C4	C3	C2	1	0	C3
9	C7	C6	C5	C4	C3	C2	C1	1	C2
10	C7	C6	C5	C4	C3	C2	C1	C0	-

Table 1: SAR logic summary

3 SAR ADC Testbench

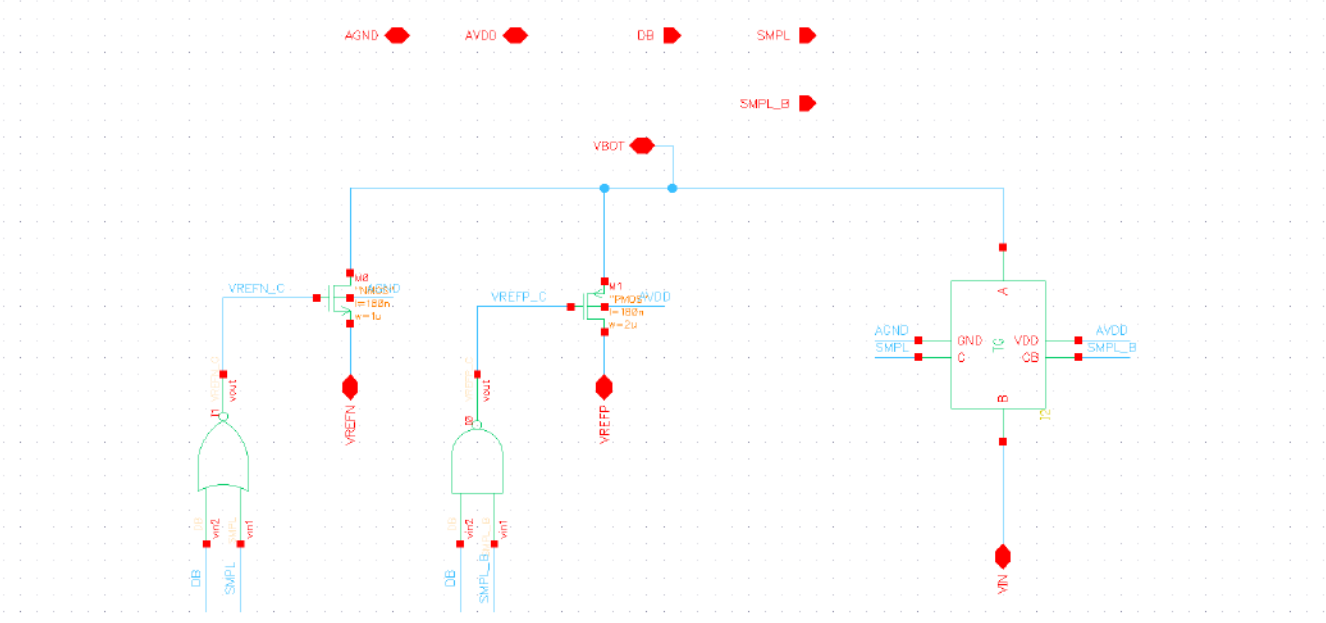

Figure 16: Bottom plate switch

– When the sampling clock is high, all capacitors' bottom plates will be connected to VIN. Then, they will be connected to VREFN or VFERP depending on the code register output.

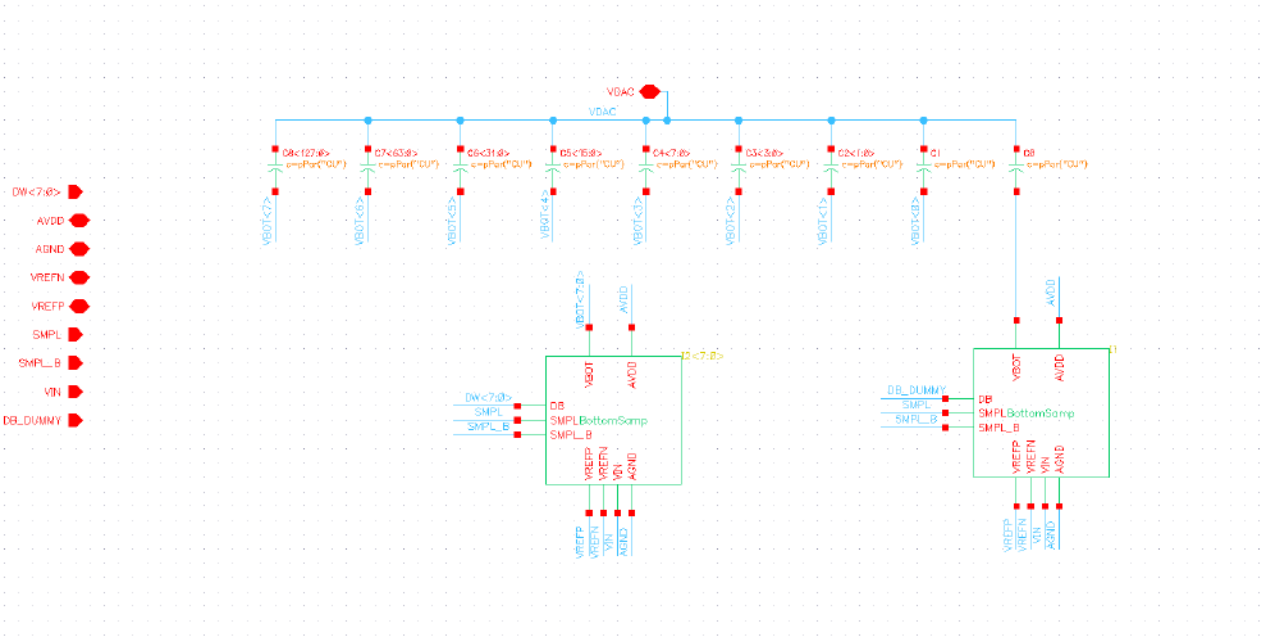

Figure 17: Capacitive DAC

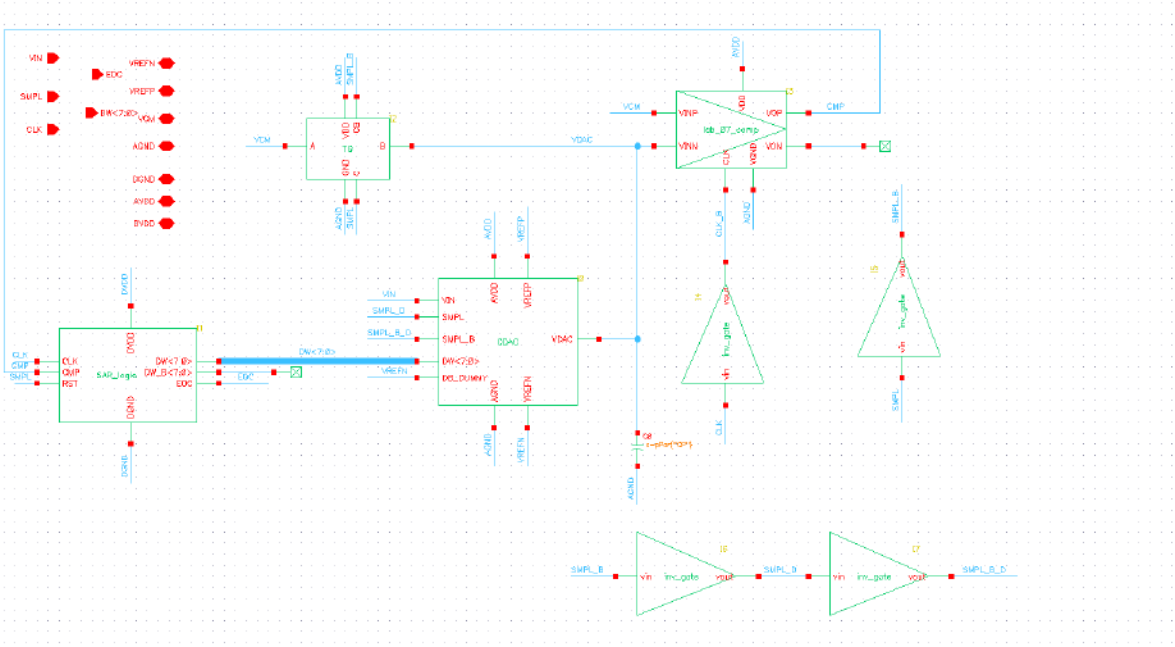

Figure 18: SAR ADC

4 DC Functional Test

4.1 VIN = VREFN

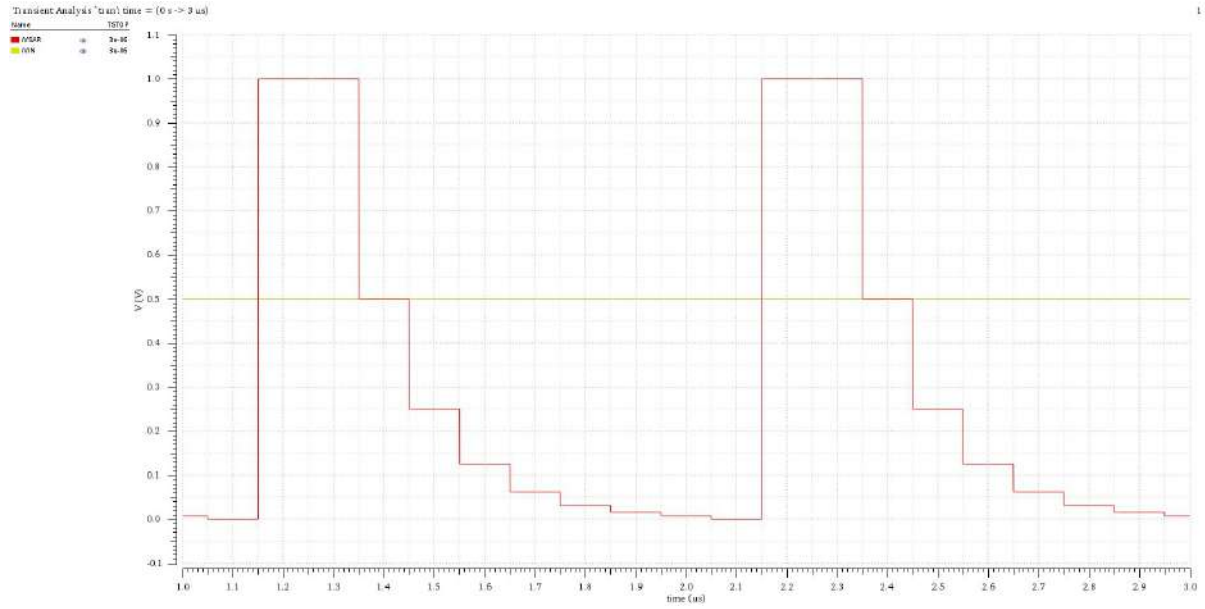

Figure 19: VIN VS VSAR

4.2 VIN = VREFP

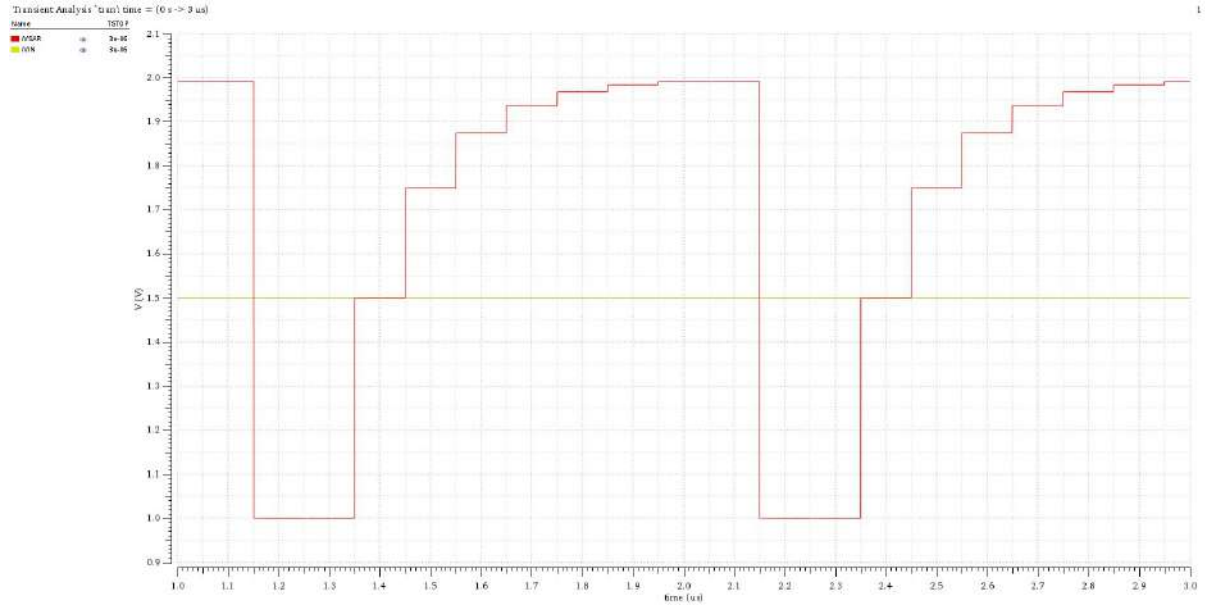

Figure 20: VIN VS VSAR

4.3 VIN = VREFN + (128+32+8+2+0.5)*VLSB

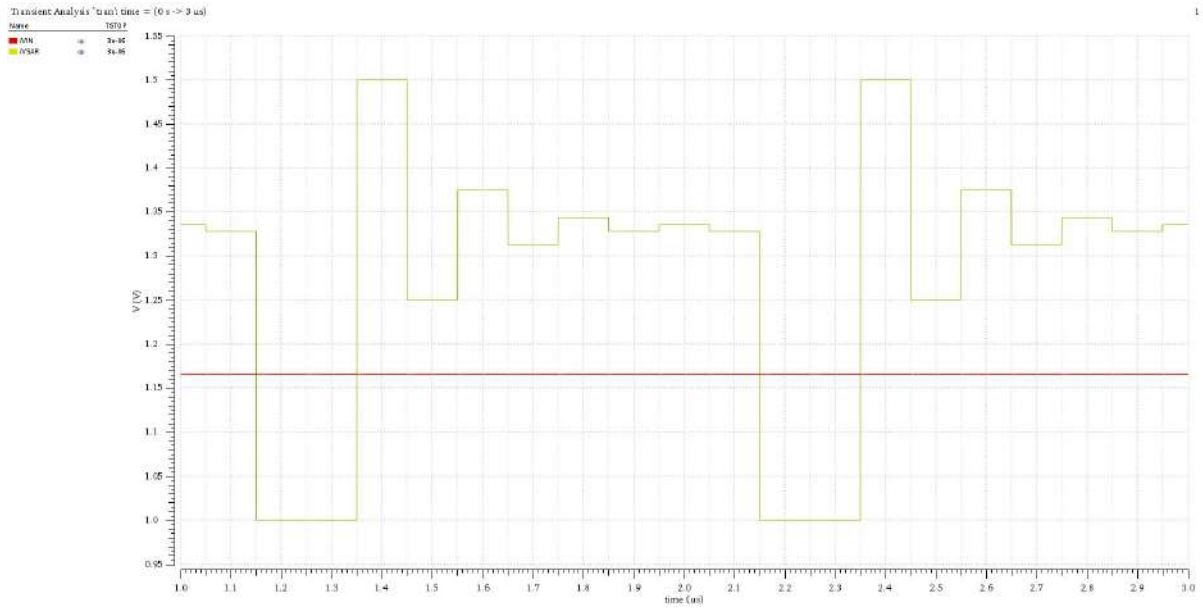

Figure 21: VIN VS VSAR

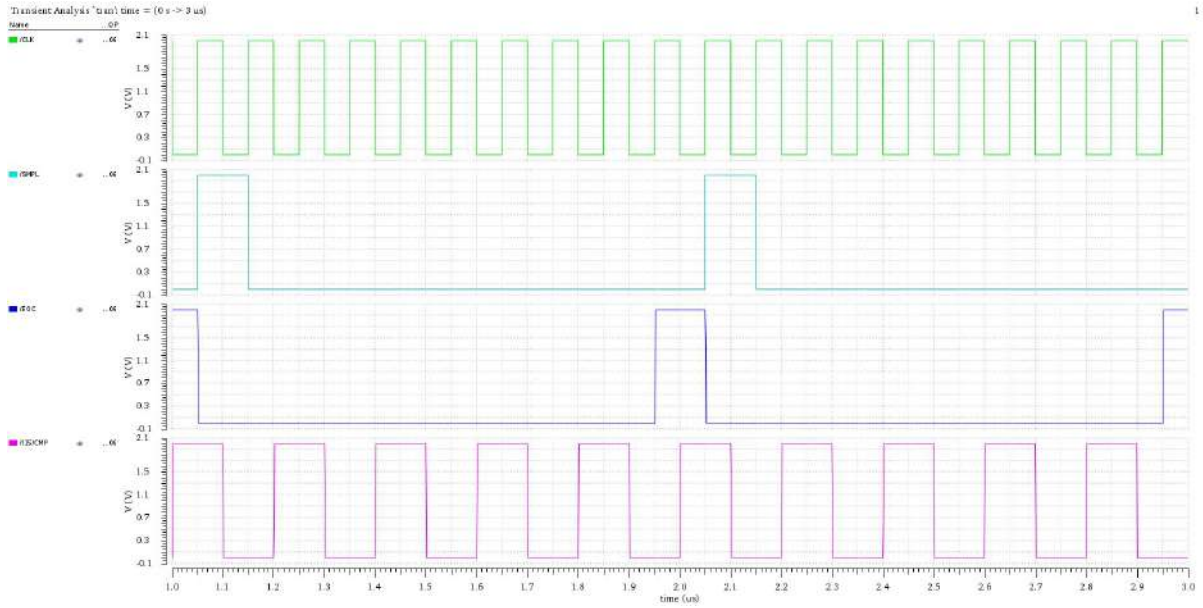

Figure 22: CLK & CMP & EOC & SMPL

5 Sine Wave Test

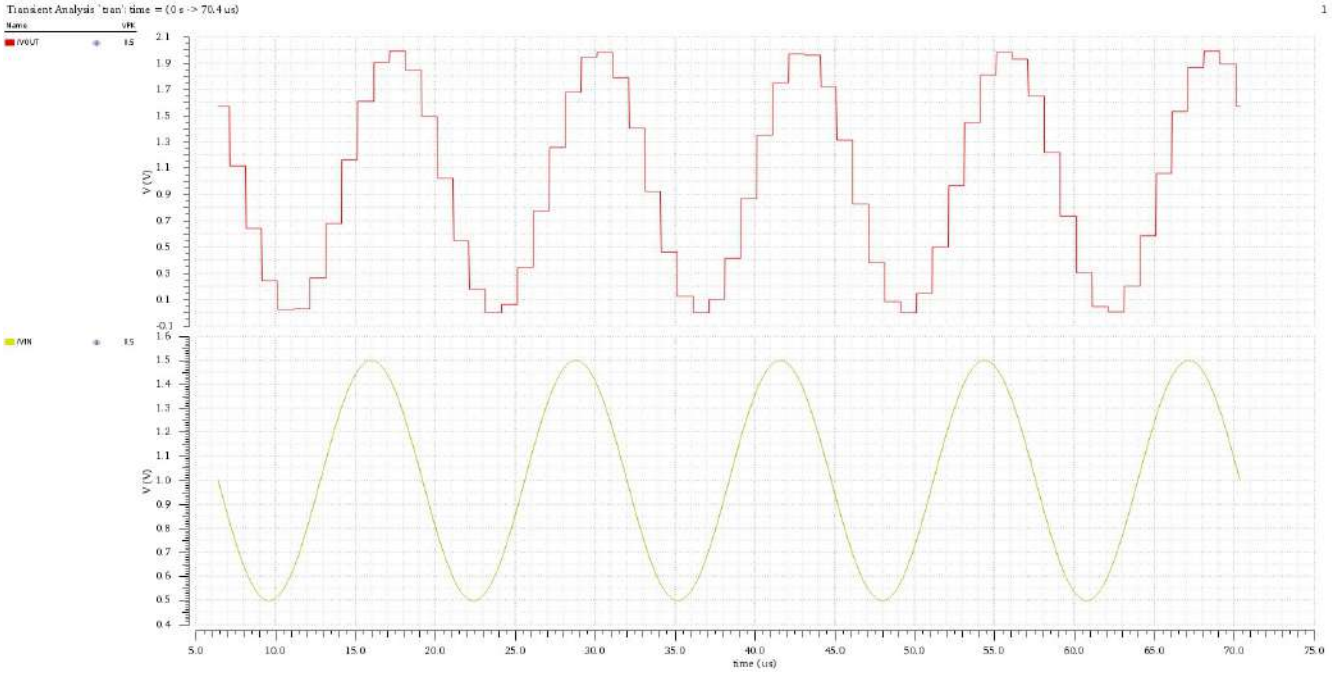

Figure 23: VOUT with sinusoidal VIN

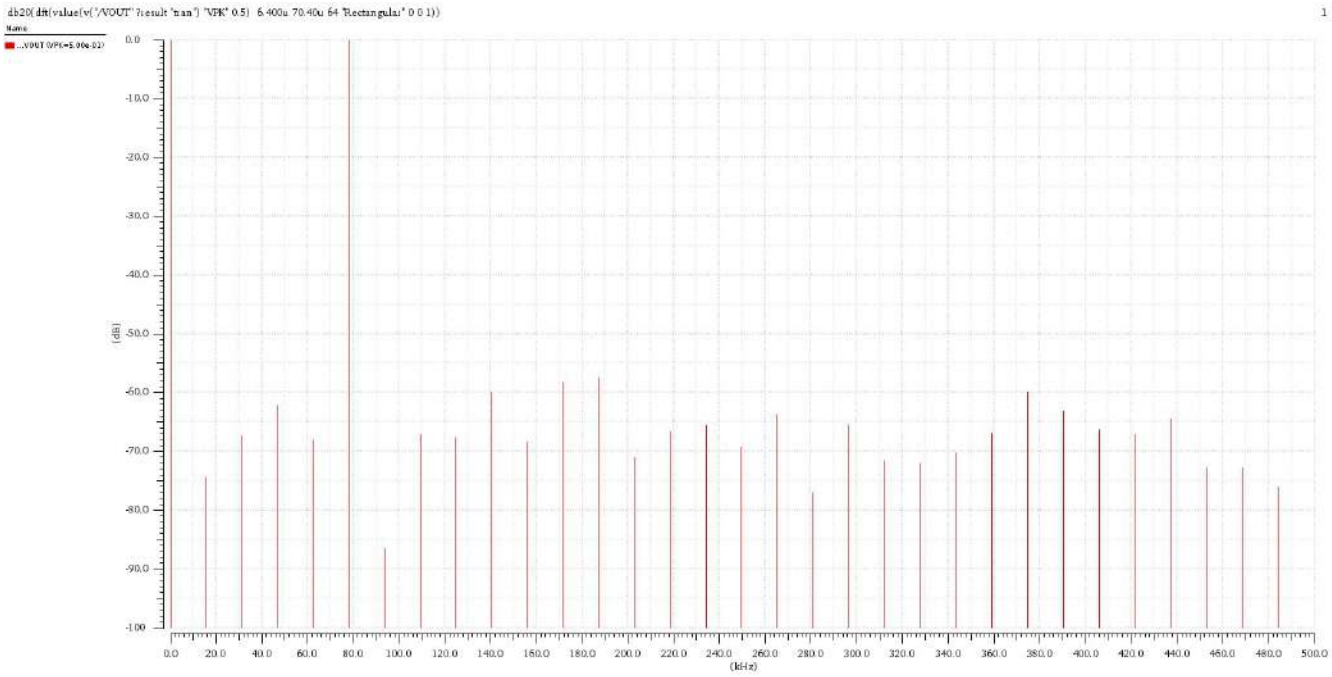

Figure 24: VOUT FFT

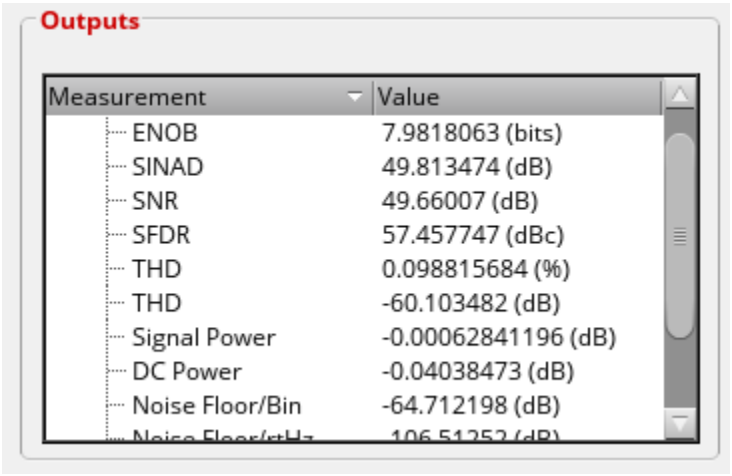

Figure 25: Performance parameters

6 Fully-Differential SAR ADC

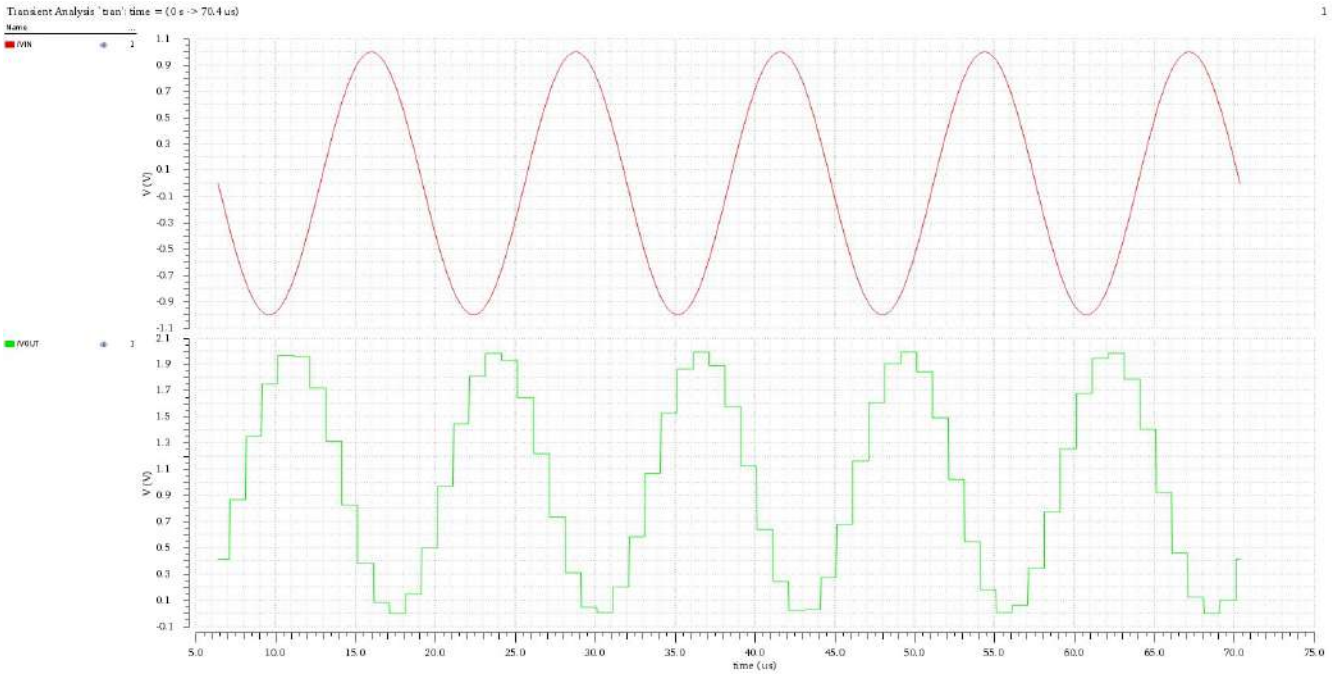

Figure 26: Fully differential operation

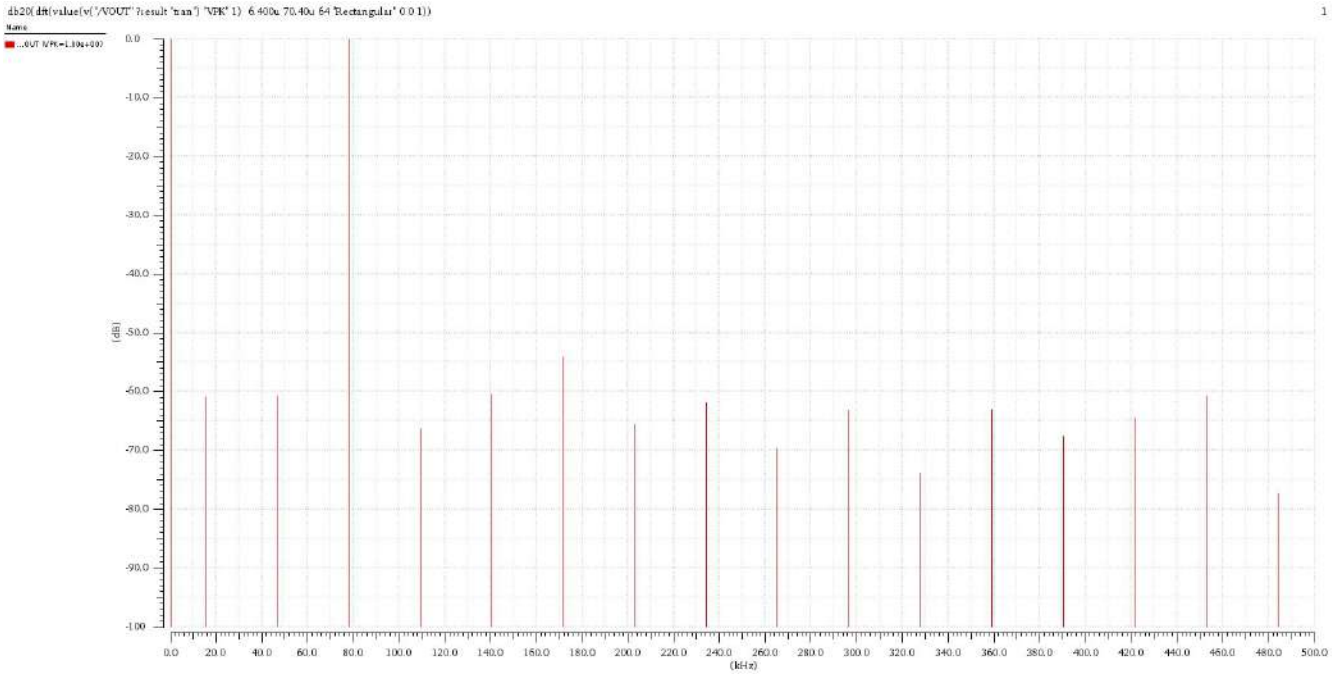

Figure 27: VOUT FFT

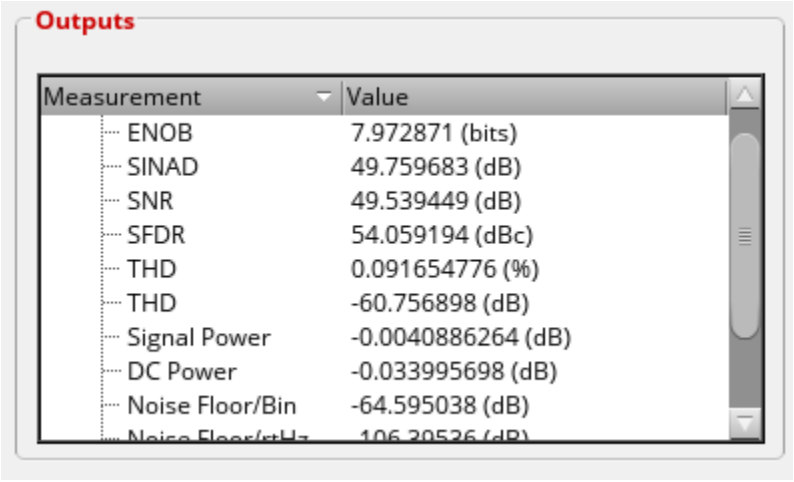

Figure 28: Performance parameters

7 References

– Hedayati, R. (2011). *A Study of Successive Approximation Registers and Implementation of an Ultra-Low Power 10-bit SAR ADC in 65nm CMOS Technology* [Master's Thesis, Linköping University]. ResearchGate. www.researchgate.net/publication/318469027 _A_Study_of_Successive_Approximation_Registers_and_Implementation_of_an_UltraLow_Power_10bit_SAR_ADC_in_65nm_CMOS_Technology