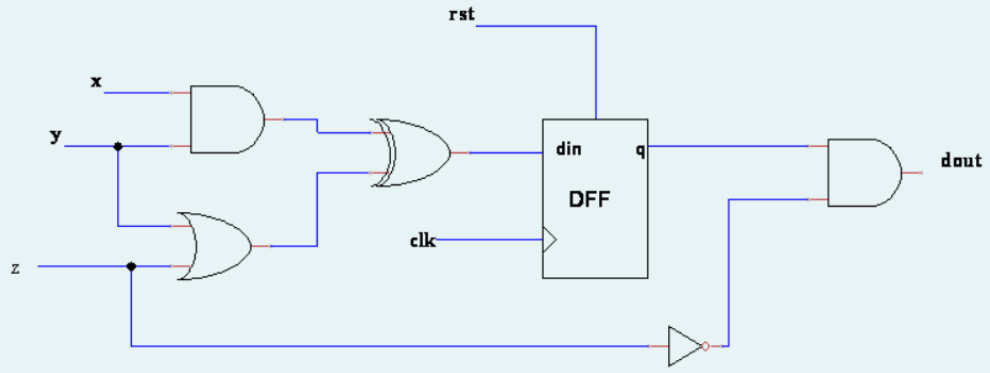
Which of the following represents the correct code for the following circuit?



a.

```
library ieee;

use ieee.std_logic_1164.all;

use ieee.std_logic_arith.all;

entity circuit_1 is

port (x,y,z,clk,rst: in std_logic;

dout: out std_logic);

end entity circuit_1;

architecture rtl of circuit_1 is

signal q,n,m,din :std_logic;

begin

process (clk,rst)

begin

if (rst ='1')then

q <= '0';

elsif (rising_edge(clk)) then

n <= x AND y;

m <= y OR z;

din <= n XOR m;

q <= din;

end if;

end process;

end rtl;
```

b. b & C

c.

```
library ieee;

use ieee.std_logic_1164.all;

use ieee.std_logic_arith.all;

entity circuit_1 is

port (x,y,z,clk,rst: in std_logic;

dout: out std_logic);

end entity circuit_1;

architecture rtl of circuit_1 is

signal q,n,m,din :std_logic;

begin

n <= x AND y;

m <= y OR z;

din <= n XOR m;

process (clk,rst)

begin

if (rst ='1')then

q <= '0';

elsif (rising_edge(clk)) then

q <= din;

end if;

end process;

end rtl;
```

○ d.

```
library ieee;

use ieee.std_logic_1164.all;

use ieee.std_logic_arith.all;

entity circuit_1 is

port (x,y,z,clk,rst: in std_logic;

dout: out std_logic);

end entity circuit_1;

architecture rtl of circuit_1 is

signal q :std_logic;

begin

process (clk,rst)

variable n,m,din :std_logic;

begin

if (rst ='1')then

q <= '0';

elsif (rising_edge(clk)) then

n := x AND y;

m := y OR z;

din := n XOR m;

q <= din;

end if;

end process;

end rtl;
```

Which of the following can't be declared in an architecture directly?

- a. Constant
- b. Signal
- c. Bit_Vector
- d. Variable

How many types of resets are there in hardware design?

- a. One
- b. Three
- c. Two
- d. Four

```
entity reg_par is

port (clk rst: in std_logic;

reg_in: in std_logic_vector(7 down  to 0);

reg_out: out std_logic_vector(7 downto 0);

end entity reg_par;

architecture rtl of reg_par is

begin

process (clk)

begin

if (rst = '1') then

reg_out <= "00000000"

elseif (rising_edge(clk)) then

reg_out <= reg_in;

end if;

end process;

end architecture rtl;
```

- ○ a. None of All
- ◉ b. 3

Which of the following is correct syntax for entity declaration?

a.
```
ENTITY entity_name
  PORT port_name
  (signal_names : signal_modes;
  signal_names : signal_modes);
 END ENTITY;
```

b.
```
ENTITY entity_name IS
  PORT port_name
  ( signal_names : signal_modes signal_type;
  signal_names : signal_modes signal_type);
 END entity_name;
```

c.
```
ENTITY entity_name IS
  PORT( signal_names : signal_modes;
  signal_names : signal_modes);
 END entity_name;
```

d.
```
ENTITY entity_name
  PORT( signal_names : signal_modes;
  signal_names : signal_modes);
```

```
begin

if (rst ='1')then

q <= '0';

elsif (rising_edge(clk)) then

n := x & y;

m := y OR z;

din := n XOR m;

q <= din;

end if;

end process;

dout1 <= q;

dout2 <= din;

end rtl;
```

- a. 3
- b. 2
- c. None of All
- d. 4

During synthesis, a variable infers _____

- a. Flip flop
- b. Wire
- c. Register
- d. Variables are not synthesizable

Why we needed HDLs (Hardware Description Languages) while having many traditional Programming languages?

- a. Traditional programming languages are complex
- b. Some characteristics of digital hardware couldn't be captured by traditional languages
- c. HDLs are complementary to traditional programming languages to complete the design process
- d. HDLs offer more complexity than traditional programming languages.

If the declarative part in the architecture of a half adder is as below

```
ARCHITECTURE     OF my_logic IS
 BEGIN
y <= (a AND c) AND (b OR c);
END ARCHITECTURE;
```

- a. Behavior
- b. None of All
- c. Structure
- d. Data flow

Which of the following is not defined by the entity?

- a. Names of signal
- b. Behavior of the signals
- c. Direction of any signal
- d. Different ports

Clear my choice

Why do we need to define clock signal in the sensitivity list of the process?

- a. To trigger the statement as soon as there is some event on input
- b. To trigger the clock signal as soon as there is some event on input
- c. To trigger the statement as soon as there is some event on clock
- d. To trigger the clock signal as soon as there is some event on output

What will be the output in the following code?

```
ARCHITECTURE my_logic OF my_design IS
BEGIN
a <= '1';
b <= '1';
PROCESS (a, b)
BEGIN
IF (a AND b = '1') THEN
output <= a;
ELSIF (a OR b = '1') THEN
output <= b;
ELSE
output <= '0';
END IF;
END PROCESS;
END my_logic;
```

- a. 1
- b. b
- c. a
- d. 0

What is the difference between SIGNAL and VARIABLE?

- a. SIGNAL can be used for input or output whereas VARIABLE acts as intermediate signals
- b. SIGNAL is global and VARIABLE is local to the process in which it is declared
- c. The value of SIGNAL never varies whereas VARIABLE can change its value
- d. SIGNAL depends upon VARIABLE for various operations

FPGA stands for...

- [x] a. Field Programmable Gate Array
- [ ] b. Field Program Gate Array
- [ ] c. First programmable Gate Array
- [ ] d. First Program Gate Array

Clear my choice

a.

```
ARCHITECTURE rtl of circuit_1 is

BEGIN


PROCESS ()


                -- Here


BEGIN


END PROCESS;
```

b.

```
ARCHITECTURE rtl of circuit_1 is


                -- Here

BEGIN

PROCESS ()

BEGIN
```

The cells in a FPGA may contain registers, look-up tables and memory

- a. True
- b. False

Clear my choice

Which of the following circuit can't be described without using a process statement?

- a. D flip-flop
- b. Decoder
- c. Comparator
- d. Multiplexer

Synchronous reset is a fast reset.

- a. True
- b. False

Clear my choice

Which of the following circuit can be used as parallel to serial converter?

- a. Demultiplexer
- b. Decoder
- c. Multiplexer
- d. Digital counter

VHDL is one of the programming languages

- a. False
- b. True

Clear my choice

Which of the following sequential circuit doesn't need a clock signal?

- a. Shift register
- b. Flip flop
- c. Asynchronous counter
- d. Latch

Clear my choice

If a user gets an error at the time which is "the IF statement is illegal" what could be the reason?

- a. Using IF statement without ELSE
- b. Using multiple ELSIF statements
- c. Using IF statement in architecture body directly
- d. Using concurrent assignment in the IF

Clear my choice