















Not yet answered

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F Flag question

FPGA stands for...

- O a. First Program Gate Array
- b. Field Programmable Gate Array
- O c. First programmable Gate Array
- O d. Field Program Gate Array

Not yet answered

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P Flag question

For using a process to implement combinational circuit, which signals should be in the sensitivity list?

Select one:

- O a. Output of the circuit
- O b. No signal should be in the sensitivity list
- O c. Both of the inputs and outputs
- d. Inputs of the circuit

Not yet answered

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F Flag question

What is the correct code for a shift left register that can shift the input data by 3 bits?

```
O a. library ieee;
       use ieee.std_logic_1164.all;
       use ieee.std_logic_arith.all;
       entity reg par is
       port (clk, rst: in std_logic;
       reg_in: in std_logic_vector(7 downto 0);
       reg_out: out std_logic_vector(7 downto 0));
       end entity reg par;
       architecture rtl of reg par is
       signal reg_temp: std_logic_vector (7 downto 0);
       begin
       process (rst, clk)
       begin
       if (rst = '1') then
       reg_temp <= "00000000";
       elsif (rising edge(clk)) then
       reg_temp <= "111" & reg_temp (7 downto 3);
       end if;
       end process;
       reg_out <= reg_ temp;
       end architecture rtl;
O b. library ieee;
       use ieee.std_logic_1164.all;
```

use ieee.std_logic_arith.all;







Not yet answered

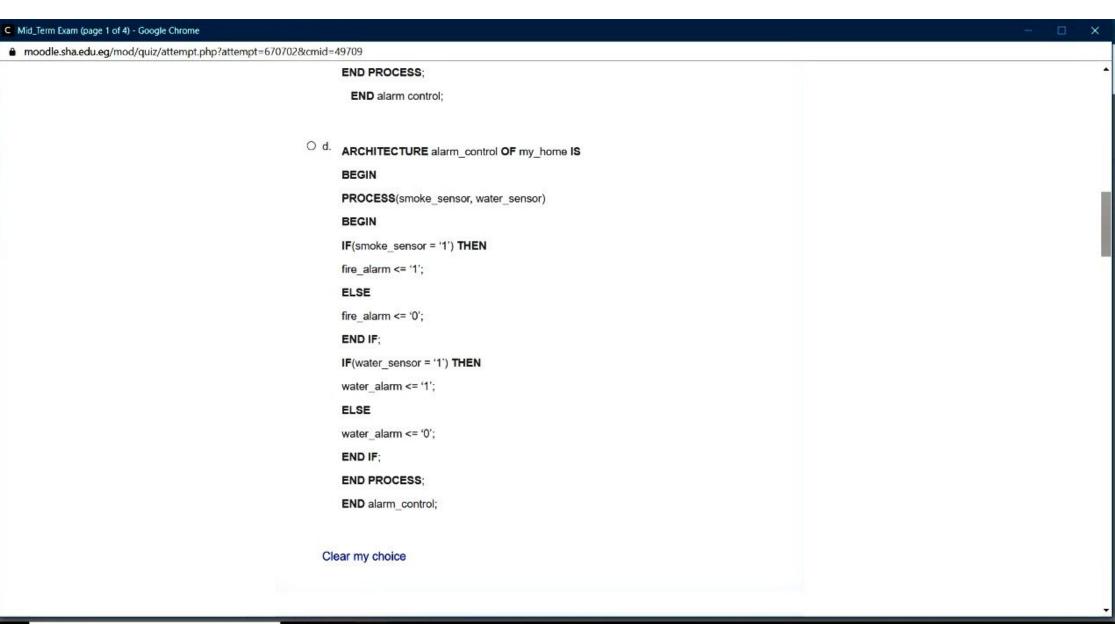
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F Flag question

Difference between simulation tools and Synthesis tool is _____

Select one:

- O a. Simulators and Synthesis tools works exactly same
- b. Simulators are used to check the performance of circuit and Synthesis tools are for the fabrication of circuits
- c. Simulators are used just to check basic functionality of the circuit and Synthesis tools includes timing constraints and other factors along with simulation
- O d. Simulation finds the error in the code and Synthesis tool corrects the code







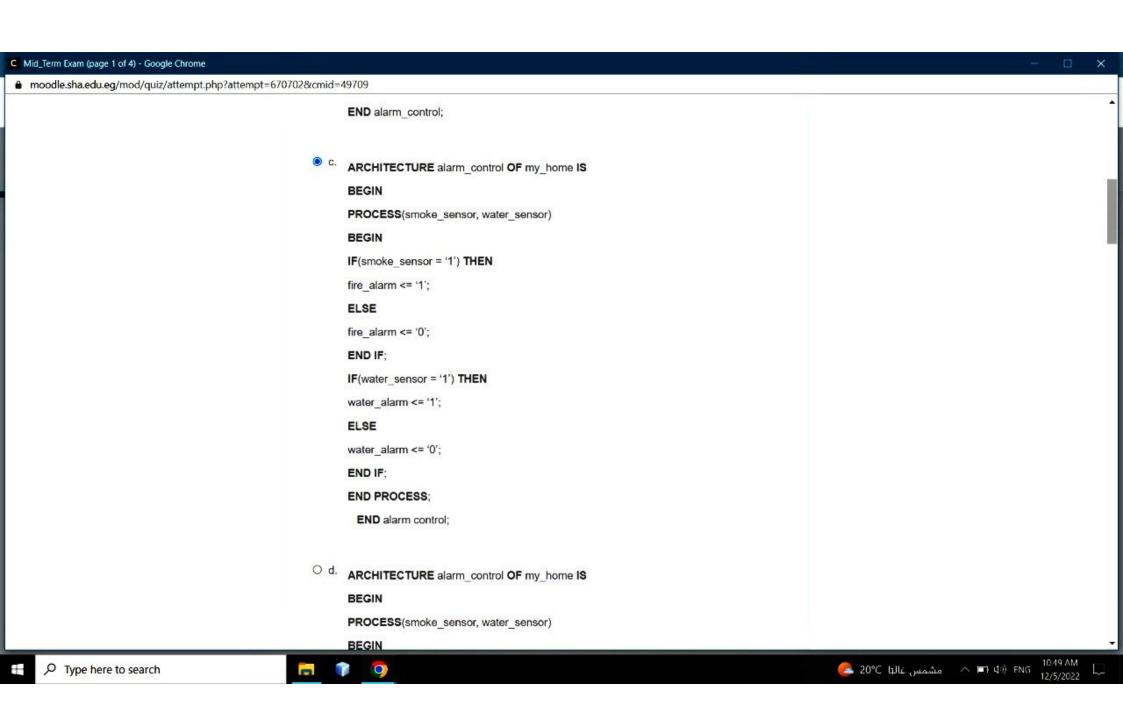












Not yet answered

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Which of the following is a not a characteristics of combinational circuits?

Select one:

- O a. There is no storage element in combinational circuit
- O b. There is no use of clock signal in combinational circuits
- O c. The output of combinational circuit depends on present input
- d. The output of combinational circuit depends on previous output

Clear my choice

QUESTION 15

Not yet answered

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Flag question

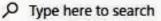
Sequential code can't be used to design combinational circuit.

Select one:

- a. False
- O b. True















Not yet answered

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F Flag question

QUESTION 10

Not yet answered

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F Flag question

VHDL is one of the programming languages

- a. False
- O b. True

Clear my choice

During synthesis, a variable infers _____

- O a. Flip flop
- b. Compantorial circuit
- O c. Variables are not synthesizable
- O d. Register

Not yet answered

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F Flag question

If only two bit vectors are allowed to use in the VHDL code, then how many number of multiplexers will be required to implement 4 to 1 Multiplexer?

Select one:

- O a. 4
- O b. 1
- c. 3
- O d. 2

Not yet answered

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Flag question

If the declarative part in the architecture of a half adder is as below

ARCHITECTURE OF my_logic IS

BEGIN

 $y \le (a AND c) AND (b OR c);$

END ARCHITECTURE;

- O a. Data flow
- b. Structure
- O c. None of the mentioned
- O d. Behavior











Not yet answered

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F Flag question

QUESTION 7

Not yet answered

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P Flag question

In which of the situations listed below would a designer use an FPGA?

Select one:

- O a. The system should be fast.
- O b. Only few copies of the system will be produced and we have a limited budget to spend on all the components.
- O c. The system should be as power efficient.

Which of the following circuit can be used as parallel to serial converter?

- O a. Demultiplexer
- Multiplexer
- Decoder
- O d. Digital counter



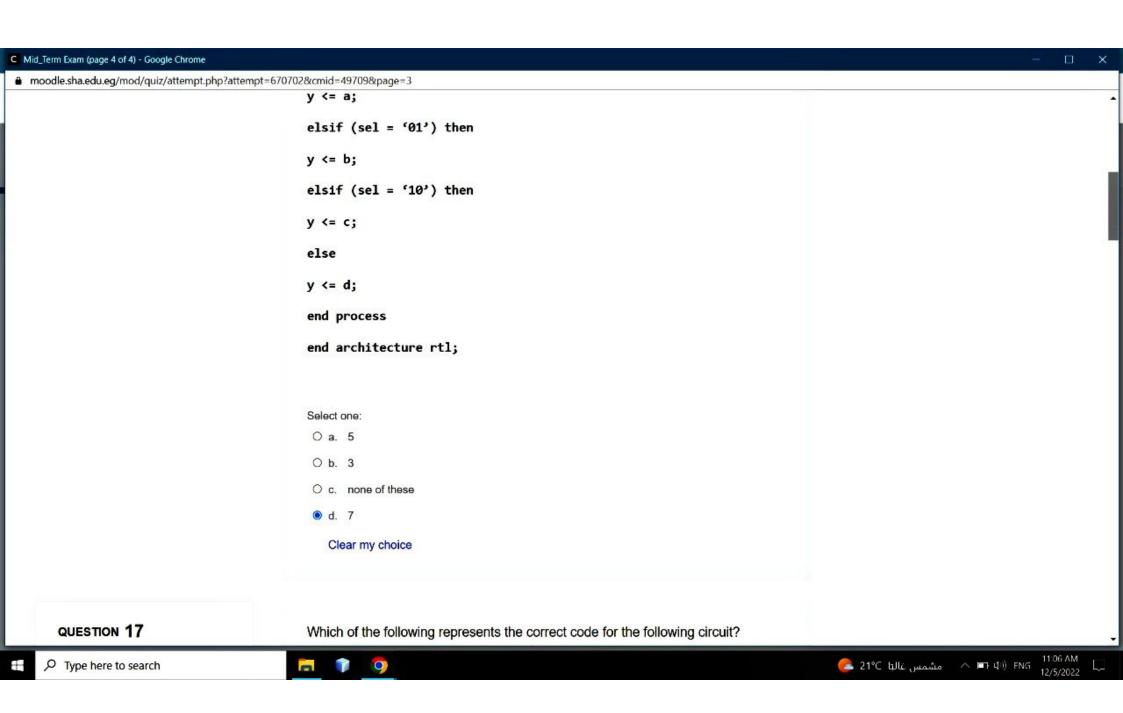












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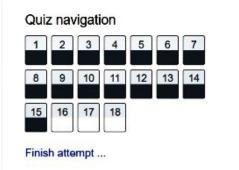
QUESTION 16

Not yet answered

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F Flag question

The number of errors in the following code is _____ library ieee; use ieee.std logic 1164.all; use ieee.std_logic_arith.all; entity mux4 1 is port (sel: in std_logic_vector (0 to 1); a, b, c, d: in std_logic_vector(7 downto 0); y: out std_logic_vector(7 downto 0); end entity mux4_1; architecture rtl of mux4_1 is begin process (sel) begin if (sel = '00') then





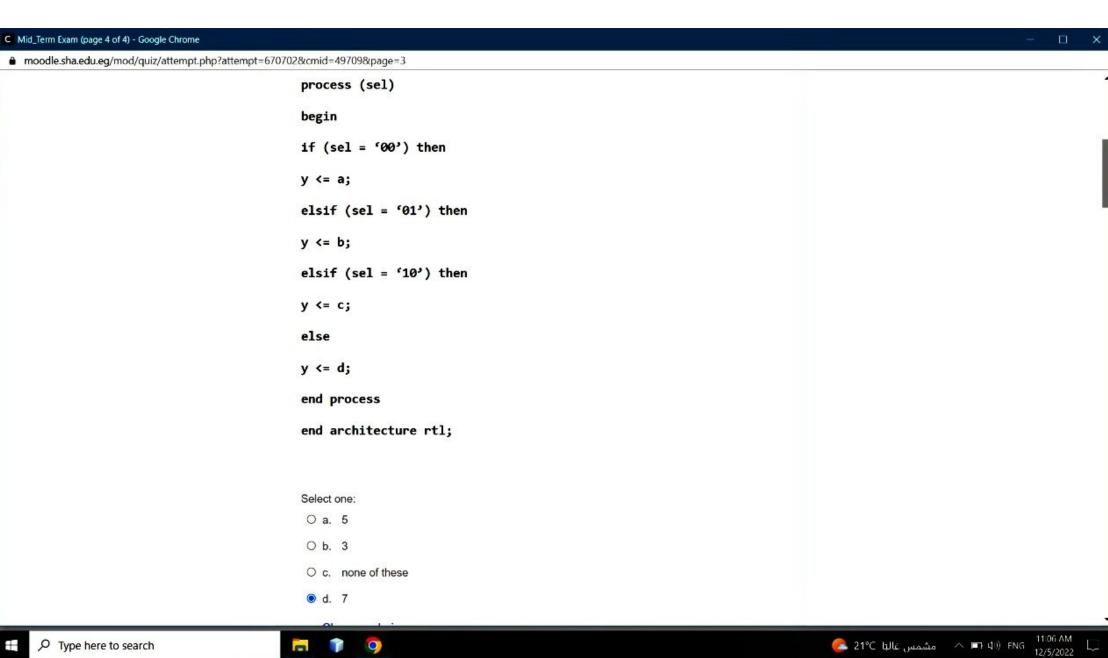




















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P Flag question

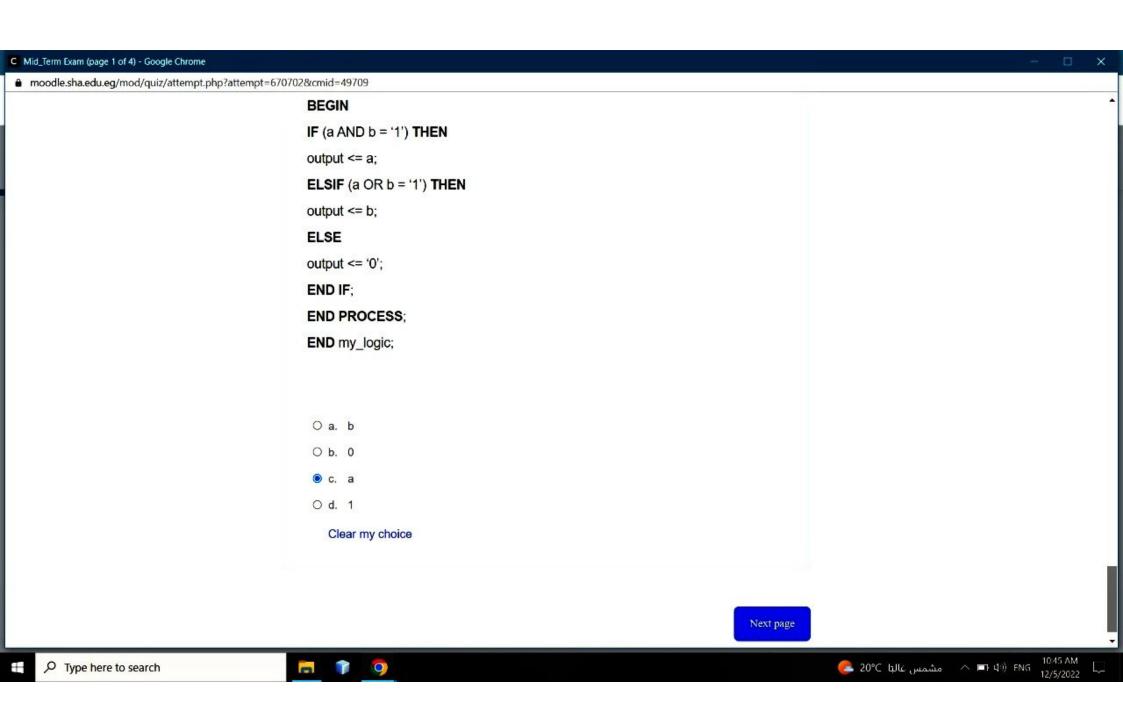
Which of the following sequential circuit doesn't need a clock signal?

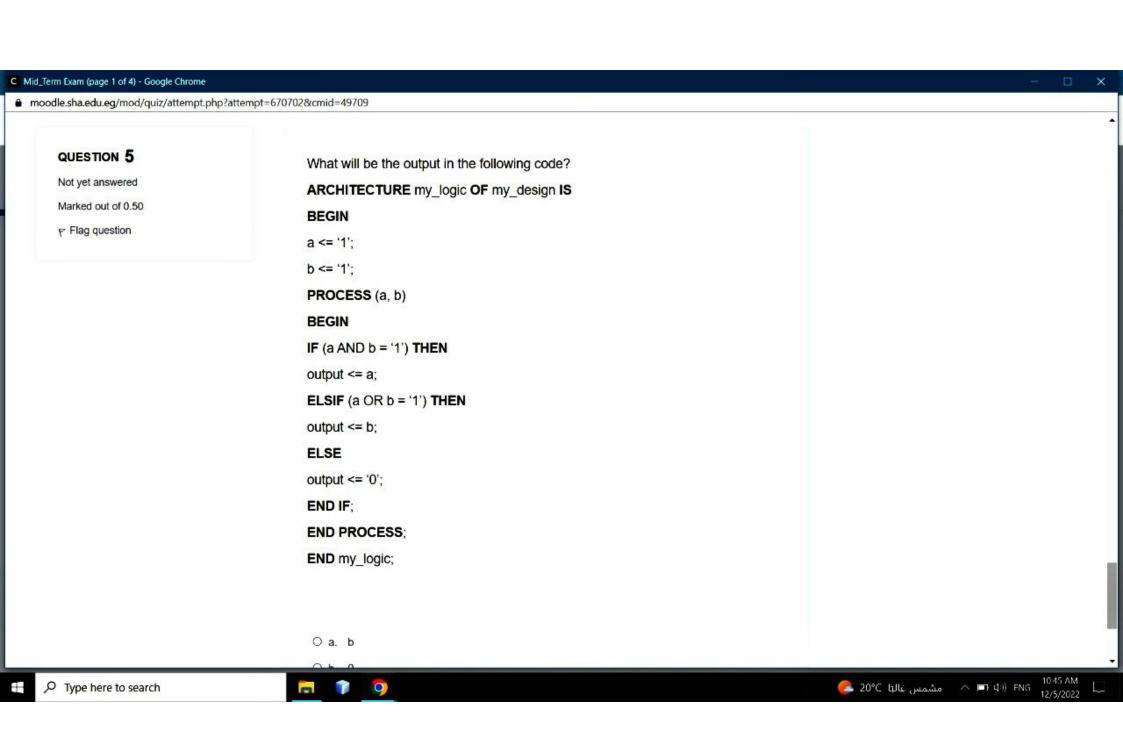
O a. Asynchronous counter

O b. Flip flop

O c. Shift register

d. Latch







Not yet answered

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F Flag question

A user wants to implement a logic by using VHDL. In which he has inputs from two sensors which are smoke sensor and water level detector. If any input is high, he has to turn on the respective alarm. Which of the following is representing the correct code for the given logic?

Select one:

O a. a&c

ARCHITECTURE alarm control OF my home IS

BEGIN

PROCESS(smoke sensor, water sensor)

BEGIN

IF(smoke_sensor = '1') THEN

fire_alarm <= '0';

ELSE

fire_alarm <= '1';

END IF:

IF(water_sensor = '1') THEN

water_alarm <= '1';

ELSE

Quiz navigation

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15 16 17 18

Finish attempt ...















