EL DOFDE
ORGANIZATION

Sheet 02
Answers

References
Shefaa Sections

Computer
Architecture

No Excellence
Just Pass

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Sec:- 2 Date: / /

2] Virtual memory = 2^{10} → Virtual address = 10 bits
physical memory = 2^8 → physical address = 8 bits
n.pages = $2^{10}/2^4 = 2^6$ → Page bits = 6 bits
n.frames = $2^8/2^4 = 2^4$ → frame bits = 8 bits

(a) n.pages in Virtual = 2^6 = 64 page
(b) n.frames in physical = 2^4 = 16 frame
(c) n.entries in page table = n.frames = 16 entry

3] 2-way set associative Cache → set = 2 blocks
Cache Block = 8 = 2^3 byte → offset = 3 bit
n.sets = 2^1 → set = 1 bit
Main memory size = $2^2 * 2^4 = 2^6$ → physical address = 6 bit
n.frames = 2^2 → frame = 2 bits

Virtual memory size = $2^3 * 2^4 = 2^7$ → Virtual address = 7 bit
n.pages = 2^3 → Page = 3 bits

3	4		2	4		2	1	3
Page	offset		Frame	offset		Tag	Set	offset
Virtual address			Physical address		=	Cache address		

(a) n.bits for virtual address = 7

(b) n.bits for physical address = 6

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© 0x12 → Virtual address → 001010
→ located in page 1 and frame 0 "From page table"
→ physical address → 000010
replace page bits with frame 0 bits.

ⓓ 0x0B → Virtual address → 0X36 → physical address
0X36 → 110110 → Tag, set, offset
→ Located in Set 0 after overwritting on Block(I)
→ Located in frame 3, offset 6

ⓔ 0x19 → Virtual address
→ Located in frame 0
→ physical address → 001001

Data accessing: After CPU generates a virtual address, It know it's location in virtual memory, Then check for frame in TLB, if miss, it goes to page table and check there. if miss, it is a page fault and get the data from virtual memory to free frame in main memory, or evict frame when it's full. then copy physical address Block to cache.

The previous proccess occurs when Data in Cache is missed.

4] No, Because TLB is smaller than page table in size, and it store the most recent paging of virtual pages to physial so when TLB miss, it maybe hit in page table.

* TLB Stores only a subset of page table *