

The Higher Institute of Engineering

Shorouk City

Course Name : Electronic Circuits
Design using computer

Course Code : ECE 312

Date of Exam : 10/3/2019



2nd

Semester
Academic Year
2018/2019

Time Allowed : (0.15) Hours

Level: 3rd year

Department : Communication
and Computer Eng.

Quiz (1)

Answer the Following

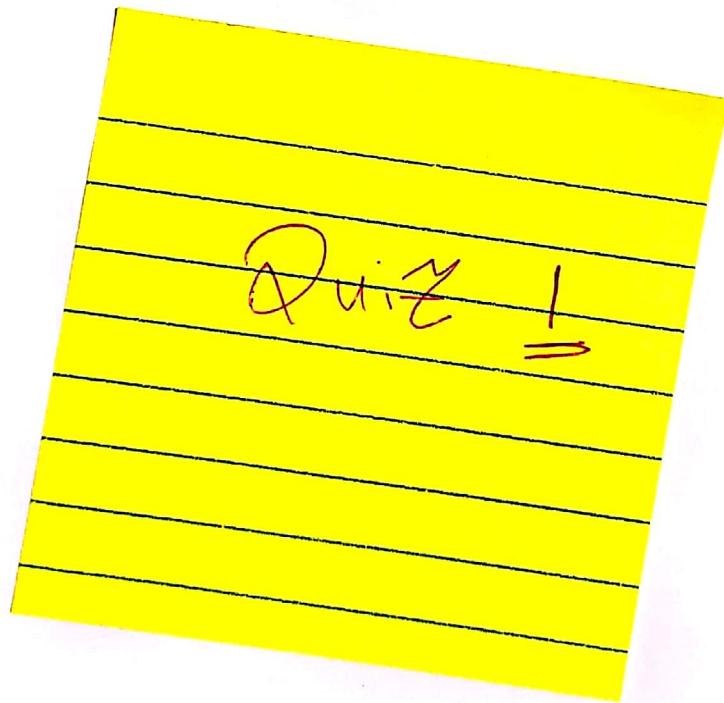
Intended Learning Outcomes (ILOS)

Q1	Knowledge & Understanding	Intellectual Skills	Practical Skills
	(k2,k3)	(i2)	(p2)

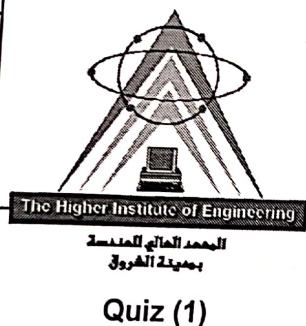
Write A VHDL code for 5-1 Multiplexer

Examiner :Dr. Fatma Elfouly

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The Higher Institute of Engineering	
Shorouk City	
Course Name : Electronic Circuits	
Design using computer	
Course Code : ECE 312	
Date of Exam : 10/3/2019	



2nd	Semester Academic Year 2018/2019
	Time Allowed : (0.15) Hours
	Level: 3rd year
	Department : Communication and Computer Eng.

Answer the Following

Q1	Intended Learning Outcomes (ILOS)			Marks (6)
	Knowledge & Understanding	Intellectual Skills	Practical Skills	
	(k2,k3)	(i2)	(p2)	

Write A VHDL code for 5-1 Multiplexer

Examiner :Dr. Fatma Elfouly	Page 1/1	Total Marks
		(6)

الحالات
VLSI

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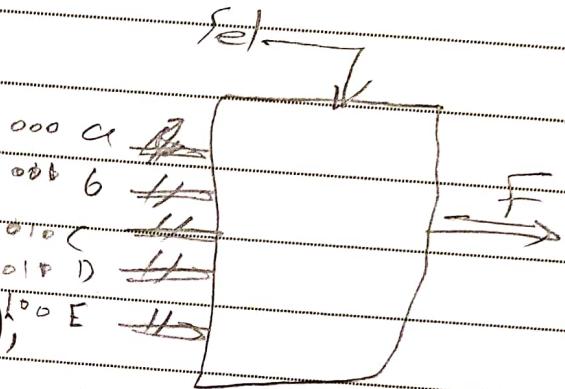
~~PMHDs MAX = 1 X 5~~

~~Port(a,b,c,d,e) : STD-logic Vector(4 downto 0);~~

~~sel : in STD-logic Vector(2 downto 0);~~

~~F : out : STD-logic Vector(4 downto 0);~~

~~end Max = 1;~~



Architecture RTL of max 1 is
begin

process (sel)

begin

if (sel = "000") then F <= a;

elsif (sel = "001") then F <= b;

elsif (sel = "010") then F <= c;

elsif (sel = "011") then F <= d;

elsif (sel = "100") then F <= e;

else F <= "00000";

endif;

end process;

end RTL;

The Higher Institute of Engineering

Shorouk City

**Course Name : Electronic Circuits
Design using computer**

Course Code : ECE 312

Date of Exam : 7/4/2019



Quiz (2)

2nd

**Semester
Academic Year
2018/2019**

Time Allowed : (0.15) Hours

Level: 3rd year

**Department : Communication
and Computer Eng.**

Answer the Following

Q1	Intended Learning Outcomes (ILOS)			Marks (6)
	Knowledge & Understanding (k2,k2)	Intellectual Skills	Practical Skills	
	(-)	(-)	(-)	

Design the finite state machine FSM needed for a sequence detector to detect the sequence (i.e. "01001") when applied at its input in overlapping and non-overlapping modes.

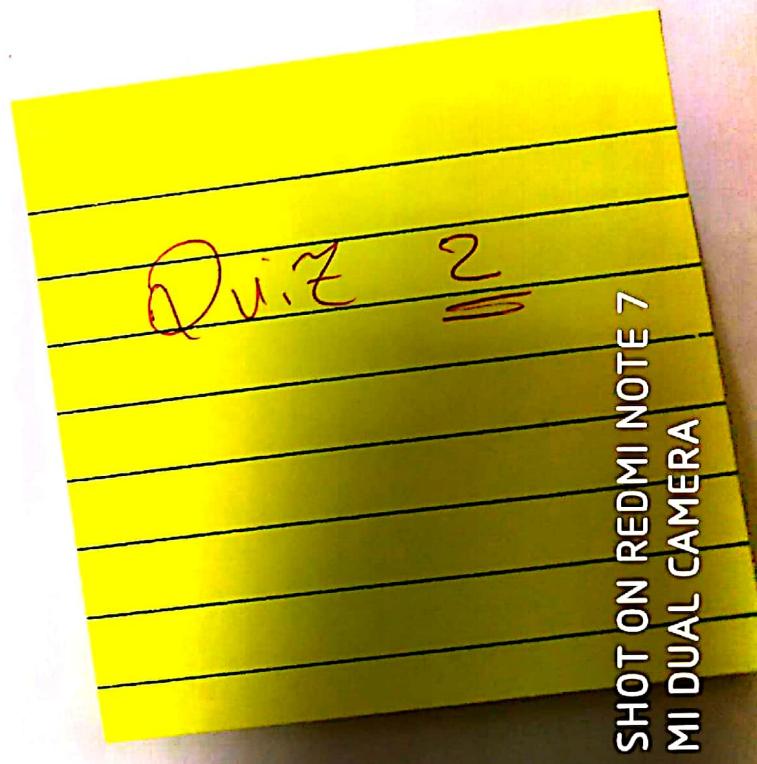
Examine

Fatma Elfouly

Page 1/1

Total Marks

(6)

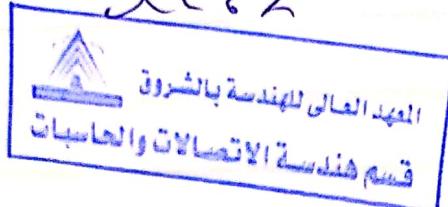


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MI DUAL CAMERA**

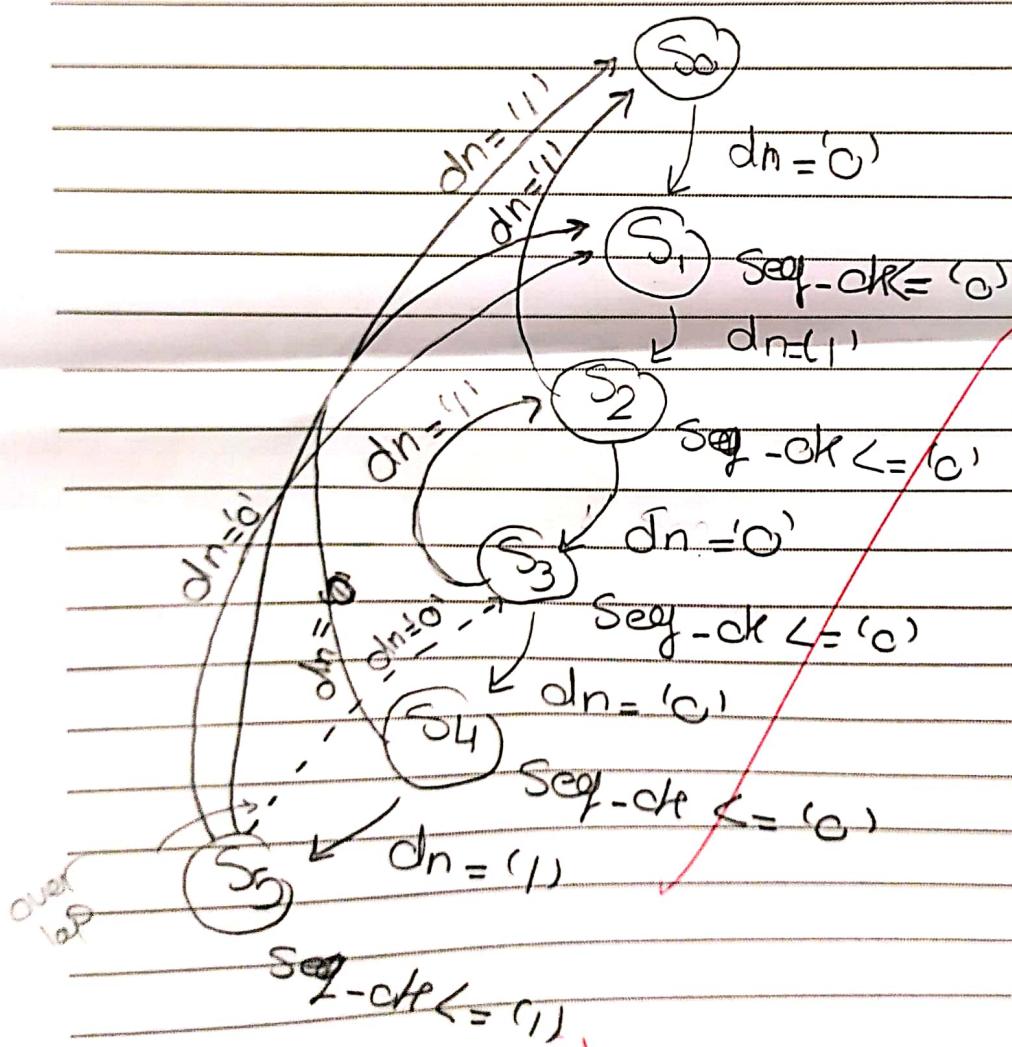
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الدرجة

Sec 2



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Shorouk City
Course Name : Electronic Circuits Design using computer
Course Code : ECE 312
Date of Exam : 28/3/2019



2nd

Academic Year
2018/2019

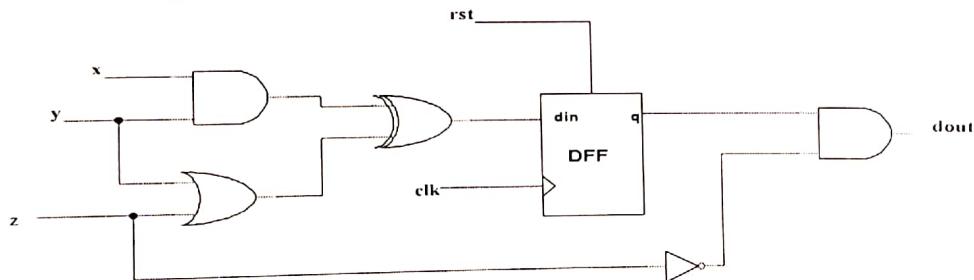
Time Allowed : (1.15) Hours

Level: 3rd year

Department : Communication and Computer Eng.

Answer the Following

Q1	Intended Learning Outcomes (ILOS)			Marks (3)
	Knowledge & Understanding (k1,k2,k3)	Intellectual Skills ()	Practical Skills ()	
	a) VHDL divides the description of a module into an Entity and an Architecture section, what is the purpose of each of these two sections? b) What is the difference between STD_LOGIC type and BIT type? c) What is the FPGA?			
Q2	Intended Learning Outcomes (ILOS)			Marks (5)
	Knowledge & Understanding (k2,k3)	Intellectual Skills (i2)	Practical Skills (p2)	
	Write A VHDL code for the following circuit			



Q3	Intended Learning Outcomes (ILOS)			Marks (4)
	Knowledge & Understanding (k2,k3)	Intellectual Skills (i2)	Practical Skills (p2)	
	There are some errors in the following VHDL code. Find the errors and correct these errors.			
	library ieee; use ieee.std_logic_1164.all; use ieee.std_logic_arith.all; entity mux4_1 port (sel: in std_logic_vector (0 down to 1); a, b, c, d: in std_logic; y: out std_logic end entity mux4_1; architecture rtl of mux4_1 is with sel select y <= a when "00", b when "01", c when "10", d when "11", end architecture rtl;			

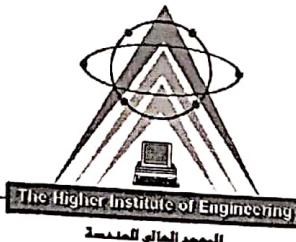
There are some errors in the following VHDL code. Find the errors and correct these errors.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
entity mux4_1
port (sel: in std_logic_vector (0 down to 1);
a, b, c, d: in std_logic;
y: out std_logic
end entity mux4_1;
architecture rtl of mux4_1 is
with sel select
y <= a when "00",
b when "01",
c when "10",
d when "11",
end architecture rtl;
```

Examiner :Dr. Fatma Elfouly

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Total Marks
(12)



Model Answer

Answer of Q1

- a) The Entity section specifies the name of the entity as well as the names and types of its input and output ports. The Architecture section specifies the name of this architecture for a specific entity and then contains either a structural or behavioral description of the entity. Essentially, the Entity section specifies the interface to the entity and the Architecture section specifies the functionality or composition of the entity.
- b) VHDL uses the STD_LOGIC type to model represent logic values. It includes not only values of 0 and 1, but also Z, U, X, -, L, W, and H which are needed for some designs. While the BIT type includes the values of 0 and 1 only which is practically unsuitable.
- c) A field programmable gate array (FPGA) is an integrated circuit that can be programmed or reprogrammed to the required functionality or application in the field after manufacturing.

Answer of Q2

```

library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
entity circuit_1 is
port (x,y,z,clk,rst: in std_logic;
dout: out std_logic);
end entity circuit_1;
architecture rtl of circuit_1 is
signal q :std_logic;
begin
process (clk,rst)
variable n,m,din :std_logic;
begin
if (rst = '1')then
q <= '0';
elsif (rising_edge(clk)) then
n := x AND y;
m := y OR z;
din := n XOR m;
q <= din;
end if;
end process;

```

```
    d_out <= (NOT z) AND q;  
end architecture rtl;
```

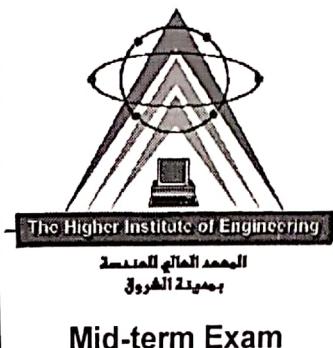
Answer of Q3

```
library ieee;  
use ieee.std_logic_1164.all;  
use ieee.std_logic_arith.all;  
entity mux4_1 is  
port (sel: in std_logic_vector (1 downto 0);  
a, b, c, d: in std_logic;  
y: out std_logic);  
end entity mux4_1;  
architecture rtl of mux4_1 is  
begin  
with sel select  
y <= a when "00",  
b when "01",  
c when "10",  
d when others;  
end architecture rtl;
```

```
avut <= (NOT z) AND q;  
end architecture rtl;
```

Answer of Q3

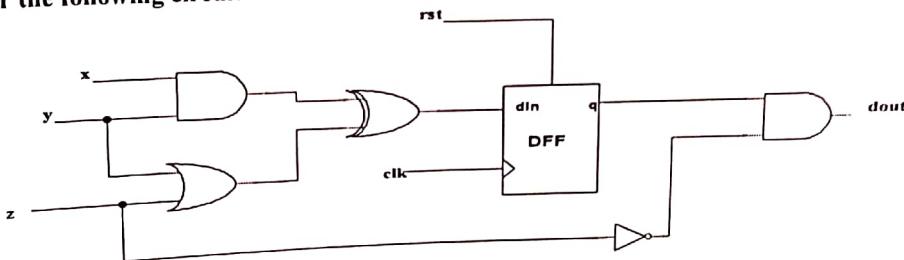
```
library ieee;  
use ieee.std_logic_1164.all;  
use ieee.std_logic_arith.all;  
entity mux4_1 is  
port (sel: in std_logic_vector (1 downto 0);  
a, b, c, d: in std_logic;  
y: out std_logic);  
end entity mux4_1;  
architecture rtl of mux4_1 is  
begin  
with sel select  
y <= a when "00",  
b when "01",  
c when "10",  
d when others;  
end architecture rtl;
```



Answer the Following

Q1	Intended Learning Outcomes (ILOS)			Marks (3)
	Knowledge & Understanding	Intellectual Skills	Practical Skills	
	(k1,k2,k3)	(i1)	(p1)	
a) VHDL divides the description of a module into an Entity and an Architecture section, what is the purpose of each of these two sections? b) What is the difference between STD_LOGIC type and BIT type? c) What is the FPGA?				
Q2	Intended Learning Outcomes (ILOS)			Marks (5)
	Knowledge & Understanding	Intellectual Skills	Practical Skills	
	(k2,k3)	(i2)	(p2)	

Write A VHDL code for the following circuit



Q3	Intended Learning Outcomes (ILOS)			Marks (4)
	Knowledge & Understanding	Intellectual Skills	Practical Skills	
	(k2,k3)	(i2)	(p2)	
There are some errors in the following VHDL code. Find the errors and correct these errors.				

```

library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
entity mux4_1
port (sel: in std_logic_vector (0 down to 1);
      a, b, c, d: in std_logic;
      y: out std_logic
      );
end entity mux4_1;
architecture rtl of mux4_1 is
begin
  sel select
    y <= a when "00",
    b when "01",
    c when "10",
    d when "11";
end architecture rtl;
  
```

Marker :Dr. Fatma Elfouly

The Higher Institute of
Engineering

Shorouk City

Course Name : Electronic Circuits
Design using computer

Course Code : ECE 312

Mid-term model answer



2nd

Semester
Academic Year
2018/2019

Level: 3rd year

Department : Communication
and Computer Eng.

Model Answer

Answer of Q1

- a) The Entity section specifies the name of the entity as well as the names and types of its input and output ports. The Architecture section specifies the name of this architecture for a specific entity and then contains either a structural or behavioral description of the entity. Essentially, the Entity section specifies the interface to the entity and the Architecture section specifies the functionality or composition of the entity.
- b) VHDL uses the STD_LOGIC type to model represent logic values. It includes not only values of 0 and 1, but also Z, U, X, -, L, W, and H which are needed for some designs. While the BIT type includes the values of 0 and 1 only which is practically unsuitable.
- c) A field programmable gate array (FPGA) is an integrated circuit that can be programmed or reprogrammed to the required functionality or application in the field after manufacturing.

Answer of Q2

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
entity circuit_1 is
port (x,y,z,clk,rst: in std_logic;
dout: out std_logic);
end entity circuit_1;
architecture rtl of circuit_1 is
signal q :std_logic;
begin
process (clk,rst)
variable n,m,din :std_logic;
begin
if (rst = '1')then
q <= '0';
elsif (rising_edge(clk)) then
n := x AND y;
m := y OR z;
din := n XOR m;
q <= din;
end if;
end process;
```

```
dout <= (NOT z) AND q;  
end architecture rtl;
```

Answer of Q3

```
library ieee;  
use ieee.std_logic_1164.all;  
use ieee.std_logic_arith.all;  
entity mux4_1 is  
port (sel: in std_logic_vector (1 downto 0);  
a, b, c, d: in std_logic;  
y: out std_logic);  
end entity mux4_1;  
architecture rtl of mux4_1 is  
begin  
with sel select  
y <= a when "00",  
b when "01",  
c when "10",  
d when others;  
end architecture rtl;
```

SHOT ON REDMI NOTE 7
MI DUAL CAMERA

Questions Bank

- 1- Define the following:
 - a- FPGA.
 - b- VHDL
- 2- Describe the FPGA design process using CAD tools
- 3- Define the following:
 - a- PLD
 - b- SPLD
 - c- CPLD
- 4- Define the types of PLD.
- 5- Explain the difference between the CPLD and FPGA.
- 6- Explain the difference between the VHDL language and java language.
- 7- State the advantages of digital circuit design using PLD over digital circuit design using fixed logic device like 74xx-series.
- 8- Illustrate the fundamental VHDL units.
- 9- Explain the difference between the VHDL language and C language.
- 10- Define the CAD tools.
- 11- Illustrate the main components of FPGA chip.
- 12- What is the main advantage of FPGA over microcontroller of PLC.
- 13- Illustrate the assignment statements of VHDL language.
- 14- What is the difference between function simulation and timing simulation?
- 15- What is the difference between asynchronous reset and synchronous reset signal?
- 16- Write a legal VHDL code to describe NAND gate.
- 17- Write a legal VHDL code to describe AND gate.
- 18- Write a legal VHDL code to describe OR gate.
- 19- Write a legal VHDL code to describe XOR gate.
- 20- Write a legal VHDL code to describe XNOR gate.
- 21- Write a legal VHDL code to describe 2-1 multiplexer circuit. Each input signal has 4 bits.
- 22- Write a legal VHDL code to describe 2-1 multiplexer circuit. Each input signal has 2 bits.
- 23- Write a legal VHDL code to describe 2-1 multiplexer circuit. Each input signal has 1 bit.
- 24- Write a legal VHDL code to describe 2-1 multiplexer circuit. Each input signal has 8 bits.

- 25- Write a legal VHDL code to describe 4-1 multiplexer circuit. Each input signal has 4 bits.
- 26- Write a legal VHDL code to describe 4-1 multiplexer circuit. Each input signal has 2 bits.
- 27- Write a legal VHDL code to describe 4-1 multiplexer circuit. Each input signal has 1 bit.
- 28- Write a legal VHDL code to describe 4-1 multiplexer circuit. Each input signal has 8 bits.
- 29- Write a legal VHDL code to describe 8-1 multiplexer circuit. Each input signal has 4 bits.
- 30- Write a legal VHDL code to describe 8-1 multiplexer circuit. Each input signal has 2 bits.
- 31- Write a legal VHDL code to describe 8-1 multiplexer circuit. Each input signal has 1 bit.
- 32- Write a legal VHDL code to describe 8-1 multiplexer circuit. Each input signal has 8 bits.
- 33- Write a legal VHDL code to describe 2 to 4 decoder.
- 34- Write a legal VHDL code to describe 3 to 8 decoder.
- 35- Write a legal VHDL code to describe 3 to 8 decoder using 2 to 4 decoder.
- 36- Write a legal VHDL code to describe Latch, D Flip-Flop.
- 37- Write a legal VHDL code to describe 8 bit parallel register.
- 38- Write a legal VHDL code to describe a shift right register with one bit. Data input signal has 8 bits.
- 39- Write a legal VHDL code to describe a shift right register with two bit. Data input signal has 8 bits.
- 40- Write a legal VHDL code to describe a shift right register with three bit. Data input signal has 8 bits.
- 41- Write a legal VHDL code to describe a shift right register with four bit. Data input signal has 8 bits.
- 42- Write a legal VHDL code to describe a shift left register with one bit. Data input signal has 8 bits.
- 43- Write a legal VHDL code to describe a shift left register with two bit. Data input signal has 8 bits.
- 44- Write a legal VHDL code to describe a shift left register with three bit. Data input signal has 8 bits.
- 45- Write a legal VHDL code to describe a shift left register with four bit. Data input signal has 8 bits.
- 46- Write a legal VHDL code to describe a shift right and shift left register with one bit. Data input signal has 8 bits.
- 47- Write a legal VHDL code to describe 2 bit up counter.
- 48- Write a legal VHDL code to describe 4 bit up counter.

- 49- Write a legal VHDL code to describe 2 bit down counter.
- 50- Write a legal VHDL code to describe 4 bit down counter.
- 51- Write a legal VHDL code to describe 2 bit up-down counter.
- 52- Write a legal VHDL code to describe 4 bit up-down counter.
- 53- Write a legal VHDL code to describe half adder and full adder circuits
- 54- Write a legal VHDL code to describe half subtractor and full subtractor.
- 55- Write a legal VHDL code to describe adder/subtractor circuit (assume, 2-inputs x and y each one have 4-bits).
- 56- Write a legal VHDL code to describe parallel adder circuit (assume, 2-inputs x and y each one have 4-bits).
- 57- Write a legal VHDL code to describe parallel subtractor circuit (assume, 2-inputs x and y each one have 4-bits).
- 58- Design a finite state machine FSM needed for a sequence detector to detect the sequence (i.e. "1010") when applied at its input.
- 59- Design a finite state machine FSM needed for a sequence detector to detect the sequence (i.e. "1001") when applied at its input.
- 60- Design a finite state machine FSM needed for a sequence detector to detect the sequence (i.e. "10010") when applied at its input.
- 61- Design a finite state machine FSM needed for a sequence detector to detect the sequence (i.e. "01001") when applied at its input.
- 62- Design a finite state machine FSM needed for a sequence detector to detect the sequence (i.e. "110011") when applied at its input.



El Shorouk Academy

Communications Department

3rd Year

VLSI

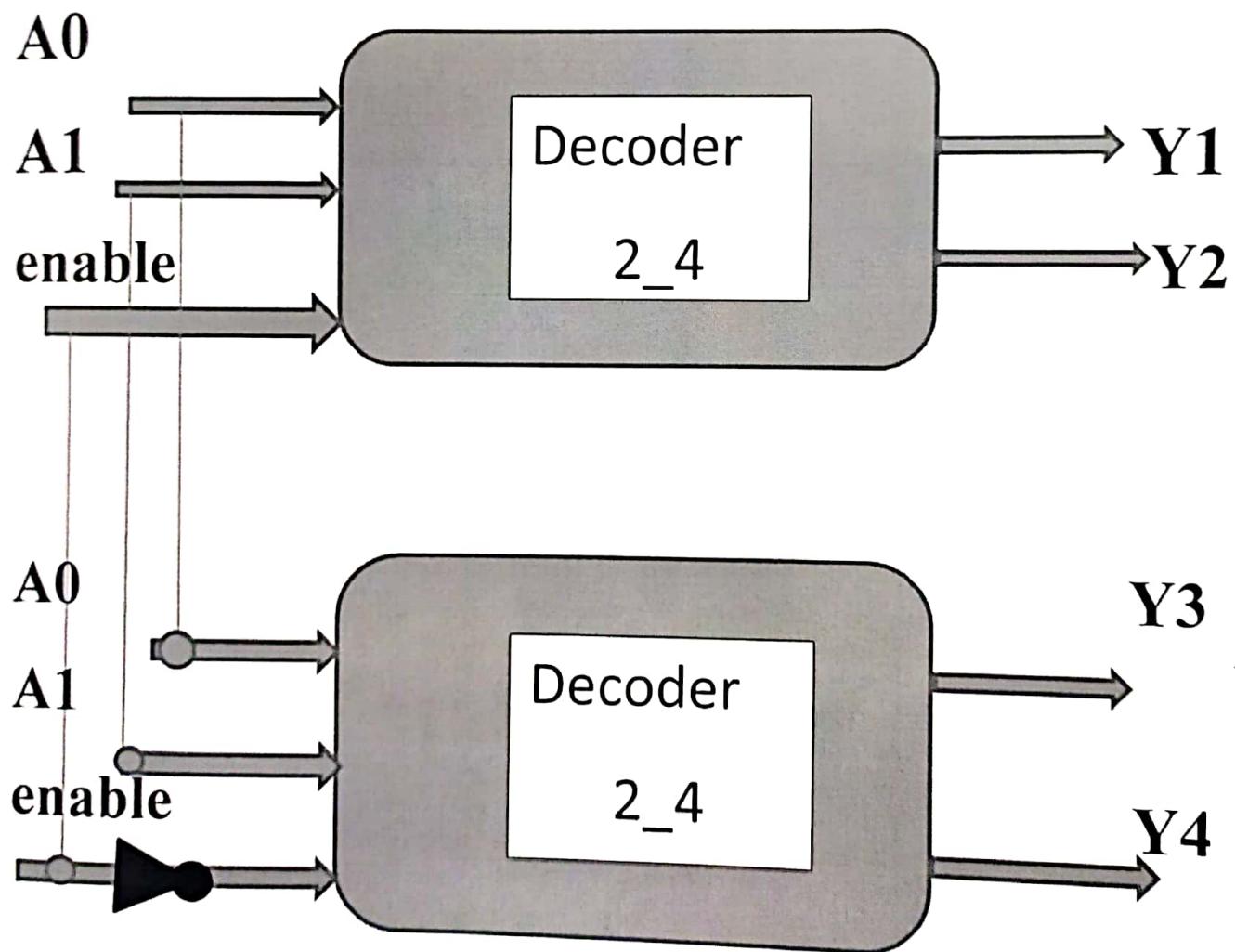
Under Supervision of:

: Fatma Elfouly

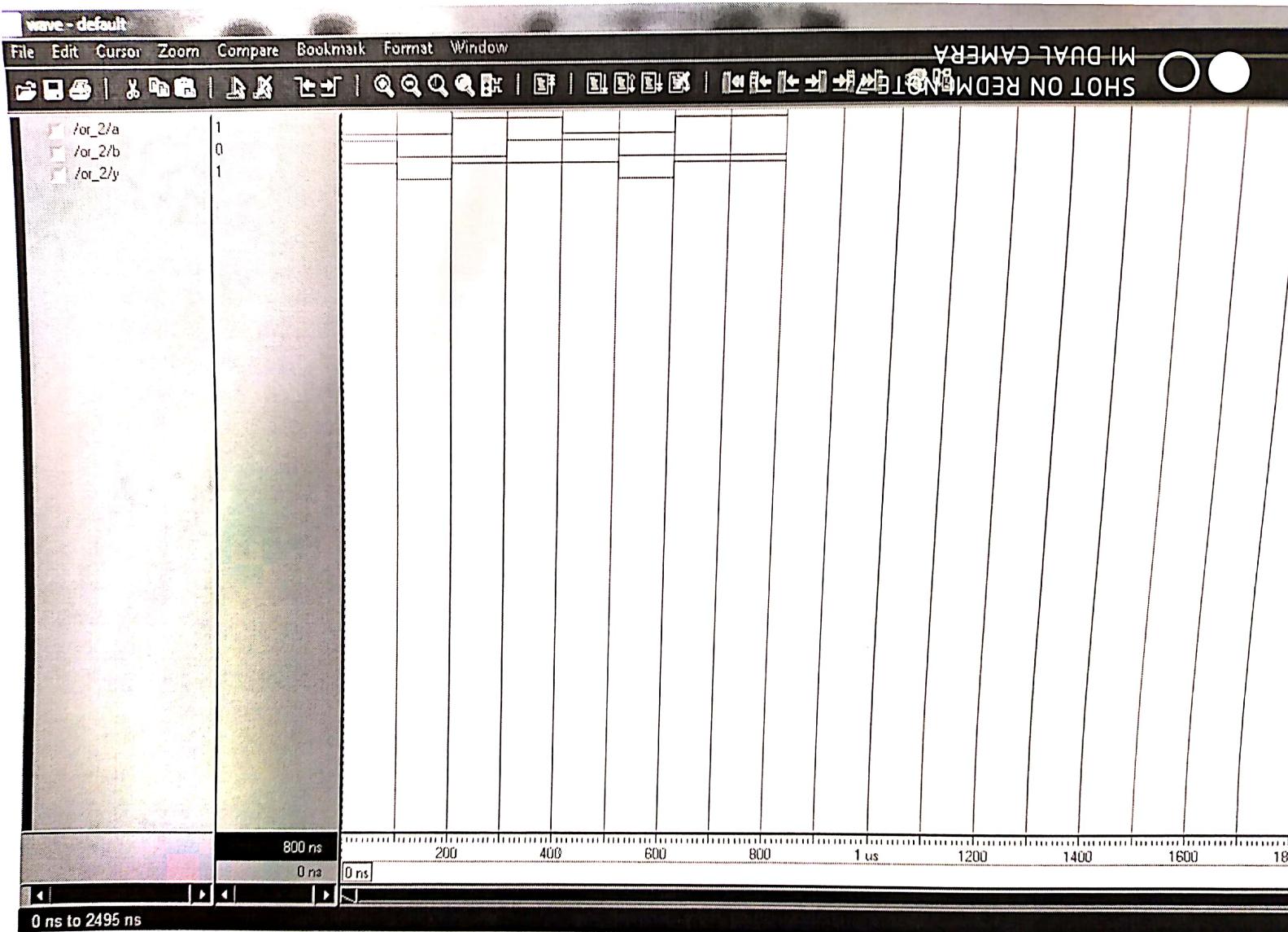
NORAN HATE



Decoder 3 8 by using decoder 2 4:



```
File Edit View Help  
C File New Open Save Print Find Options  
- hds header_start  
-- VHDL Architecture Noran.And_2.rtl  
Created:  
    by - acc_home.UNKNOWN (ACC_HOME-PC)  
    at - 21:34:53 03/30/2019  
Generated by Mentor Graphics' HDL Designer(TM) 2001.5 (Build 170)  
-- hds header_end  
LIBRARY ieee;  
USE ieee.std_logic_1164.all;  
USE ieee.std_logic_arith.all;  
  
ENTITY Or_2 IS  
-- Declarations  
port(a,b: in std_logic;  
     y: out std_logic);  
  
END Or_2 ;  
  
-- hds interface_end  
ARCHITECTURE rtl OF Or_2 IS  
BEGIN  
y<= a or b;  
END rtl;
```



The Higher Institute of
Engineering

Shorouk City

Course Name : Electronic Circuits
Design using computer

Course Code : ECE 312

Date of Exam : 23/4/2019



Final practical Exam
Model (1)

Semester
Academic Year
2018/2019

2nd

Time Allowed : (2) Hours

Level: 3rd year

Department : Communication
and Computer Eng.

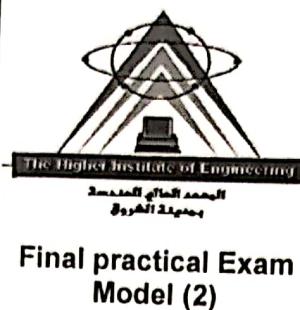
Answer the Following

Q1	Intended Learning Outcomes (ILOS)			Marks (15)
	Knowledge & Understanding	Intellectual Skills	Practical Skills	
	(k1,k2,k3)	(i1,i2)	(p1,p2,p2)	

Design and simulate a legal VHDL code to describe a 8-bit shift register (i.e. shift left with 4-bits and shift right with 2-bit).

Examiner :Dr. Fatma Elfouly	Page 1/1	Total Marks (15)
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The Higher Institute of Engineering
Shorouk City
Course Name : Electronic Circuits Design using computer
Course Code : ECE 312
Date of Exam : 23/4/2019



2nd	Semester Academic Year 2018/2019
	Time Allowed : (2) Hours
	Level: 3rd year
	Department : Communication and Computer Eng.

Answer the Following

Q1	Intended Learning Outcomes (ILOS)			Marks (15)
	Knowledge & Understanding (k1,k2,k3)	Intellectual Skills (i1,i2)	Practical Skills (p1,p2,p2)	

Design and simulate a legal VHDL code to describe a counter circuit that counts the numbers from 0 to 9.

Examiner :Dr. Fatma Elfouly	Page 1/1	Total Marks
		(15)

The Higher Institute of
Engineering

Shorouk City

Course Name : Electronic Circuits
Design using computer

Course Code : ECE 312

Date of Exam : 23/4/2019



Final practical Exam
Model (3)

Semester
Academic Year
2018/2019

2nd

Time Allowed : (2) Hours

Level: 3rd year

Department : Communication
and Computer Eng.

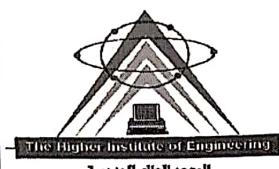
Answer the Following

Q1	Intended Learning Outcomes (ILOS)			Marks (15)
	Knowledge & Understanding	Intellectual Skills	Practical Skills	
	(k1,k2,k3)	(i1,i2)	(p1,p2,p2)	

Design and simulate a legal VHDL code to describe a counter circuit that counts the numbers from 1 to 11.

Examiner :Dr. Fatma Elfouly	Page 1/1	Total Marks (15)
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**The Higher Institute of
Engineering**
Shorouk City
Course Name : Electronic Circuits
Design using computer
Course Code : ECE 312
Date of Exam : 23/4/2019



**Final practical Exam
Model (4)**

**Semester
Academic Year
2018/2019**

Time Allowed : (2) Hours

Level: 3rd year

**Department : Communication
and Computer Eng.**

Answer the Following

Q1	Intended Learning Outcomes (ILOs)			Marks (15)
	Knowledge & Understanding (k1,k2,k3)	Intellectual Skills (i1,i2)	Practical Skills (p1,p2,p2)	

Design and simulate a legal VHDL code to describe a 8-bit rotate register (i.e. shift left with 4-bits)

Examiner :Dr. Fatma Elfouly	Page 1/1	Total Marks (15)
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El Shorouk Academy

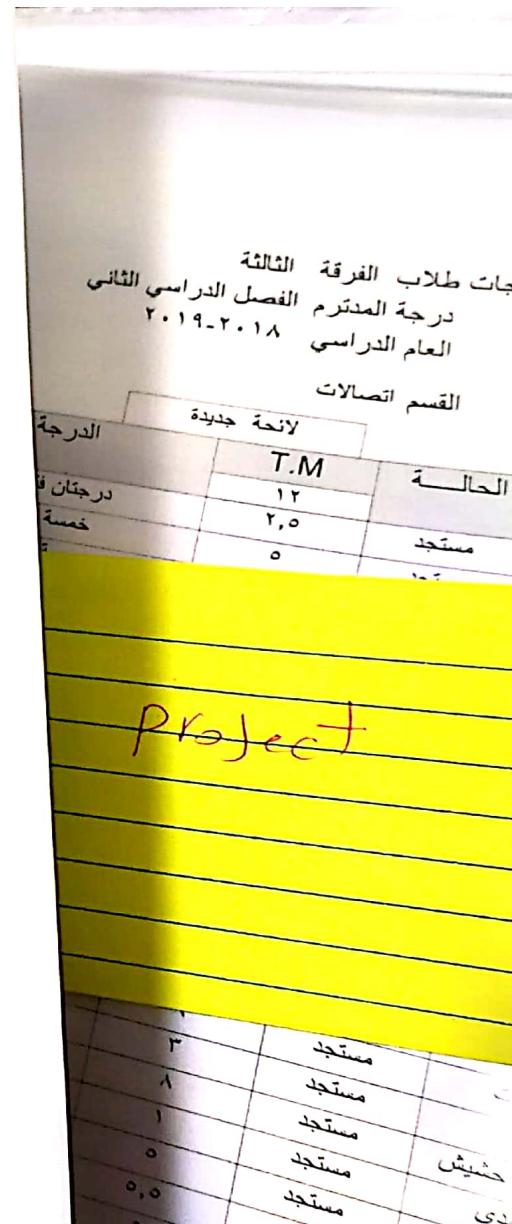
The Higher Institute of Engineering

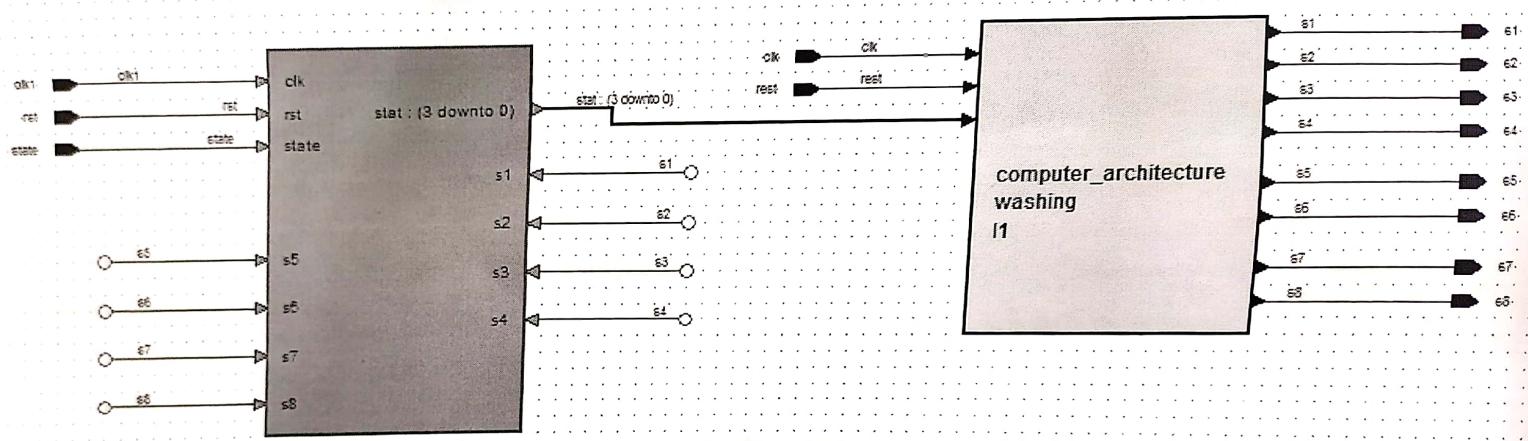
**Communications and Electronics
Engineering Department**

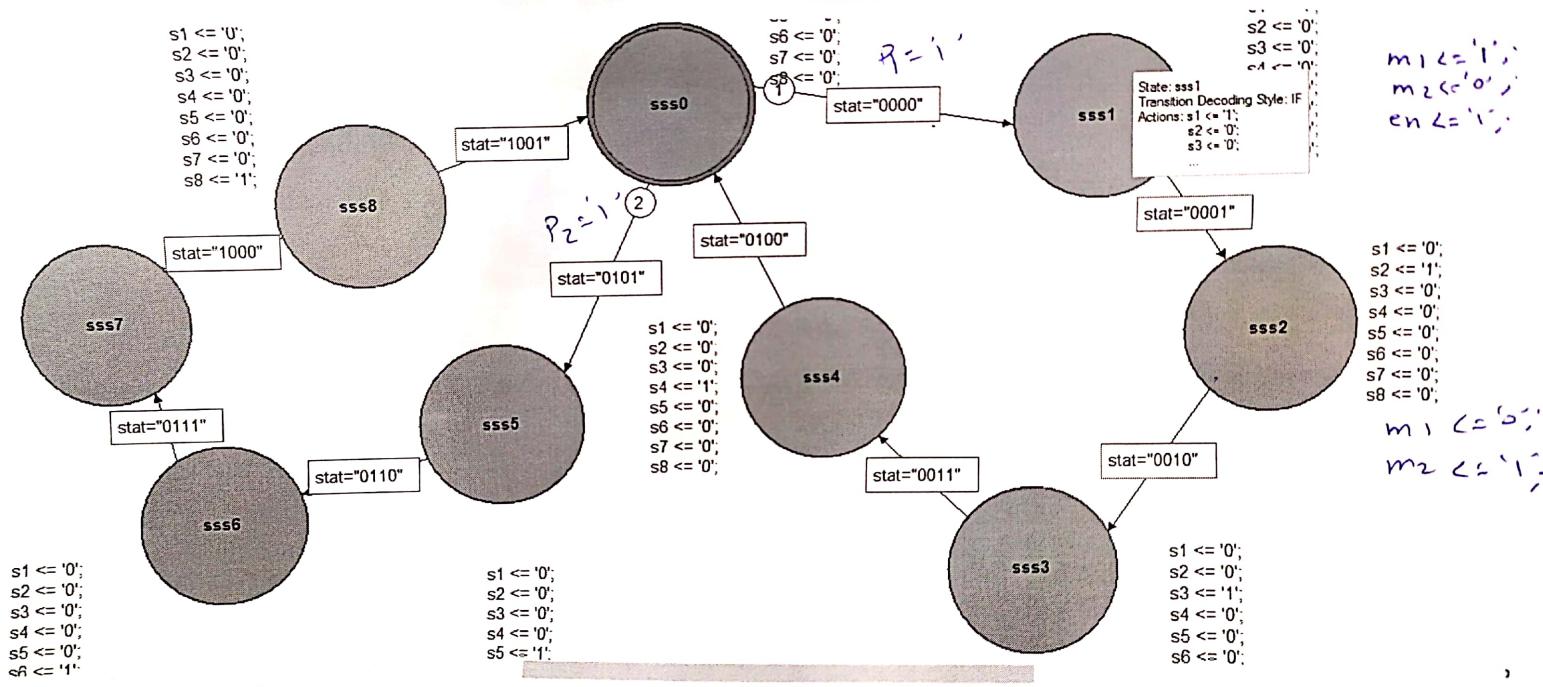
3rd Year

VSLI

DR/Fatma El-Fouly







```

ENTITY count IS
-- Declarations
port(clk,rst,state: in std_logic;
s1,s2,s3,s4,s5,s6,s7,s8 : in std_logic;
stat : out std_logic_vector(3 downto 0));
--count_out: out std_logic_vector(3 downto 0));
END count;

ARCHITECTURE rtl OF count IS
signal count_temp: unsigned (3 downto 0);
signal count      : unsigned (2 downto 0);
--signal en :std_logic_vector (2 downto 0);
BEGIN
process (rst,clk)
begin
if (rst='1') then
count_temp <=(others=> '0');
count      <=(others=> '0');
elsif (rising_edge (clk)) then
if ((state ='0') and (count = 0) ) then
stat <="0000";
count <= count+1;
elsif (s1 = '1') then
count_temp <= count_temp+1;
if (count_temp = 12)then
stat <="0001";
count_temp <= (others=>'0');
count <= count+1;
end if;
elsif(s2 = '1')then

```

```
count_temp <= count_temp+1;
if (count_temp = 4)then
stat <="0010";

count_temp <= (others=>'0');
count <= count+1;
end if;

elsif(s3 = '1')then
count_temp <= count_temp+1;
if (count_temp = 9)then
count_temp <= (others=>'0');
count <= count+1;
stat <="0011";
end if;

elsif(s4 = '1')then
count_temp <= count_temp+1;
if (count_temp = 9)then
count_temp <= (others=>'0');
count <= (others=> '0');
stat <="0100";
end if;

elsif ((state ='1') and (count = 0) ) then
stat <="0101";
count <= count+1;
elsif (s5 = '1') then
count_temp <= count_temp+1;
if (count_temp = 6)then
count_temp <= (others=>'0');
count <= count+1;
stat <="0110";
```

```
end if;

elsif(s6 = '1')then

count_temp <= count_temp+1;
if (count_temp = 5)then
count_temp <= (others=>'0');
count <= count+1;
stat <="0111";
end if;

elsif(s7 = '1')then

count_temp <= count_temp+1;
if (count_temp = 4)then
count_temp <= (others=>'0');
count <= count+1;
stat <="1000";
end if;

elsif(s8 = '1')then

count_temp <= count_temp+1;
if (count_temp = 3)then
count_temp <= (others=>'0');
count <= (others=> '0');
stat <="1001";
end if;
end if;
end if;
end process;

END rtl;
```

The Higher Institute of Engineering
Shorouk City
Course Name : Electronic Circuits Design using computer
Course Code : ECE 312
Date of Exam : 16/5/2019



2 nd	Semester Academic Year 2018/2019
Time Allowed : (2) Hours	
Level: 3 rd year	
Department : Communication and Computer Eng.	

Answer the Following

Q1	Intended Learning Outcomes (ILOS)			Marks (20)
	Knowledge & Understanding	Intellectual Skills	Practical Skills	
	(k1,k2)	()	()	

- A) A coca machine is to be designed so that the user must insert 3 pounds in coins to active the machine. The machine has single coin slot for one pounds P and half pounds H and returns no change. Using the basic design approach, design a FSM for this machine taking into account all possible input combinations.
 B) Design the finite state machine FSM needed for a sequence detector to detect the sequence (i.e. "001100") when applied at its input in overlapping and non-overlapping modes.

Q2	Intended Learning Outcomes (ILOS)			Marks (10)
	Knowledge & Understanding	Intellectual Skills	Practical Skills	
	(k1,k2,k3)	(i2)	(p2)	

Write a legal VHDL code for a 10 seconds stopwatch timer. The clock frequency is 2 Hz.

Q3	Intended Learning Outcomes (ILOS)			Marks (10)
	Knowledge & Understanding	Intellectual Skills	Practical Skills	
	(k1,k2,k3)	(i2)	(p2)	

- A) Write a legal VHDL code to describe a 8-bit shift register (i.e. shift left with 3-bits and shift right with 1-bit).
 B) Write a legal VHDL code to describe a 3-8 decoder.

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The Higher Institute of
 Engineering
 Shorouk City
 Course Name : Electronic Circuits
 Design using computer
 Course Code : ECE 312
 Final exam model answer

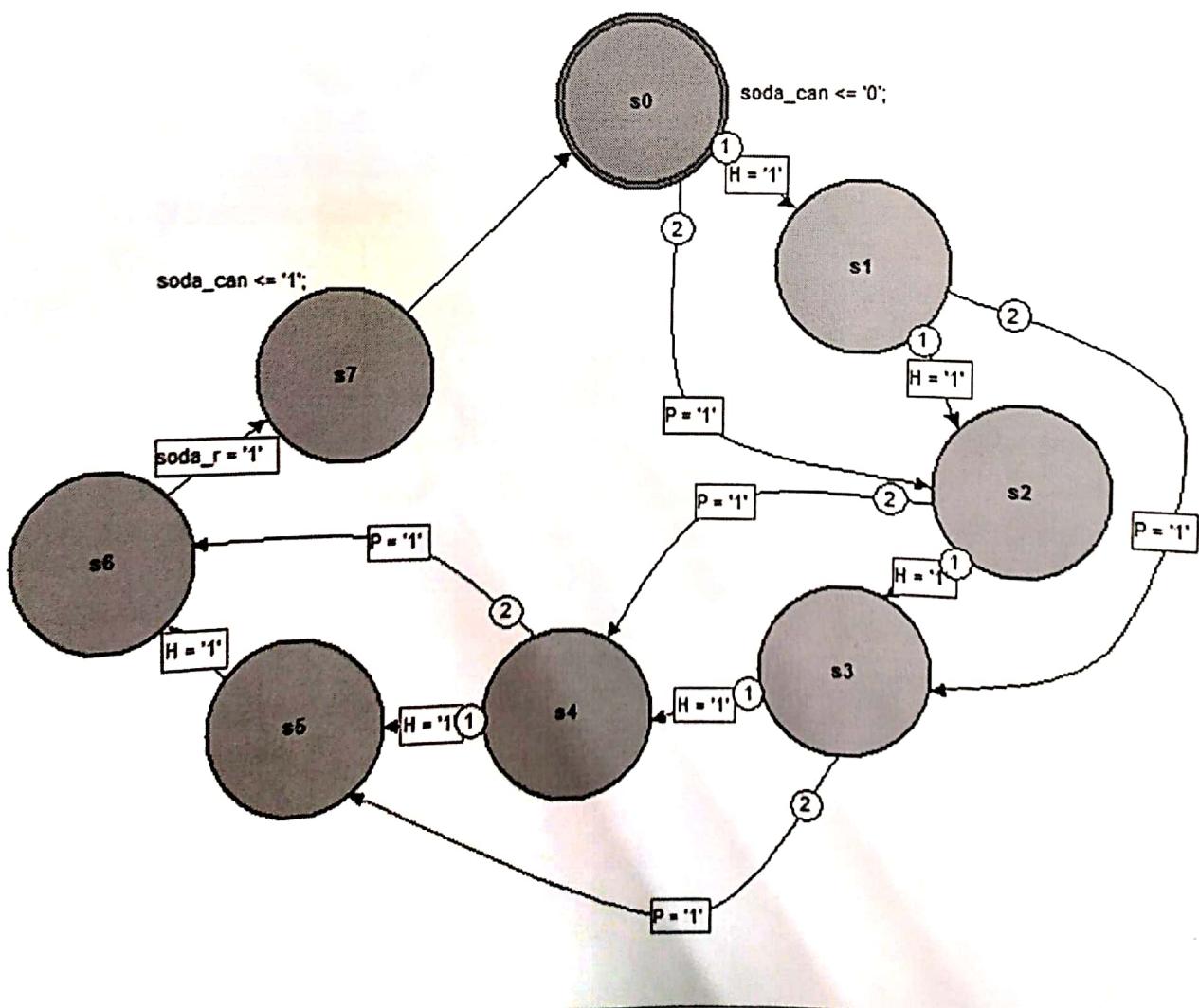


2 nd	Semester Academic Year 2018/2019
Level: 3 rd year	
Department : Communication and Computer Eng.	

Model Answer

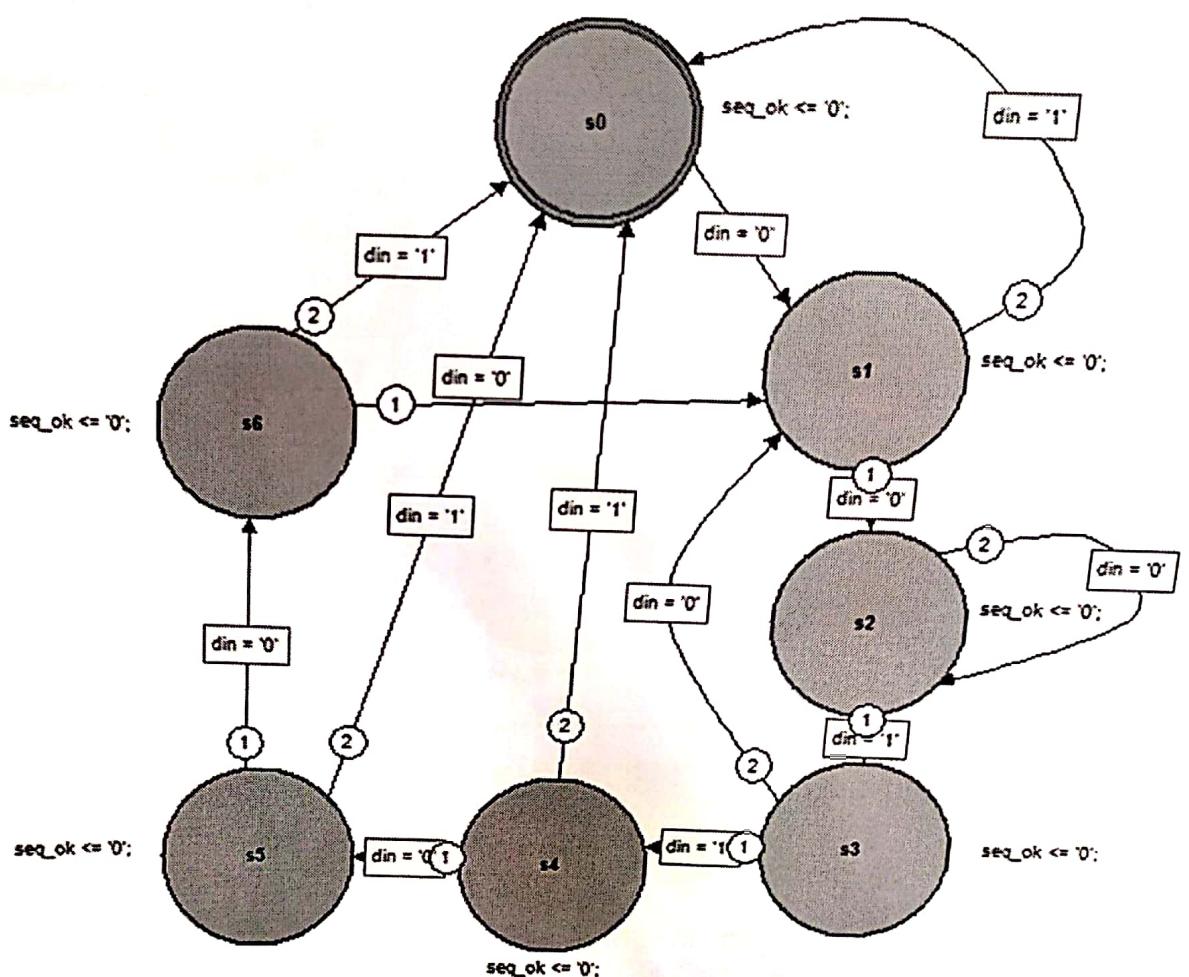
Answer of Q1

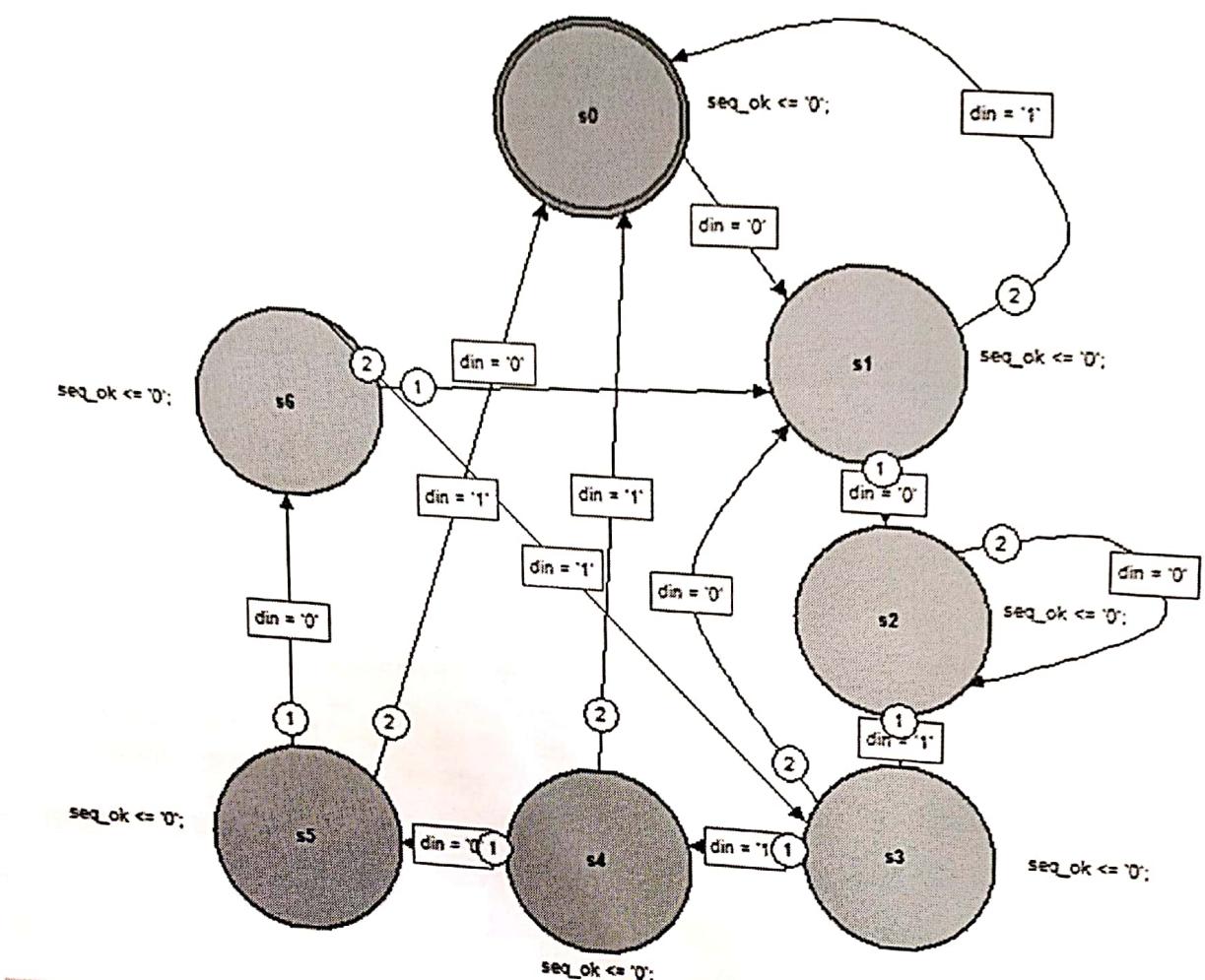
A)



B)

Without overlap:



With overlap:**Answer of Q2**

```

library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

ENTITY timer IS
port(clk,start,rst: in std_logic;
count: out std_logic_vector(4 downto 0));
END timer ;
ARCHITECTURE rtl OF timer IS
signal count_sig: unsigned (4 downto 0);
BEGIN
process (rst,clk)
begin
if (rst='1') then
count_sig <=(others=> '0');
elsif (rising_edge (clk)) then
if (start='1') then
count_sig <= count_sig+1;
if (count sig=19) then
  
```

```
count_sig <= "00000";
end if;
end if;
end process;
count <= std_logic_vector(count_sig);
END rtl;
```

Answer of Q3

A)

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
entity reg_par_shift is
port (clk, rst: in std_logic;
load :in std_logic_vector(1 downto 0);
reg_in: in std_logic_vector(1 downto 0);
reg_out: out std_logic_vector(7 downto 0));
end entity reg_par_shift;
architecture rtl of reg_par_shift is
signal reg_temp: std_logic_vector(7 downto 0);
begin
process (rst, clk)
begin
if (rst = '1') then
reg_temp <= (others => '0');
elsif (rising_edge(clk)) then
if (load = "00") then
reg_temp <= reg_in;
elsif (load = "01") then
reg_temp <= "reg_temp(4 downto 0)&"000";
else
reg_temp <= '0' & reg_temp(7 downto 1);
end if;
end if;
end process;
reg_out <= reg_temp;
end architecture rtl;
```

B)

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
entity decoder3_8 is
port (a: in std_logic_vector(2 downto 0),
y: out std_logic_vector(7 downto 0));
end entity decoder3_8;
architecture rtl of decoder3_8 is
begin
y <= "00000001" when a = "000" else
"00000010" when a = "001" else
```

```
"00000100" when a = "010" else  
"00001000" when a = "011" else  
"00010000" when a = "100" else  
"00100000" when a = "101" else  
"01000000" when a = "110" else  
"10000000" when a = "111" else  
"00000001";  
end architecture rtl;
```

Dr. Fatma Elfouly

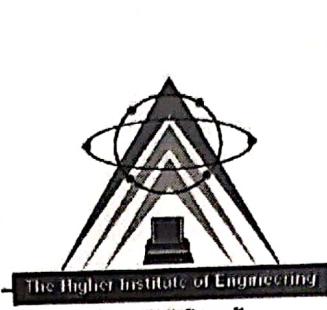
The Higher Institute of
Engineering

Sharouk City

Course Name : Electronic Circuits
Design using computer

Course Code : ECE 312

Date of Exam : 23/5/2018



Final Exam

Semester
Academic Year
2017/2018

2nd

Time Allowed : (2) Hours

Level: 3rd year

Department : Communication
and Computer Eng.

Answer the Following

Intended Learning Outcomes (ILOS)

Q1	Knowledge & Understanding (k1,k2,k3)	Intellectual Skills (i2)	Pr	Mark (15)

Design the finite state machine FSM needed for a sequence detector to detect the sequence (i.e. "101001") when applied at its input in overlapping and non-overlapping modes.

Intended Learning Outcomes (ILOS)

Q2	Knowledge & Understanding (k1,k2,k3)	Intellectual Skills (i2)	Practical Skills (p2)	Marks (15)

Design and simulate a circuit to control a simple traffic light such that:

- a- Assume a 2 Hz clock.
- b- The default state is yellow.
- c- After 13 seconds, the TLC will go to the red state.
- d- Remain 10 seconds in red state.
- e- Then change to the green state and remain for 16 seconds.
- f- Finally return to the yellow state.

Intended Learning Outcomes (ILOS)

Knowledge & Understanding (k1,k2,k3)	Intellectual Skills (i2)	Practical Skills (p2)	Marks (10)

Write a legal VHDL code to describe a 8-bit shift register (i.e. shift right with 3-bits and shift left with 2-bits).

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Total Marks

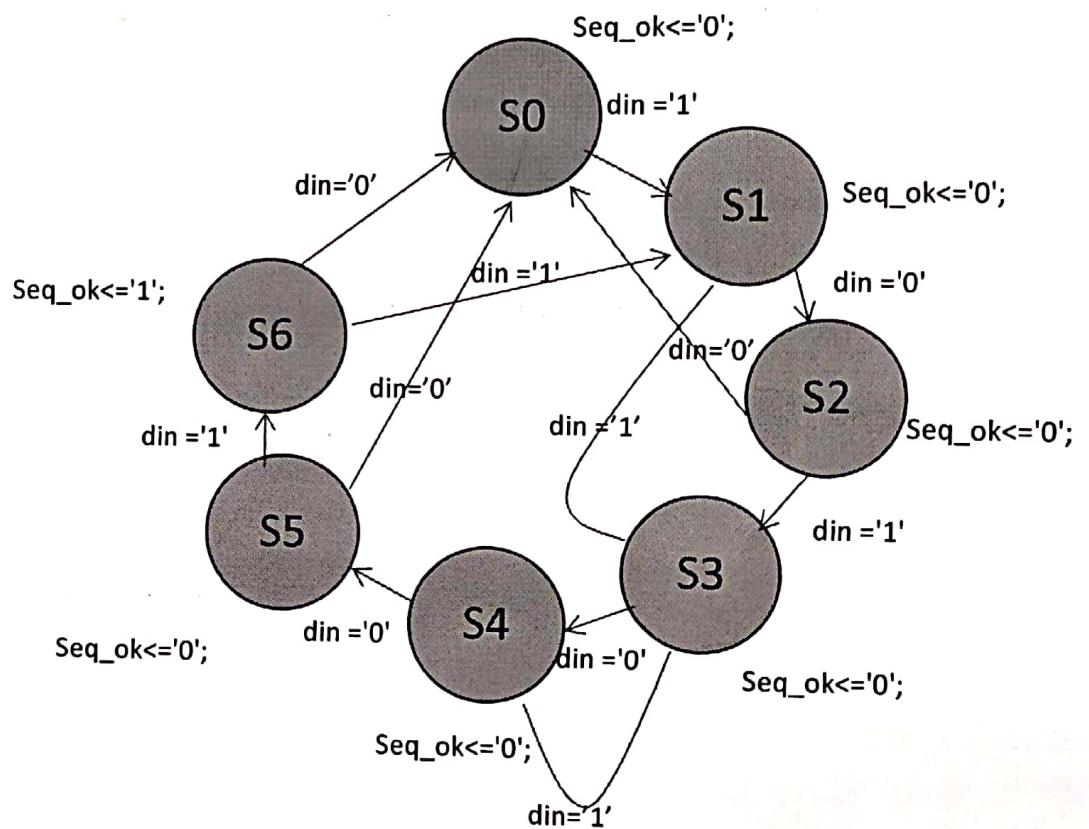
(40)



Model Answer

Answer of Q1

With non-overlapping mode.



```

process (rst,clk)
begin
if (rst='1') then
count_sig<=(others=> '0');
elsif (rising_edge (clk)) then
if (en='1') then
count_sig<= count_sig+1;
if (count_sig = 19) then
count_sig<= (others=>'0');
end if;
end if;
end if;
end process;
q <= '1' when count_sig = 19 else '0';
ENDrtl;

```

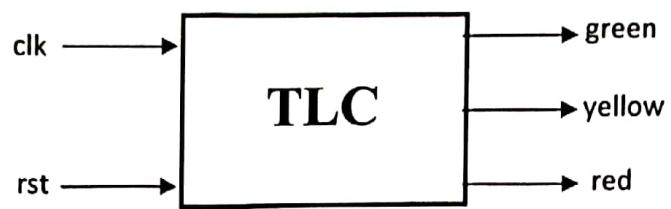
Answer of Q3

```

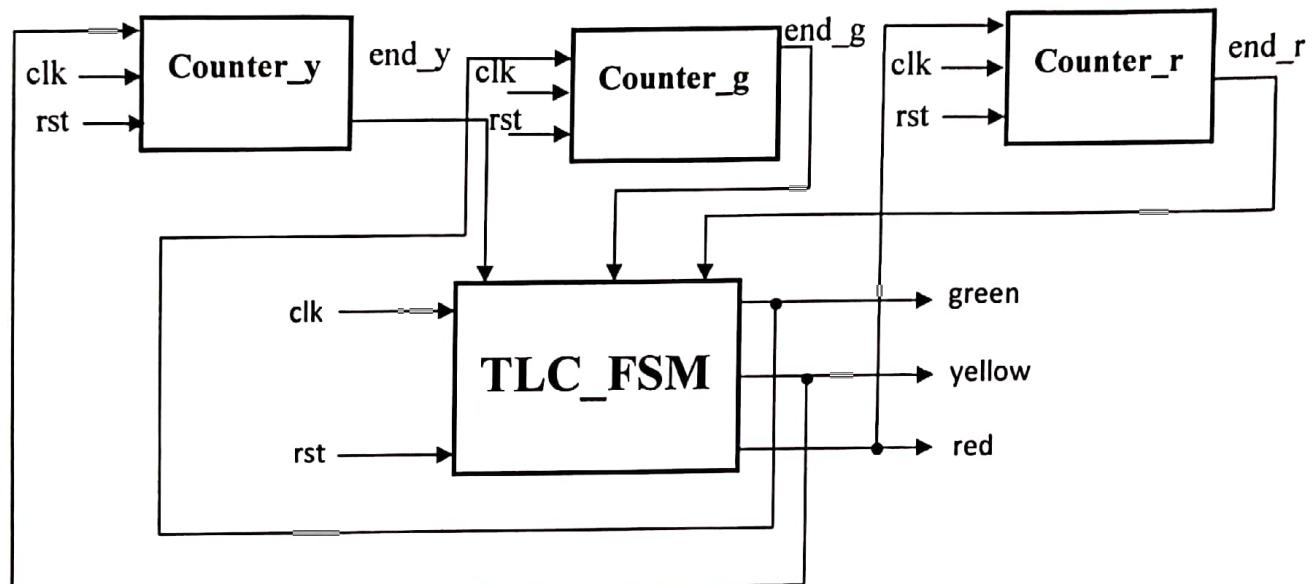
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
entity reg_par_shift is
port (clk, rst: in std_logic;
load :in std_logic_vector(1 downto 0);
reg_in: in std_logic_vector(7 downto 0);
reg_out: out std_logic_vector(7 downto 0));
end entity reg_par_shift;
architecture rtl of reg_par_shift is
signal reg_temp: std_logic_vector(7 downto 0);
begin
shift_control<= shift_left&shift_right;
process (rst, clk)
begin
if (rst = '1') then
reg_temp<= (others => '0');
elsif (rising_edge(clk)) then
if (load = "00") then
reg_temp<= reg_in;
elsif (load = "01") then
reg_temp<= "000"&reg_temp(7 downto 3);
else
reg_temp<= reg_temp(5 downto 0)&"00";
end if;
end if;
end process;
reg_out<= reg_temp;
end architecture rtl;

```

Answer of Q2



(a) Graphical symbol



(b) Block Diagram

Figure 2 Automatic TLC

TLC_FSM:

