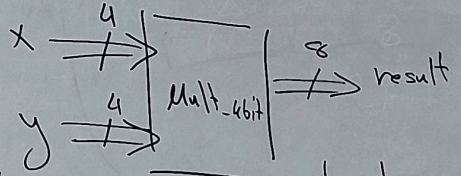
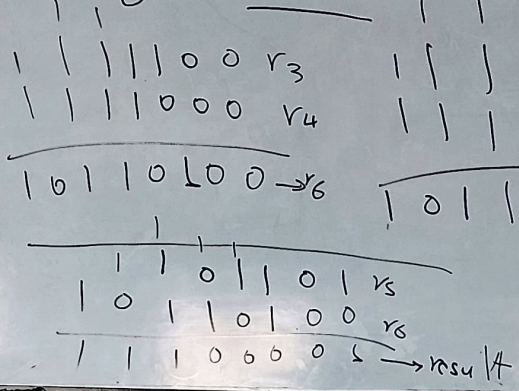
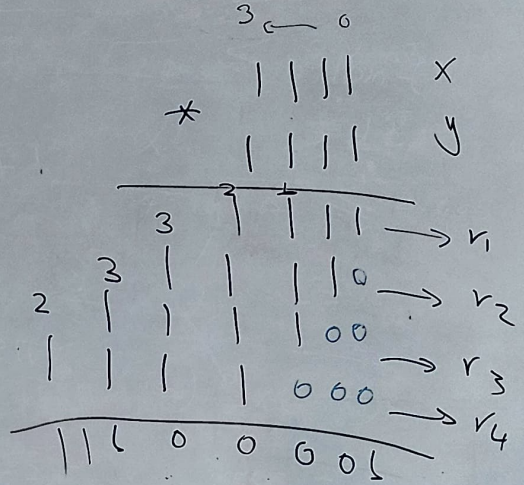
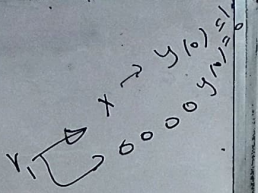
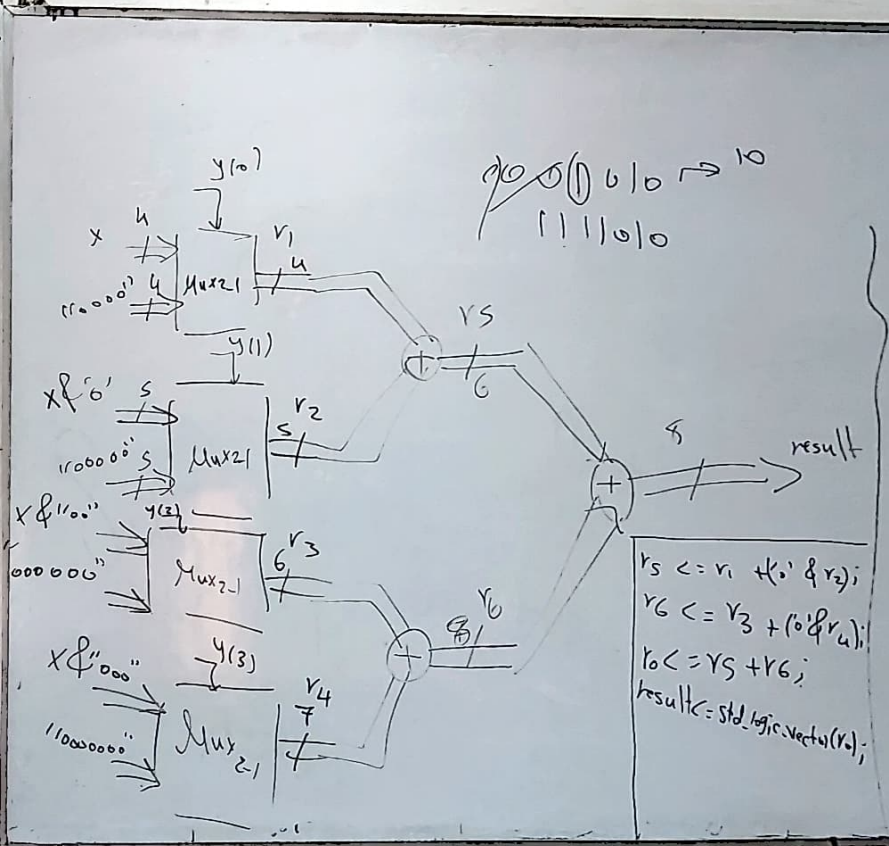
Multiplier


x
y
4
4
Mult_4bit
8
result


r3
r4
r6
r1
r2
r5
r5
r6
result


3
0
x
y
r1
r2
r3
r4


x
y(0)
r1




```
entity Mult_4bit is
Port( x,y  :in std_logic_vector(3 downto 0);
      result : out std_logic_vector(7 downto 0));
end Mult_4bit;
architecture rtl of Mult_4bit is
Signal  r1     : unsigned (3 downto 0);
Signal  r2     : unsigned (4 downto 0);
Signal  r3,r5  : unsigned (5 downto 0);
Signal  r4     : unsigned (6 downto 0);
Signal  r6,r0  : unsigned (7 downto 0);
begin
r1 <=unsigned(x) when y(0) ='1' else (others=>'0');
r2 <=(unsigned(x)&'0') when y(1)='1' else (others=>'0');
r3 <=(unsigned(x)&"00") when y(2)='1' else (others=>'0');
r4 <=(unsigned(x)&"000") when y(3)='1' else (others=>'0');
```