

* What's VHDL ?? \rightarrow VH-SIC

Very high Speed integrated Circuit Hardware Description language.
hardware language مكتبة لغات المكونات

* Difference between Hardware Description Language & Software language

\rightarrow Hardware description language

describe hardware internal form, describe behaviour and structure

\rightarrow Software language

Programme language

* VHDL Basic Code (3 Com Ponants)

1 LIBRARY declarations:

موجود فيها المكتبة التي تستخدم في التصميم
ويعرفها بـ library وتحتوي على وحدات المكونات
وهي قائمة بالمكتبات التي ستستخدم في التصميم

has list of all libraries to be used in The design

Such as: Std, Work, ieee

2. Entity

design entity name or output pins

Specifies The I/O Pins of The Circuit

3. Architecture

descriPe The Function

Function \leftrightarrow قيم

Entity (key word)

Any VHDL has

Entity entity_name is

2 types

1. entity

2. architecture

Port (

Port name : Signal mode Signal type

يُكتب

);

END entity-name;

أمثلة

NOTE:

الامثلية لـ Port (mode , type) هي

1. Signal-mode (mode)

→ in

→ ~~out~~ OUT

→ buffer

لـ حابي العرج وافرد FeedBack دخل

→ inout

Dataflow أو الائين RAM

2 Signal-type (type)

→ bit (1, 0)

→ Std-logic (1, 0, H, L, HL)

الحادي لـ bit واحد

الحادي لـ bus (array) سلك وبروفه هيكاج واحد

From Bits

النوع TYPE

Signal

bus

bit

Std-logic

bit-vector (size)

Std-logicVector (size)

Size = 4bit MSB LSB

3 → 0

* Std-logic Vector (MSB down to LSB) ✓

(or)

* Std-logicVector (LSB to MSB)

Std. logic vector (3 down to 0)

من يكتب على الطريقة التالية

(0 to 3)

على ترتيب لا يدخل من الصياغة اليمن

3 ← 0 1 0 1 (من L to M) حال

0 1 0 1

2. Architecture

Structure (describe the Circuit)

behavior (

RTL (register transfer logic)

include behaviour of Structure

Assignment Statement (VHDL Statement)

1. Concurrent Assignment Statement Parallel الاوامر التي تندى

في نفس الوقت ومهما يزور في المفترض

Simple Signal Assignment

Logic out gates

Selected Signal Assignment

Conditional Signal Assignment

2. Sequential Assignment

if - else

Case Statement

Somenotes

1. في Port لو الحاب (بواحد كل ادخن) ليه نفس x, y
يكتبوا في نفس السطر type و Mood

* 1. Blackbox او ببساطة

2. Function Bentity

3. Code

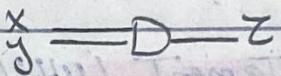
→ (Comment)

→ الاسم الذي يكتبوا بعد entity يكون عادة entity name و ارقام

$x <= \rightarrow$ equal

→ (Inverter) \rightarrow \neg بعكسه \neg logic gate
Note: gate

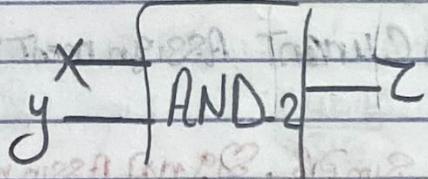
VHDL Code For AND gate



→ Blackbox

→ Function

$$z = x \cdot y$$



Code:

→ entity AND_2 is

Port (x, y : in Std-logic ;

z : out Std-logic);

end ~~entity~~ AND_2;

architecture RTL OF AND_2 IS

begin

z <= x AND y;

end RTL;

else $\xrightarrow{\text{long con}} \text{elseif}$

Concurrent Assignment Statement

1- Simple Signal Assignment : It is used for logic or arithmetic expression

→ Signal-name < - expression
↳ out

ex $y \leftarrow x \text{ AND } z;$

2- Selected Signal Assignment Used to assign one of several values based on selection criterion used with key word.

WITH expression Select

Signal name < - expression When Constant Value;
الرقم القياسي للإشارة

expression

العامه الى قايم عليها

3- Conditional Signal Assignment When ~~but~~ else

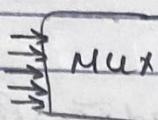
Signalname <= expression When logic expression else expression

out

المراد

البرل

Multiplexer



* دايره لها اكتر من 2ⁿ وله IP واحد

مدين الى حقولي ان INPUT هياو ، OUT الفلافي ؟
نحوال Selector او Control Signal او 2^n ويعطى عالي على OUT والصالح الى طبعاته هوها على ده بيس

Signal type
→ Signal
→ Bus

وكمان رقى Size

BIT Selection كامان تعرف

Control Signal - input عدد مدخلات ملحوظ عدوى

Sel ده عدد ال
Fraction و لو طبقت على $2^n >$ عدد
يبي بقى للإيج

② زى مثال size 3 عنده 3 input تكون هو هو ال size

① MUX 4-1

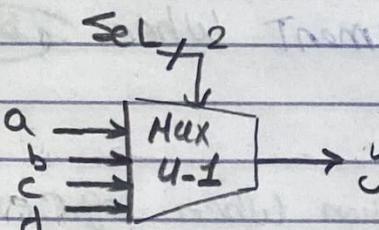
* Input Signal

* Sel \rightarrow Bus

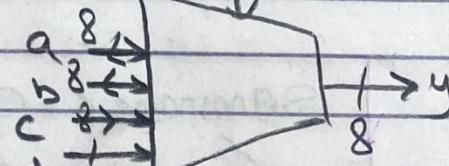
$$2^n \rightarrow 4$$

$$n = 2 \rightarrow 0 \rightarrow 1$$

OUT \rightarrow Signal



② Sel \rightarrow Bus



(معنی ده ان كل واحد سبب 8 خلايا)

input \rightarrow bus

Selector \rightarrow bus

$$2^n \rightarrow 6 \rightarrow n=2$$

OUT \rightarrow Signal

لارقا
الجهات
جاءون
كتراو
كمراه
لوقاه
00 \rightarrow a

SEL		Y
0	0	a
0	1	b
1	0	c
1	1	d

$\text{O}_2 \rightarrow \text{alo}$

$$01 \rightarrow a(1)$$

$$10 \rightarrow a(2)$$

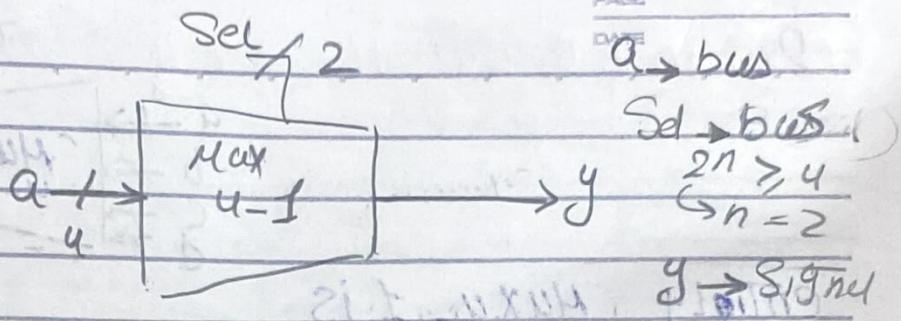
$$11 \rightarrow a(3)$$

هذه الاربع اراء لكم

4bit 3 0.019

وکل مردمی Select

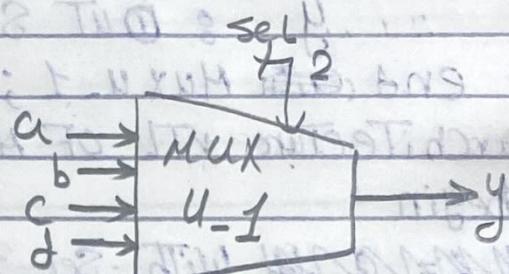
عن واعده ليس من



Selected Signal Assignment (Multiplexer) (With Select)

1

~~entity mux u_1 is~~



```
Port ( Sel : in Std_logic_vector (3 down to 0);  
      a,b,c,d : in Std_logic ;  
      y : out Std_logic );
```

end flux u_{-1} ;

Architecture RTL of Mux 4:1 is

Notes

begin

With SEL Select

$y \leq a$ when "00" g

b When " 01 ",

C When "to",

d When "11".

a When Others •

End rTl •

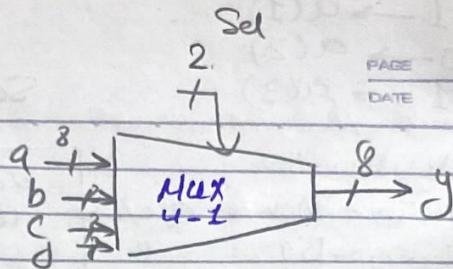
لارج کیجھا std::vector<T> کیا ہے؟

Binary لامباجيل بكتوا

لُوكو^و ← Signs

" " ← Buy لوعو

2.



entity MUXU_1 is

```
Port ( Sel : in Std_logic_vector(1 downto 0);  
      a,b,c,d : in Std_logic_vector(7 downto 0);  
      y : out Std_logic_vector(7 downto 0));  
end MUXU_1;
```

architecture RTL OF MUXU_1 is

begin

with Sel select

y <= a when "00",

b when "01",

c when "10",

d when "11",

a when others;

end RTL;

3.

entity MUXU_1 is

```
Port ( Sel : in Std_logic_vector(1 downto 0);  
      a : in Std_logic_vector(3 downto 0);  
      y : out Std_logic);  
end MUXU_1;
```

architecture RTL OF MUXU_1 is

begin

with Sel select

y <= a when "00",

b when "01",

c when "10",

d when others;

end RTL;

Conditional Assignment

entity MUXU_1 is

```
Port( Sel : in Std_logic_Vector(3 downTo 0);
      a,b,c,d : in Std_logic;
      y : out Std_logic);
end MUXU_1;
```

Architecture RTL OF MUXU_1 is

```
begin
  y <= a When Sel = "00" else
  b When Sel = "01" else
  c When Sel = "10" else
  d;                                ← الترتيب المقصود
                                         ← Others *
```

End RTL;

Sequential Assignment Statement

Using IF. Elsif

Process Process لغز بینی لها خوبان اید

end begin

Process (Sensitivity-list)

```
begin
  If (Cond) Then
    :
  Elsif (Cond) Then
    :
  Else
```

مین Sensitivity list

دست داشت اینها لو

غیرتها بتغير OUT معا

اوئکب جوها حاصل بتصر

علیها اللطف لواتغير

هیغز OUT ولیها

اعل Priority

ماچون

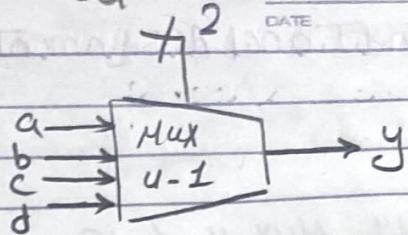
حاتا لوکب جوها فایر زاده ولیها اول رنگ های عمل delay / باز

Code Page 23, 24

Sel

PAGE
DATE

Job entity



entity MUX U_1 is

```
Port ( Sel : in std_logic_vector ( 1 downto 0 );
      a,b,c,d : in std_logic;
      y : out std_logic);
end MUX U_1;
```

architecture RTL OF MUX U_1 is

begin

Process (Sel)

begin

IF (Sel = "00") Then

y <= a;

Elsif (Sel = "01") Then

y <= b;

Elsif (Sel = "10") Then

y <= c;

else

y <= d;

end if;

end Process;

End RTL;

a →

00 → 01

c

حول تغير بختار
شكل طبع التغير
لس

01 → 10 → c

d

← Sel

00

01

10

11

y



العاملات لواتغير
autoregen int

select

hand sim

us 1 solo dec

→ abc ملخص

y ابعاد عبار سل

~~Assignment of S. Plan, Date, Serial No. 1018, 2018~~

Process (Sel, a, b, c, d)

Page 24 c, abd

بِسْمِ اللَّهِ الرَّحْمَنِ الرَّحِيمِ

الحل

PAGE

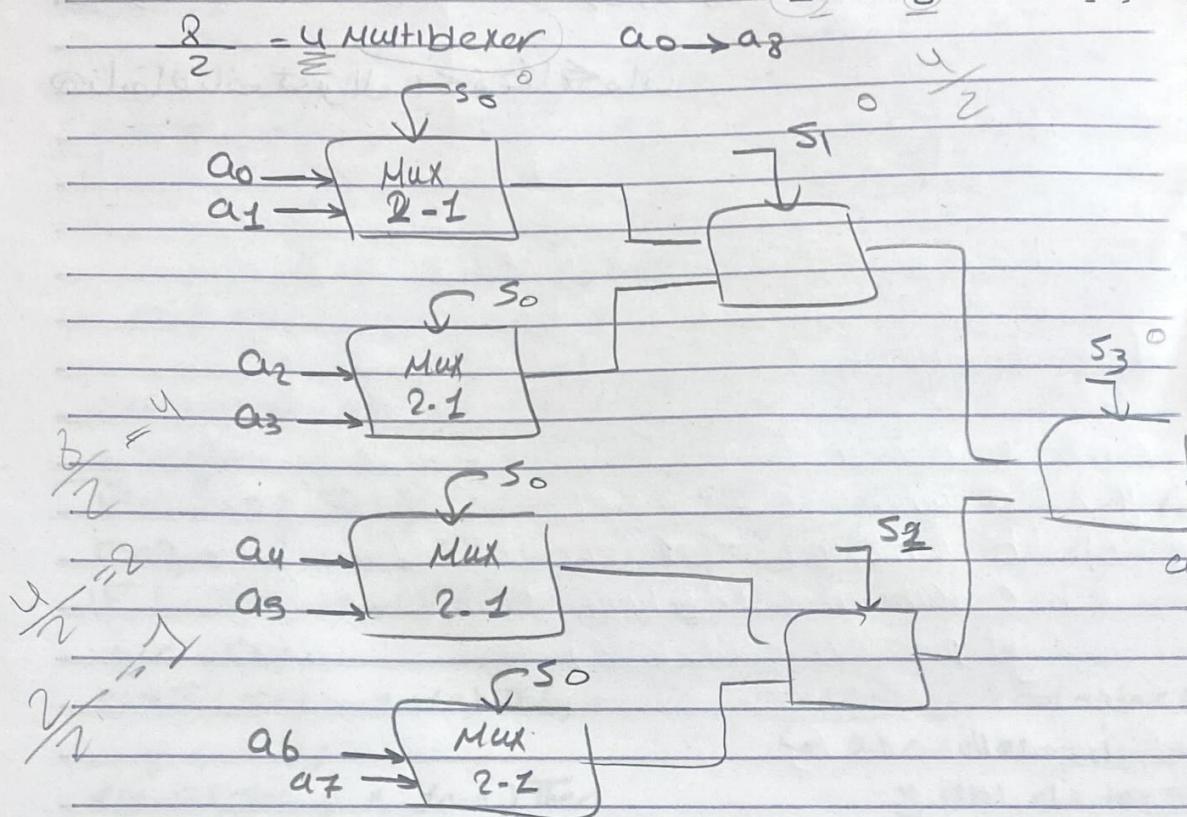
DATE

Design 8 to 1 Multiplexer using only 2 to 1 multiplexer

2 to 8 دوال

$\frac{8}{2} = 4$ Multiplexer

$a_0 \rightarrow a_8$



$$2^n >= 8 \Rightarrow n=3 \quad ③ \text{ مفهوم } s_0 \rightarrow s_2$$

$$2^n >= 2 \rightarrow n=1 \rightarrow \text{ لكل واحد}$$

S			y
s_2	s_1	s_0	
0	0	0	a_0
0	0	1	a_1
0	1	0	a_2
0	1	1	a_3
1	0	0	a_4
1	0	1	a_5
1	1	0	a_6
1	1	1	a_7