Subject : .....

Date: / /

Shift left & right register:-

load "00" → load data
"01" → shift data to right
"10" → shift data to left

VHDL Code with Asynchronous rst:-

```
entity shift_reg is
    Port( rst, clk, load : in std_logic;
          load           : in std_logic_vector(1 downto 0);
          din            : in std_logic_vector(3 downto 0);
          dout           : out std_logic_vector(3 downto 0));
end entity shift_reg;

architecture rtl of shift_reg is
signal d_temp : std_logic_vector(3 downto 0);
 begin
 process(rst, clk)
    if(rst = '1') then
d_temp <= (others => '0');
    elsif (rising_edge(clk)) then
        if(load = "00") then -- load data
            d_temp <= din;
        elsif(load = "01") then -- shift data to right
            d_temp <= '0' & d_temp(3 downto 1);
        elsif(load = "10") then -- shift data to left
            d_temp <= d_temp(2 downto 0) & '0';
        endif;
    endif;
 end process;
 dout <= d_temp;
end architecture rtl;
```