Syn.
Asyn.
A.L
A.L

(C/V event and c/K = h') entity D-FF is Port (din, CIK, rst: in std_109;c; dout ont std_109;c); end D-FF; architecture vt2 of D-FF is begin 600 in

(Vising edge(C|K)) Then | end if;
end process
end HL; Process (c/K) dout <= '0: endif. dent c=din;

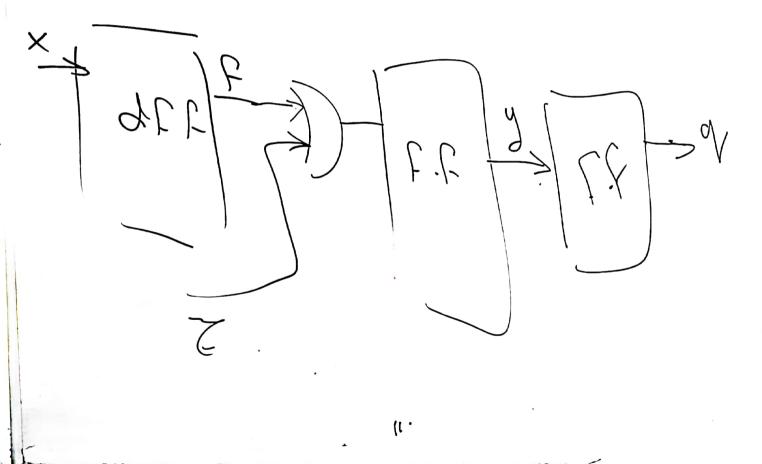
(CIV esent and clk=5) entity D-FF is Port (din, CIK, rst: in std_109;c; dout iont std_109;c); end D-FF; architecture vt2 of D-FF is begin Proce-609in

() -> If (rising -edge(C|K)) Then | End if;
end proces
end HL; Process (c/K) dout <= '0.; enditional cadini

(C/Y esent and clk=5) entity D-FF is Port (din, CIK, rst : in std_109:0; end D-FF; iont std-logic); architecture vt2 of D-FF is begin Process (c/Kirst) begin If (rst="1") Then dout <= 'o ... elsif (rising -edge (C/K)) then dout <= din; endif; End Pricess,

rst υı

الممسوحة ضوئيا بـ CamScanner



C14-5

entity cir-1 is Port (E,X, rst, ClK ', in std-losic, of iont stallogic): end civ_1; drehitecture rtl of cir_1 is Signal Jif: std-logic: | elsip (vising-edge(clk)) Then Process (clk, rst) 16 (rst = (1.) Then ~ nd , K,

Cir-Z

entity Cir-1 is Port (E,X, rst, Clk : in std-box; 9 : out std-109;(): end civ_1; architecture rHL of civ_1 is Clk. Signal fistd-logicilelsif (rising-edge(clk)) then Process (clk, rst)

variable y: std. legic;

/f (rst = 1) Then f <= x; endik, Phol Process,