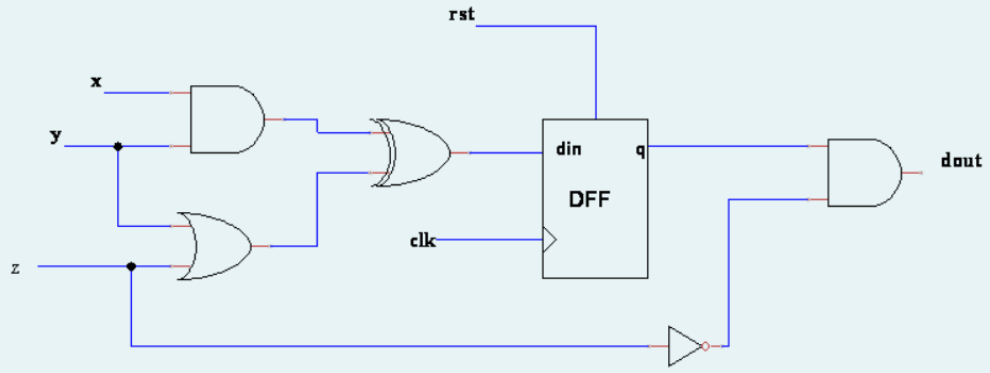
Which of the following represents the correct code for the following circuit?



a.

```
library ieee;

use ieee.std_logic_1164.all;

use ieee.std_logic_arith.all;

entity circuit_1 is

port (x,y,z,clk,rst: in std_logic;

dout: out std_logic);

end entity circuit_1;

architecture rtl of circuit_1 is

signal q,n,m,din :std_logic;

begin

process (clk,rst)

begin

if (rst ='1')then

q <= '0';

elsif (rising_edge(clk)) then

n <= x AND y;

m <= y OR z;

din <= n XOR m;

q <= din;

end if;

end process;

end rtl;
```

b. b & C

c.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
entity circuit_1 is
port (x,y,z,clk,rst: in std_logic;
dout: out std_logic);
end entity circuit_1;
architecture rtl of circuit_1 is
signal q,n,m,din :std_logic;
begin
n <= x AND y;
m <= y OR z;
din <= n XOR m;
process (clk,rst)
begin
if (rst ='1')then
q <= '0';
elsif (rising_edge(clk)) then
q <= din;
end if;
end process;
end rtl;
```

d.

```
library ieee;

use ieee.std_logic_1164.all;

use ieee.std_logic_arith.all;

entity circuit_1 is

port (x,y,z,clk,rst: in std_logic;

dout: out std_logic);

end entity circuit_1;

architecture rtl of circuit_1 is

signal q :std_logic;

begin

process (clk,rst)

variable n,m,din :std_logic;

begin

if (rst ='1')then

q <= '0';

elsif (rising_edge(clk)) then

n := x AND y;

m := y OR z;

din := n XOR m;

q <= din;

end if;

end process;

end rtl;
```

Which of the following can't be declared in an architecture directly?

- a. Constant
- b. Signal
- c. Bit_Vector
- d. Variable

How many types of resets are there in hardware design?

- a. One
- b. Three
- c. Two
- d. Four

Which of the following is correct syntax for entity declaration?

a.
```
ENTITY entity_name
  PORT port_name
  (signal_names : signal_modes;
  signal_names : signal_modes);
 END ENTITY;
```

b.
```
ENTITY entity_name IS
  PORT port_name
  ( signal_names : signal_modes signal_type;
  signal_names : signal_modes signal_type);
 END entity_name;
```

c.
```
ENTITY entity_name IS
  PORT( signal_names : signal_modes;
  signal_names : signal_modes);
 END entity_name;
```

d.
```
ENTITY entity_name
  PORT( signal_names : signal_modes;
  signal_names : signal_modes);
```

During synthesis, a variable infers _____

- a. Flip flop <--- Signal
- b. Wire
- c. Register
- d. Variables are not synthesizable

Why we needed HDLs (Hardware Description Languages) while having many traditional Programming languages?

- a. Traditional programming languages are complex
- b. Some characteristics of digital hardware couldn't be captured by traditional languages
- c. HDLs are complementary to traditional programming languages to complete the design process
- d. HDLs offer more complexity than traditional programming languages.

Which of the following is not defined by the entity?

- a. Names of signal
- b. Behavior of the signals
- c. Direction of any signal
- d. Different ports

Clear my choice

Why do we need to define clock signal in the sensitivity list of the process?

- a. To trigger the statement as soon as there is some event on input
- b. To trigger the clock signal as soon as there is some event on input
- c. To trigger the statement as soon as there is some event on clock
- d. To trigger the clock signal as soon as there is some event on output

What will be the output in the following code?

```
ARCHITECTURE my_logic OF my_design IS
BEGIN
a <= '1';
b <= '1';
PROCESS (a, b)
BEGIN
IF (a AND b = '1') THEN
output <= a;
ELSIF (a OR b = '1') THEN
output <= b;
ELSE
output <= '0';
END IF;
END PROCESS;
END my_logic;
```

- a. 1
- b. b
- c. a
- d. 0

What is the difference between SIGNAL and VARIABLE?

- a. SIGNAL can be used for input or output whereas VARIABLE acts as intermediate signals
- b. SIGNAL is global and VARIABLE is local to the process in which it is declared
- c. The value of SIGNAL never varies whereas VARIABLE can change its value
- d. SIGNAL depends upon VARIABLE for various operations

FPGA stands for...

- [x] a. Field Programmable Gate Array
- [ ] b. Field Program Gate Array
- [ ] c. First programmable Gate Array
- [ ] d. First Program Gate Array

Clear my choice

The cells in a FPGA may contain registers, look-up tables and memory

- a. True
- b. False

Clear my choice

Which of the following circuit can't be described without using a process statement?

- a. D flip-flop
- b. Decoder
- c. Comparator
- d. Multiplexer

Synchronous reset is a fast reset.

- a. True
- b. False

Clear my choice

Which of the following sequential circuit doesn't need a clock signal?

- a. Shift register
- b. Flip flop
- c. Asynchronous counter
- d. Latch

Clear my choice

If a user gets an error at the time which is "the IF statement is illegal" what could be the reason?

- a. Using IF statement without ELSE
- b. Using multiple ELSIF statements
- c. Using IF statement in architecture body directly
- d. Using concurrent assignment in the IF

Clear my choice

Which of the following circuit can be used as parallel to serial converter?

- a. Demultiplexer
- b. Decoder
- c. Multiplexer
- d. Digital counter

VHDL is one of the programming languages

- a. False
- b. True

Clear my choice

How many errors in this code?

```
entity reg_par is

port (clk,rst: in std_logic;

reg_in: in std_logic_vector(7 down to 0);

reg_out: out std_logic_vector(7 downto 0);

end entity reg_par;

architecture rtl of reg_par is

begin

process (clk)

begin

if (rst = '1') then

reg_out <= "00000000";

elseif (rising_edge(clk)) then

reg_out <= reg_in;

end if;

end process;

end architecture rtl;
```

5

- a. None of All
- b. 3

TIME LEFT 0:20:50

QUESTION 1

Not yet answered

Marked out of 0.50

Flag question

A user wants to implement a logic by using VHDL. In which he has inputs from two sensors which are smoke sensor and water level detector. If any input is high, he has to turn on the respective alarm. Which of the following is representing the correct code for the given logic?

Select one:

a. a & c

b.
```
ARCHITECTURE alarm_control OF my_home IS
BEGIN
PROCESS(smoke_sensor, water_sensor)
BEGIN
IF(smoke_sensor = '1') THEN
fire_alarm <= '0';
ELSE
fire_alarm <= '1';
END IF;
IF(water_sensor = '1') THEN
water_alarm <= '1';
ELSE
```

Quiz navigation

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15 16 17 18

Finish attempt ...

c.

```
ARCHITECTURE alarm_control OF my_home IS
BEGIN
PROCESS(smoke_sensor, water_sensor)
BEGIN
IF(smoke_sensor = '1') THEN
fire_alarm <= '1';
ELSE
fire_alarm <= '0';
END IF;
IF(water_sensor = '1') THEN
water_alarm <= '1';
ELSE
water_alarm <= '0';
END IF;
END PROCESS;
  END alarm control;
```

d.

```
ARCHITECTURE alarm_control OF my_home IS
BEGIN
PROCESS(smoke_sensor, water_sensor)
BEGIN
IF(smoke_sensor = '1') THEN
fire_alarm <= '1';
```

```
END PROCESS;
  END alarm control;
```

d.

```
ARCHITECTURE alarm_control OF my_home IS
BEGIN
PROCESS(smoke_sensor, water_sensor)
BEGIN
IF(smoke_sensor = '1') THEN
fire_alarm <= '1';
ELSE
fire_alarm <= '0';
END IF;
IF(water_sensor = '1') THEN
water_alarm <= '1';
ELSE
water_alarm <= '0';
END IF;
END PROCESS;
END alarm_control;
```

Clear my choice

QUESTION 11

Not yet answered

Marked out of 0.50

Flag question

FPGA stands for…

- a. First Program Gate Array
- b. Field Programmable Gate Array
- c. First programmable Gate Array
- d. Field Program Gate Array

Clear my choice

QUESTION 14

Not yet answered

Marked out of 0.50

Flag question

Which of the following is a not a characteristics of combinational circuits?

Select one:

- a. There is no storage element in combinational circuit
- b. There is no use of clock signal in combinational circuits
- c. The output of combinational circuit depends on present input
- d. The output of combinational circuit depends on previous output

Clear my choice

QUESTION 15

Not yet answered

Marked out of 0.50

Flag question

Sequential code can't be used to design combinational circuit.

Select one:

- a. False
- b. True

QUESTION 8

Not yet answered

Marked out of 0.50

Flag question

For using a process to implement combinational circuit, which signals should be in the sensitivity list?

Select one:

- a. Output of the circuit
- b. No signal should be in the sensitivity list
- c. Both of the inputs and outputs
- d. Inputs of the circuit

Clear my choice

QUESTION 3

Not yet answered

Marked out of 1.00

Flag question

What is the correct code for a shift left register that can shift the input data by 3 bits?

a.
```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
entity reg_par is
port (clk, rst: in std_logic;
reg_in: in std_logic_vector(7 downto 0);
reg_out: out std_logic_vector(7 downto 0));
end entity reg_par;
architecture rtl of reg_par is
signal  reg_temp : std_logic_vector (7 downto 0);
begin
process (rst, clk)
begin
if (rst = '1') then
reg_temp <= "00000000";
elsif (rising_edge(clk)) then
reg_ temp <= "111"  & reg_ temp (7 downto 3);
end if;
end process;
reg_out <= reg_ temp;
end architecture rtl;
```

b.
```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
```

QUESTION 4

Not yet answered

Marked out of 0.50

Flag question

Difference between simulation tools and Synthesis tool is _____

Select one:

- a. Simulators and Synthesis tools works exactly same
- b. Simulators are used to check the performance of circuit and Synthesis tools are for the fabrication of circuits
- c. Simulators are used just to check basic functionality of the circuit and Synthesis tools includes timing constraints and other factors along with simulation
- d. Simulation finds the error in the code and Synthesis tool corrects the code

Clear my choice

QUESTION 9

Not yet answered

Marked out of 0.50

Flag question

VHDL is one of the programming languages

- a. False
- b. True

Clear my choice

QUESTION 10

Not yet answered

Marked out of 0.50

Flag question

During synthesis, a variable infers _____

- a. Flip flop
- b. Compantorial circuit
- c. Variables are not synthesizable
- d. Register

Clear my choice

QUESTION 12

Not yet answered

Marked out of 0.50

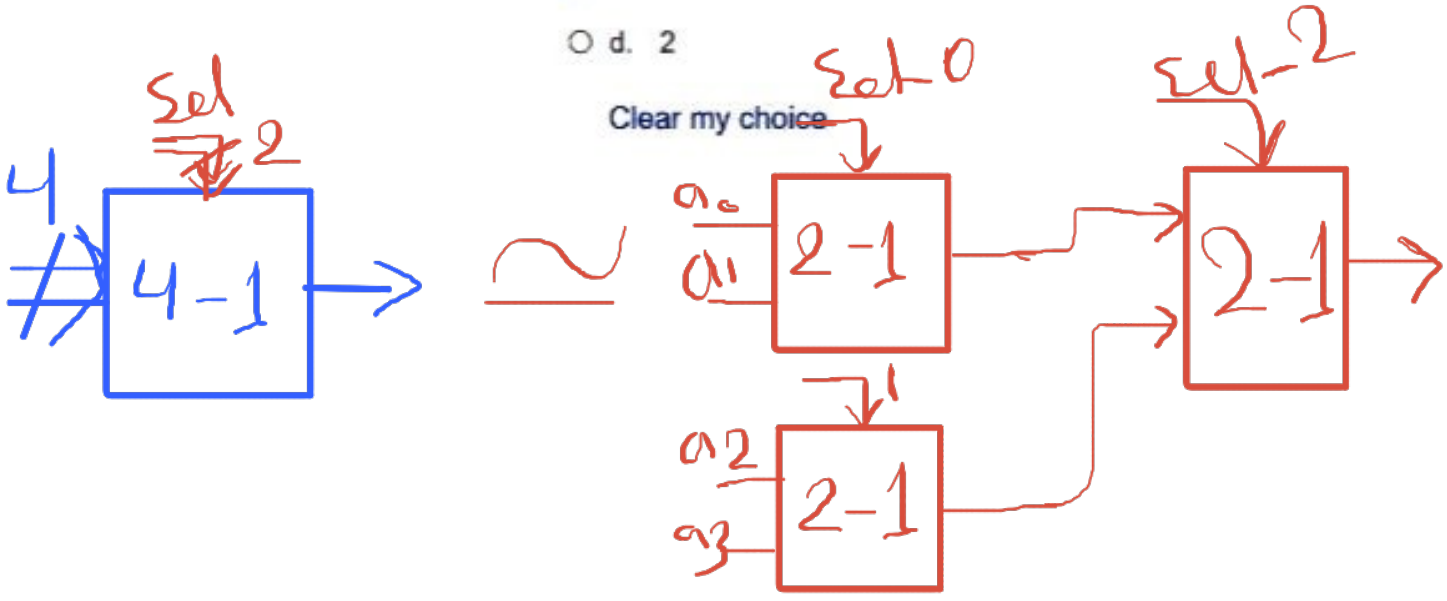
Flag question

If only two bit vectors are allowed to use in the VHDL code, then how many number of multiplexers will be required to implement 4 to 1 Multiplexer?

Select one:

- a. 4
- b. 1
- c. 3
- d. 2

Clear my choice



QUESTION 13

Not yet answered

Marked out of 0.50

Flag question

If the declarative part in the architecture of a half adder is as below

```
ARCHITECTURE    OF my_logic IS
 BEGIN
 y <= (a AND c) AND (b OR c);
END ARCHITECTURE;
```

- a. Data flow
- b. Structure
- c. None of the mentioned
- d. Behavior

Clear my choice

QUESTION 2

Not yet answered

Marked out of 0.50

Flag question

Which of the following sequential circuit doesn't need a clock signal?

- a. Asynchronous counter
- b. Flip flop
- c. Shift register
- d. Latch

Clear my choice

QUESTION 6

Not yet answered

Marked out of 0.50

Flag question

In which of the situations listed below would a designer use an FPGA?

Select one:

- a. The system should be fast.
- b. Only few copies of the system will be produced and we have a limited budget to spend on all the components.
- c. The system should be as power efficient.

QUESTION 7

Not yet answered

Marked out of 0.50

Flag question

Which of the following circuit can be used as parallel to serial converter?

- a. Demultiplexer
- b. Multiplexer
- c. Decoder
- d. Digital counter

Clear my choice

Mid_Term Exam (page 4 of 4) - Google Chrome

moodle.sha.edu.eg/mod/quiz/attempt.php?attempt=670702&cmid=49709&page=3

TIME LEFT 0:03:47

QUESTION 16

Not yet answered

Marked out of 1.50

Flag question

The number of errors in the following code is _____

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
entity mux4_1 is
port (sel: in std_logic_vector (0 to 1);
a, b, c, d: in std_logic_vector(7 downto 0);
y: out std_logic_vector(7 downto 0);
end entity mux4_1;
architecture rtl of mux4_1 is
begin
process (sel)
begin
if (sel = '00') then
```

Quiz navigation

1 2 3 4 5 6 7
8 9 10 11 12 13 14
15 16 17 18

Finish attempt ...

Type here to search

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```
process (sel)
begin
if (sel = '00') then
y <= a;
elsif (sel = '01') then
y <= b;
elsif (sel = '10') then
y <= c;
else
y <= d;
end process;
end architecture rtl;
```

Select one:

- a. 5
- b. 3
- c. none of these
- d. 7

a.

```
ARCHITECTURE rtl of circuit_1 is

BEGIN


PROCESS ()


                -- Here


BEGIN


END PROCESS;
```

b.

```
ARCHITECTURE rtl of circuit_1 is


                -- Here

BEGIN

PROCESS ()

BEGIN
```

```
begin

if (rst ='1')then

q <= '0';

elsif (rising_edge(clk)) then

n := x & y;

m := y OR z;

din := n XOR m;

q <= din;

end if;

end process;

dout1 <= q;

dout2 <= din;

end rtl;
```

- a. 3
- b. 2
- c. None of All
- d. 4