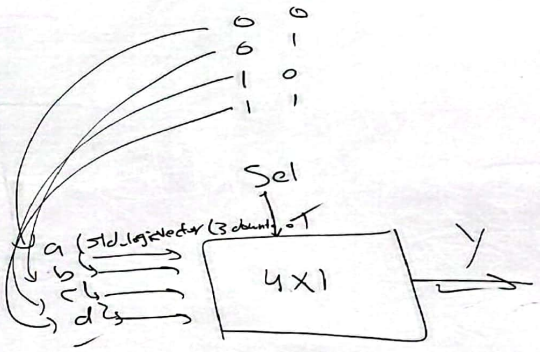
MUX

```
ENTITY MUL_4_1 is
Port( sel: in std_logic_vector(1 downto 0);
      a,b,c,d : in std_logic;( vector(3 downto 0);
         Y: out std_logic); ( _ vecto(3 downto 0);
   END ENTITY mul_4_1;
```

```
ARCHITECTURE rtl of mul_4_1 IS
BEGIN
   With sel  Select
   Y<= a  when "00";
      b when "01" ;
      c  when "10" ;
      d  when "11" ;
   END ARCHITECTUR rtl;
```

① ARCHITECTURE rtl of mul_4_1 is

```
Begin
Process( sel, a,b, c, d )
  begin
iF( sel="00") then
    y<= a;
els iF(sel="01") the
    y<=b;
elsiF (sel="10") then
   y<= c;
 else
   y<=d;
 end iF;
end process;
end ARCHITECTURE rtl;
```



$4 = 2^2$

Mux 4-1

8-1

```
ARCHITECTURE rtl of mul4_1 IS
 BEGIN
 Process( sel, a, b, c, d)
 begin
 case sel is
 when "00" => Y <= a;
 when "01" => Y <= b;
 when "10" => Y <= c;
 when "11" => Y <= d;

 end case;
 end process;
 END ARCHITECTURE rtl;
```

MUX 7-1

MUX 9-1