Modified Hetero-Gate-Dielectric TFET for Improved Analog and Digital Performance

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***Abstract*— In this paper, we have investigated the effect of shifting a high-k dielectric pocket of a 5 nm length over the tunneling and channel regions of a Hetero-Dielectric Tunneling Field Effect Transistor (HDTFET) on the DC, analog and digital performance. We propose the optimum shift length that could achieve the highest ON current and the lowest sub-threshold swing without deteriorating analog and transient performance. ON-state current, ON to OFF current ratio (I_{ON}/I_{OFF}), and Sub-threshold swing (*SS*) were realized as DC performance figures of merits. Transconductance (g_m) and the cutoff frequency (f_T) were considered as analog performance figures of merit. Moreover, transient performance was investigated, considering fall propagation delay (t_{phl}) and overshoot voltage (V_P) as figures of merits, when operating the proposed design in an inverter circuit. The proposed design shows a significant enhancement in DC, analog and circuit-level performance parameters over the conventional TFET according to the results obtained from TCAD simulation.**

Keywords*— TFET, ON to Off current ratio (I_{ON}/I_{OFF}), Subthreshold swing (SS), Transconductance (g_m), Cutoff frequency (f_T), Fall propagation delay (t_{phl}), Overshoot voltage (V_p).

I. INTRODUCTION

In order to address the great demand for scaling down of electronic devices, there have been various studies of novel electronic devices that can overcome the scaling limits of MOSFETs [1], [2]. One of the most promising alternatives, encountered in this field, is the tunneling field effect transistor (TFET). The drain current of TFETs depends on charge carriers tunneling through the potential barrier between the valence band of the source and the conduction band of the channel rather than thermionic emission [3]. TFET has the advantages of lower leakage current, *SS* less than 60 mV/decade, low-power consumption and better immunity against short channel effects (SCEs) [4]. These benefits paved the way for introducing TFET to the field of low-power applications [5], [6].

Contrarily, it has been claimed that TFET suffers from low ON-state current and high ambipolar current [7]. To boost the ON current, numerous studies have been established in literature. Some of the ideas proposed by these studies are double-gate architecture [8], using a high-*k* gate dielectric over the channel [9], or a low-*k* spacer [10]. Additional techniques include adding a pocket layer between the source and the channel (to form a PNPN structure) [11], [12] or using a strain silicon technique [13].

One of the interesting studies conducted to enhance the ON current is using a hetero-gate-dielectric TFET where a combination of high-k dielectric material and silicon dioxide (SiO_2) are used as dielectric gate materials. In [14], the length of the high-k dielectric material (HfO_2) at the source side of the channel is equivalent to the length of SiO_2 at drain side of the channel equal to the half of the channel length. Results showed higher ON-state current, lower ambipolar current and smaller *SS*. In another study [15], the effect of reducing an HfO_2 pocket length adjacent to the source over the channel (keeping SiO_2 as the remaining gate dielectric material) was studied that showed reduction of *SS* when reducing the length of the HfO_2 pocket. At a 5 nm length of the HfO_2 pocket, minimum *SS* was achieved.

In this paper, we propose a modified hetero-dielectric TFET (HDTFET) that uses a combination of HfO_2 of 5 nm length (according to the optimization done in [15]) and SiO_2 as gate dielectric materials while studying the effect of shifting the HfO_2 pocket over the tunneling and channel regions on the DC, analog and circuit level performance. ON-state current, I_{ON}/I_{OFF}, and *SS* are regarded as figures of merits for DC performance. Further, the influence of the proposed study on total gate capacitance is reckoned. Moreover, analog performance is analyzed through transconductance (g_m) and cutoff frequency (f_T). Transient analysis of the proposed HDTFET design is also investigated considering the overshoot voltage (V_p) and fall propagation delay (t_{phl}) as main digital performance parameters.

II. SIMULATION APPROACH

IC technology is one of the rapid progressing fields nowadays. The great need to study different device structures while avoiding fabrication process complexity made TCAD simulations highly important. By using TCAD simulations, new device architectures could be investigated to improve the device performance of existing structures. It has been confirmed extensively that numerical simulations are an efficient means to

explore novel devices like the Tunnel FET behavior. The dependence of TFET characteristics could be examined numerically when its various design parameters change with no need for high fabrication cost and complexity.

All simulations of the proposed design have been carried out using Silvaco/ATLAS device simulator version 5.20.2.R. The non-local BTBT model (BBT.NONLOCAL) was utilized to find the tunneling generation rate across a tunneling length and to incorporate the change in the electric field along the tunneling length [16]. Fine meshing and quantum tunneling meshing (qt.mesh) in the regions where BTBT mainly takes place were defined.

Lombardi (CVT) model was selected as the mobility model in order to consider the effects of temperature, total doping concentration and lateral and perpendicular electric fields. Band gap narrowing (BGN) was enabled to account for high doping appearing in the source and drain regions [17]. Schokley Read Hall (SRH) and Auger recombination models were also used. Newton numerical method was used for better convergence. Further, to get the figures of merit of the high-frequency performance, a small-signal AC analysis was performed at a frequency of 1 MHz.

The non-local BTBT model used has been calibrated against Boucart's work [9] as done in [18]. Optimum values for electron effective mass (m_e) and hole effective mass (m_h) were found to be 0.12 and 0.17, respectively. It may be mentioned that this study mainly focuses on the usage of qualitative trends to demonstrate the relative impact of the proposed design on the device characteristics with respect to the conventional structure by utilizing a qualitative approach.

III. Device Structure and Parameters

A cross-sectional view of the proposed HDTFET that uses the combination of HfO_2 of 5 nm long and SiO_2 as gate dielectric materials is shown in Fig. 1. The design parameters used in device simulations are listed in Table I. Channel (L_{ch}), source (L_s) and drain lengths (L_d) are 50 nm. The gate oxide material thickness (t_{ox}) is 3 nm and the silicon film thickness (t_{Si}) is 10 nm. Doping levels for source, channel, and drain regions are 1×10^{20}, 1×10^{17}, and 5×10^{18} cm^{-3}, respectively. Gate contact work function was set to be 4.5 eV.

In our analysis, the ON-state current (I_{ON}), I_{ON}/I_{OFF} and SS are considered as figures of merit for DC performance. The ON current is calculated at the condition of V_{GS} = 1 V and V_{DS} = 1 V, while the OFF current is calculated at V_{GS} = 0 V and V_{DS} = 1 V. The subthreshold swing is defined as the change in V_{GS} that should be applied to create a one decade rise in output current [19]. Regarding the analog/RF performance parameters, the transconductance (g_m) and cutoff frequency (f_T) are taken as figures of merit. The cutoff frequency can be expressed as ($f_T = g_m/2\pi C_{gg}$) where C_{gg} is the total gate capacitance that represents the summation of gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) [2].

The fall propagation delay (t_{phl}) and voltage overshoot (V_p) are figures of merit for transient analysis. The fall propagation delay is defined as the delay time of mid-input point to the mid-output point and overshoot voltage is the difference between the maximum output voltage and V_{DD} [20].

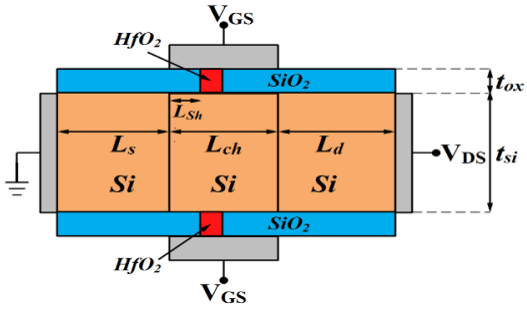

Fig. 1 A cross-sectional view of the proposed HDTFET showing the main device and biasing parameters

Table I Design parameters applied to device simulation

Parameter	Symbol	Value	Unit
Source Length	L_s	50	nm
Channel Length	L_{ch}	50	nm
Drain Length	L_d	50	nm
Gate oxide thickness	t_{ox}	3	nm
Si film thickness	t_{Si}	10	nm
Source doping (p-type)	N_s	1×10^{20}	cm^{-3}
Drain doping (n-type)	N_d	5×10^{18}	cm^{-3}
Channel doping (p-type)	N_{ch}	1×10^{17}	cm^{-3}
Gate work function	Φ_g	4.5	eV

IV. Results and Discussion

The transfer characteristics (I_D–V_{GS}) of the conventional TFET (with uniform gate oxide of SiO_2) and modified HDTFET at different shift values (L_{Sh}) is shown in Fig. 2. The results reveal that positive L_{Sh} values show higher I_{ON} than negative L_{Sh} values. At L_{Sh} of 1.5 nm, the highest I_{ON} is achieved with a value of 5.38×10^{-5} A/μm.

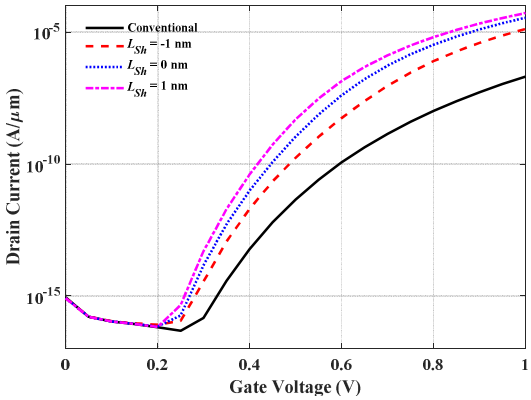

Fig. 2 Transfer characteristics of conventional TFET and HDTFET at different values of L_{Sh}

Fig. 3 shows I_{ON}/I_{OFF}, and SS for different L_{Sh} values. The results show that L_{Sh} of 1.5 nm gives the highest I_{ON}/I_{OFF} with a value of 6.59×10^{10} and SS of 24 mV/decade. Further increase of L_{Sh} in the positive range decreases I_{ON} and I_{ON}/I_{OFF}. As a result, L_{Sh} of 1.5 nm can be selected to as optimum L_{Sh} value in terms of DC performance.

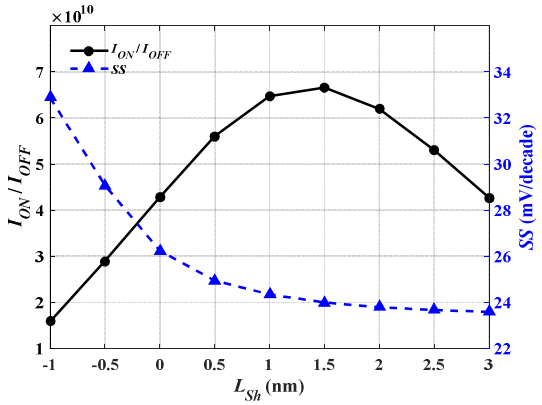

Fig. 3 I_{ON}/I_{OFF} and SS versus L_{Sh}

In order to physically explain the reason for achieving the proposed HDTFET higher drain current values than conventional TFET specially at L_{Sh} value of 1.5 nm, the non-local band to band tunneling (BBT) rate for electrons and holes and minimum tunneling width at the ON state (V_{GS} = 1 V and V_{DS} = 1 V) were investigated. A comparison between conventional TFET structure and the proposed HDTFET for different L_{Sh} values considering non-local band to band tunneling (BBT) rate for electrons and holes is shown in Fig. 4 and Fig. 5, respectively. It can be inferred that the highest tunneling rates for electrons and holes are achieved by HDTFET at L_{Sh} of 1.5 nm with values of 31.32 $cm^{-1}s^{-1}$ and 31.59 $cm^{-1}s^{-1}$.

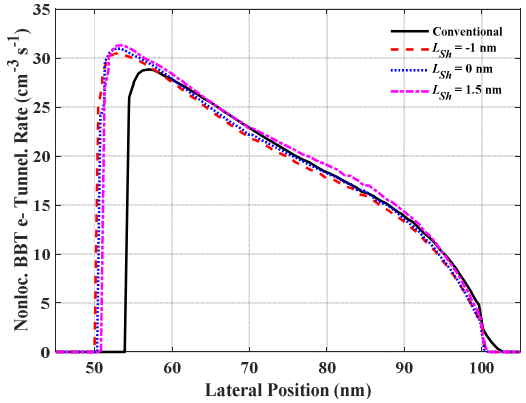

Fig. 4 Non-local BBT electrons tunneling rate of conventional TFET and HDTFET at different values of L_{Sh}

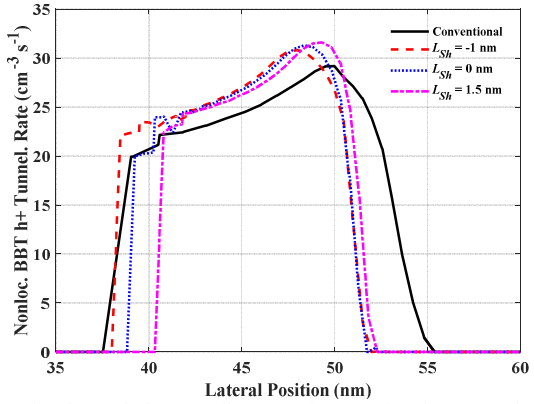

Fig. 5 Non-local BBT holes tunneling rate of conventional TFET and HDTFET at different values of L_{Sh}

Fig. 6 gives more illustration to the addressed phenomena through calculating the minimum tunneling width for the proposed HDTFET at different L_{Sh} values. The results reveal that L_{Sh} value of 1.5 nm has the least minimum tunneling width of 4 nm giving more explication for achieving the proposed HDTFET highest drain current between addressed structures at L_{Sh} value of 1.5 nm.

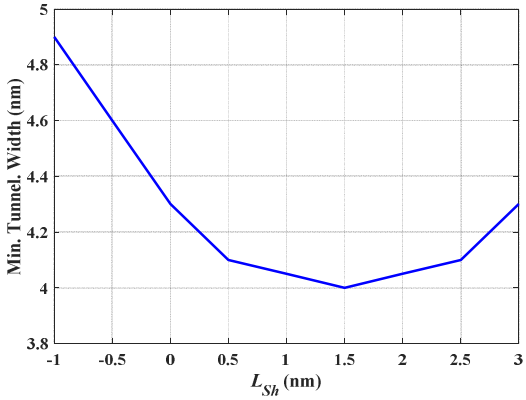

Fig. 6 Minimum tunneling width at different values of L_{Sh}

Addressing the change of SS for different L_{Sh} values from an analytical point of view, the analytical model presented in [21] was considered. In [21], WKB approximation was applied to obtain a relation ship that proves that SS is inversely proportional to the rate of change of minimum tunneling width with respect to gate voltage (dW_T/dV_{GS}). The analysis started with WKB approximation that states that band to band tunneling $T(E)$ is given by:

$$T(E) \approx e^{-2\int_{x_o}^{W} k(x)dx} \quad (1)$$

where $k(x)$ is quantum wave vector of electron inside the barrier, x_o is the start of the tunneling barrier, and W is tunneling barrier width. Solving the integration, we obtain the following equation for $T(E)$:

$$T(E) \approx e^{-[\frac{4\sqrt{2m}}{3\hbar}(\frac{W}{U_o})(U_o-E)^{3/2}]} \quad (2)$$

Where U_o is the top of the barrier, and E is the band gap of the semiconductor material. Solving for SS,

$$SS^{-1} = \frac{d[log_{10}(I_d)]}{dV_G} \propto \frac{d[log_{10}(T(E))]}{dV_G} \propto \frac{d(W(V_G))}{dV_G} \quad (3)$$

Reflecting on our proposed device, the minimum tunneling width was calculated at the onset of BTBT operation (V_{GS} = 0.2 - 0.4 V) for L_{Sh} values of 0, 1.5, and 3 nm as shown in Table II. Later dW_T/dV_{GS} was calculated for the addressed L_{Sh} values as in Table III. Observing dW_T/dV_{GS} values, L_{Sh} of 3 nm has the highest dW_T/dV_{GS} value that is a bit higher than L_{Sh} of 1.5 nm. Moreover, L_{Sh} of 0 nm shows lower dW_T/dV_{GS} value than L_{Sh} of 1.5 and 3 nm that can explain the reason for having higher SS at L_{Sh} of 0 nm while having approximately equal SS at L_{Sh} of 1.5 and 3 nm that is less than SS at L_{Sh} of 0 nm.

Table II Minimum Tunneling Width at onset of BTBT operation

		Minimum Tunneling Width (nm)		
		L_{Sh} = 0 nm	L_{Sh} = 1.5 nm	L_{Sh} = 3 nm
V_{GS} (V)	0.2	19.9	20	22
	0.4	10.5	8	8.5

Table III Rate of change of minimum tunneling width with respect to gate voltage

	L_{Sh} = 0 nm	L_{Sh} = 1.5 nm	L_{Sh} = 3 nm
$\lvert dW_T/dV_{GS}\rvert$	47	60	67.5

Further, the effect of L_{Sh} on the total gate capacitance (C_{gg}) of the device is shown in Fig. 7. It can be deduced that generally HDTFET has a higher C_{gg} than the conventional TFET. The increase of L_{Sh} in the positive direction leads to a reduction of C_{gg}. L_{Sh} of 1.5 nm shows the least value of C_{gg} when compared with L_{Sh} of 0 nm and –1 nm. On the other hand, when considering transconductance, the choice of L_{Sh} = 1.5 nm gives the highest g_m among the other cases as depicted from Fig. 8. Considering the effect of L_{Sh} on f_T shown in Fig. 9, L_{Sh} of 1.5 nm shows the highest maximum f_T with a value of 184.59 GHz. This can be explained because L_{Sh} of 1.5 nm showed highest g_m value and least C_{gg} value when comparison to other L_{Sh} values.

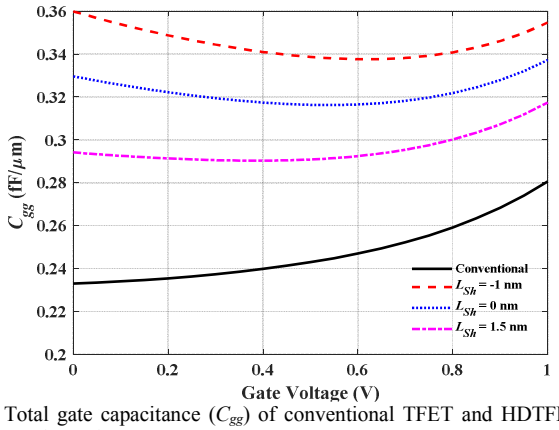

Fig. 7 Total gate capacitance (C_{gg}) of conventional TFET and HDTFET for different values of L_{Sh}

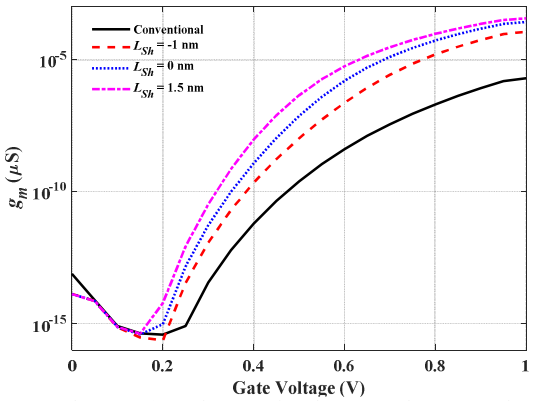

Fig. 8 Transconductance (g_m) of conventional TFET and HDTFET for different values of L_{Sh}

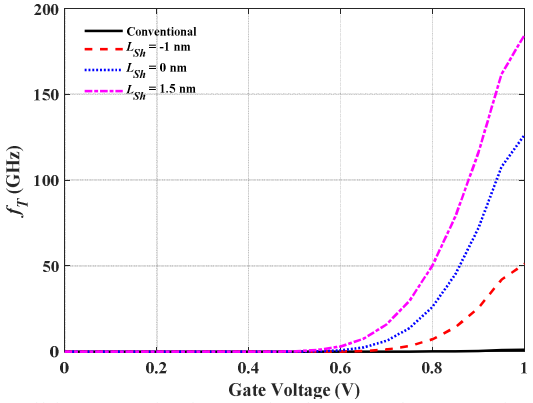

Fig. 9 Cutoff frequency (f_T) of conventional TFET and HDTFET for different values of L_{Sh}

Moreover, the transient response of an inverter circuit containing the n-TFET with a resistive load (R_L) shown in Fig. 10 was investigated, where the input voltage is a pulse with an amplitude of 1 V and rise time of 20 ps, V_{DD} is 1 V, R_L is 100 MΩ, and incorporating a load capacitor of value of C_L = 1 fF. Transient analysis results of the proposed design for different L_{Sh} values are shown in Fig. 11. Again, L_{Sh} of 1.5 nm shows the lowest overshoot voltage and fall time with values of 53 mV and 37.32 ps, respectively. Accordingly, L_{Sh} of 1.5 nm showed the best transient performance proving that it is the optimum L_{Sh} value in terms of transient performance.

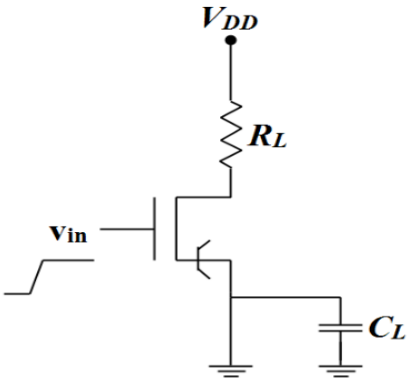

Fig. 10 Resistive load n-TFET inverter circuit

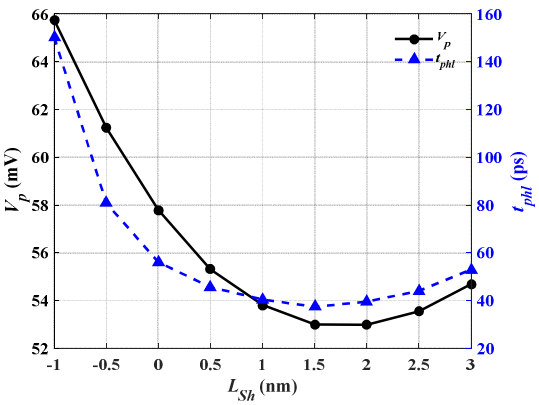

Fig. 11 Voltage overshoot (V_p) and fall propagation delay (t_{phl}) versus L_{Sh}

V. CONCLUSION

In this work, 2-D TCAD Silvaco simulations are used to study the impact of shifting an HfO_2 pocket of 5 nm through SiO_2 channel oxide of HDTFET on the DC, analog and transient performance. An optimum shift value of length 1.5 nm was found. Considering this shift value, the proposed design achieved ON-state current of 5.38×10^{-5} A/μm, I_{ON}/I_{OFF} of 6.59×10^{10}, *SS* of 24 mV/decade, and maximum cutoff frequency of 184.59 GHz. Moreover, it achieved an overshoot voltage of 53 mV and fall time 37.32 ps when operated in an inverter circuit with a resistive load. The advantageous results obtained for the proposed design show its usability in the field of digital and analog applications.

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