Digital Design using CMOS and Hybrid CMOS/Memristor Gates: A comparative Study

Nada Ibrahim, Sara Salah
Department of Communication and Electronics Engineering
Faculty of Engineering
Ain Shams University
{nada.afifyy, sara.messallam}@gmail.com

Mona Safar, M. Watheq El-Kharashi
Department of Computer and Systems Engineering
Faculty of Engineering
Ain Shams University
{mona.safar, watheq.elkharashi}@eng.asu.edu.eg

Abstract – Memristor is a passive element with two terminals, where the magnetic flux is related to the amount of the electric charge passed through the device. Memristive technologies are valuable as they are scalable, non-volatile and compatible with CMOS. In this paper, AND, OR and XOR logic gates which are the seed of any digital design are simulated using memristor, the used memristor model is Voltage ThrEshold Adaptive Memristor (VTEAM), to compare between memristor-based designs and the known CMOS-based logic gates knowing that CMOS technology used is TSMC 65 nm. A few parameters such as propagation delay, power consumption, number of devices used in each circuit have been calculated and studied in both approaches. The proposed logic shows lower power consumption and better area utilization compared to 65 nm CMOS logic circuits operating at standard 1.2 V. Our simulations were run using Cadence Virtuoso IC6.1.4 simulator.

Keywords— Hybrid; logic gates; memristor; power calculation; VTEAM;

I. INTRODUCTION

The memristor theory bases on a resistor that could vary its resistance according to the voltage applied across its terminal. In case of no voltage applied on these terminal, the charges are kept on the same value which indicates the previous voltage that was applied to them and this explain why the memristor can be used as memory element and this is an evidence of memristor non volatility feature.

Several models for memristors have been developed. One type of models is physical models that try to fit the dynamic behavior of a specific memristor. These models are complicated and based on mathematical fitting of experimental results for a specific device under a certain experimental set, while the actual physical mechanism is still unknown. For this reason, different approach for memristor modeling is used which is defining mathematical models such as Linear Ion Drift, Nonlinear Ion Drift, Simmons Tunnel Barrier, TEAM, and VTEAM. The model is chosen according to the desired characteristics of application. These models are implemented in Verilog-A. In this paper the used memristor model is Voltage ThrEshold Adaptive Memristor (VTEAM) [3].

There are three separate logic families can be distinguished. First, Logic in memory, where the logic operations are done within memory cells. In this family the logic values are represented as resistance. Gates in this family include IMPLY and MAGIC. Second, Hybrid CMOS Memristor Logic. In this family memristors are used as computational units only, it requires both CMOS gates along with memristor based gates. Logic values are stored as voltages. And third, Programmable Logic Memristor Array (PLA). This family is in fact a regular PLA, memristors are used to connect between horizontal and vertical wires. In this paper, Hybrid CMOS Memristor Logic is used as it is the most suitable logic family for digital designs.

The paper is organized as follows: Section II describes the modeling of memristor. Section III describes the hybrid CMOS Memristor logic used in logic gate. Schematics of logic gates and their logic computation models are described in Section IV including the gates design and their transient response analysis. Power dissipation calculation is described in Section V. Comparison of parameters like delay, rise time, fall time, power and number of elements used in each circuit between the hybrid-based gates and CMOS based gates is mentioned in Section VI. Conclusion and summary of the paper is included in Section VII.

II. MEMRISTOR MODELING

HP labs at the first production developed the Linear Model of Memristor which is a very simple model assuming that charged ions move freely due to the effect of large field, the conductance changes according to this movement. This concept modeled by two series resistors Ron and Roff where Roff >> Ron and the state variable W represents the relative part of each resistor [1].

$$v(t) = (Ron * \frac{w(t)}{D} + Roff\ (1 - \frac{w(t)}{D})) * i(t) \quad (1)$$

$$w(t) = \mu v * \frac{Ron}{D} * i(t) \quad \text{where } \mu v \text{ is ion mobility} \quad (2)$$

From (1) and (2) the memristance can be calculated M(q) when Roff >> Ron so the M(q) is reduced to

$$M(q) = Roff\ (1 - \frac{\mu v * Ron}{D^2} * q(t)) \quad (3)$$

The linear model was not enough to describe HP's memristor. Non-linear Model was introduced by adding a tunneling effect based on Simmons tunneling. Non-linear model uses the same relation between i(t), v(t) and M(q), the state variable W represents the width of a tunneling barrier, which is changed by current. The change in W is different between opening and closing the memristor [5].

TEAM (ThrEshold Adaptive Memristor model) model was introduced to overcome the complexity and variety of the models. The model separates between the current response and state variable. It demonstrates the memristor characteristics of having an adaptive nonlinearity and a current threshold. TEAM model has the advantage of having defined current-voltage relationship which enable us to use it as if it is linear ion drift memristor model. Also, this model is more generic and provides accuracy comparing to practical memristive devices [6], [7].

The voltage described in (1) can be changed for TEAM model as in (4).

$$v(t) = (Ron + \frac{Roff - Ron}{xoff - xon}(x - xon)) * i(t) \quad (4)$$

where Roff and Ron are the maximum and minimum device resistance respectively, xoff and xon are the internal state variable x's maximum and minimum possible values for the memristor.

Recently, TEAM model became more common to be used in electronic designs as it is simple physical element and has high level of accuracy with low computational complexity.
The main idea for TEAM model is the threshold current, resistance is affected by the current in ranges exceed this threshold only. By experiments of some memristor based structures, it is reached that a threshold voltage has is better in specific memory and logic applications than a threshold current. So another memristor model is introduced with the TEAM model merits and additionally a threshold voltage is introduced which is named the VTEAM model.

The I-V relationship in the VTEAM model could be linear or exponential dependent on the resistance and state
Linear relationship is expressed in (5)

$$i(t) = \left[Ron + \frac{Roff - Ron}{woff - won}(w - won)\right]^{-1} * v(t) \quad (5)$$

won and $woff$ are the bounds of the internal state variable w, and RON and $ROFF$ are the corresponding resistances of the device when the state variable is, respectively, won and $woff$. Or else, the exponential dependence on the state variable is expressed in (6).

$$i(t) = \frac{e^{\frac{Roff / Ron}{woff - won} * (w - won)}}{Ron} * v(t) \quad (6)$$

The VTEAM model is more accurate than the existing memristor models [8].

III. Hybrid CMOS Memristor Logic

The memristance of the memristor change according to the direction of the current flows through the memristor. When the direction of current is out from the right terminal the memristance increases and the opposite direction of the current decreases the memristance.

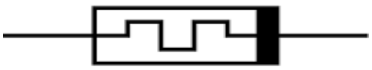

Figure 1 - Memristor Symbol

The voltage of the memristor terminals is changed upon the memristance value and this voltage value represent the logic values [2].

The method of Hybrid CMOS Memristor logic uses voltages to denote logic states. The AND and OR gates do not comprise a full set of operations so additional CMOS buffers are needed.
The output voltage doesn't always remain in the correct value even if the change in inputs does not call for a change in the output. This happens due to the fact that the output gets it's voltage from the node connected to the memristor with lower memristance, and that for different inputs the memristors might switch values.

The meaning of this is that these gates can cause "Dynamic Hazards" and therefore the output value cannot be sampled shortly after a change in the input values, but only after a measured propagation time. This phenomenon will affect the timing constraints of any logic implemented with this family.

There are two problems concerning the output voltage of the memristor based circuits. The first one is the voltage divider which causes decaying of output voltage. The second problem occurred in circuits containing cascaded gates where some current pass from the first gate output to the second gate input instead of passing the whole current from first input in the circuit to the second input. From gate point of view one of the memristors allowed the whole current to pass through it however the other one allows only some of the current to pass (total input current – output current). The different current levels lead to the problem of not full switching between memristors. In case of low voltage threshold memristor, this issue will not be highlighted due to the less sensitivity of this type of memristors.
The circuit structure is a great factor in highlighting the mentioned issue which may lead to different behavior and accordingly different results despite applying the same inputs.
The used approach is to put CMOS element (buffer or inverter) between every two gates, so the problem is solved by eliminating the current flows through the output node as

the gate of a transistor in the buffer does not allow the current flow.
The hybridization of CMOS elements and memristors mandates usage of certain voltage to prevent infractions and undesired effects.

IV. Gate Designs and Simulations

A. Function Description

For AND gate, in case of different inputs, the gate will operate according to the polarity of the memristors. When current flows into the logic gate through one input, output voltage value is derived from voltage divider between high input voltage with Ron and Roff of memristor where Roff is much higher than Ron [4].

$$Vout = Vhigh * \frac{Ron}{Roff + Ron} \approx 0 \quad (7)$$

In case of similar inputs, whether high or low voltage inputs, no current will flow in the circuit in the path between the two inputs, so the voltage values of input and output terminals will be the same as there is no voltage drop between the two inputs.

$$Vout = Vhigh * \frac{Roff}{Roff + Ron} \approx Vhigh \quad (8)$$

For OR gate memristor will operate with the same mechanism so that the output voltage is derived according to the known truth table of OR gate. The change in polarity causes the low memristance to be located near the high voltage, and vice versa. For XOR gate, there is no new operation mechanism from memristor as XOR design is based on AND and OR gates. For NAND and NOR gates, it is operate exactly the same as AND and OR gates – respectively- from memristor point of view and inverting the output of the memristor design by connecting the output to CMOS inverter. For XNOR gate, it uses the same mechanism of Hybrid CMOS memristor design as it is based on AND, OR and CMOS inverter.

B. Gates Design

OR Gate design is two series memristors connected in opposite polarity where the common node is the output of the gate and the two inputs of the gate are connected to the positive terminals of each memristor as shown in Figure 2 [4].

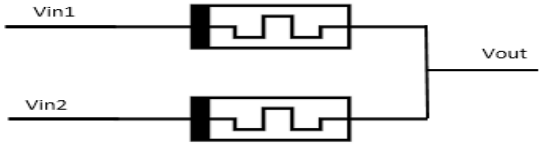

Figure 2 - OR gate design

AND Gate design is two series memristors connected in opposite polarity where the common node is the output of the gate and the two inputs of the gate are connected to the negative terminals of each memristor as shown in Figure 3.

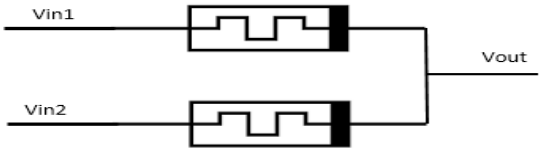

Figure 3 - AND gate design

XOR gate based on AND and OR logic gates and an inverter as shown in Figure 4. Some buffers are inserted at some nodes to avoid the erosion of output voltage of the logic gates and fan-out issue.

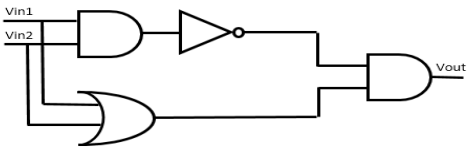

Figure 4 - XOR gate deign

NAND gate design is the same design of the AND gate connected to CMOS inverter as there is no memristor based NOT gate.

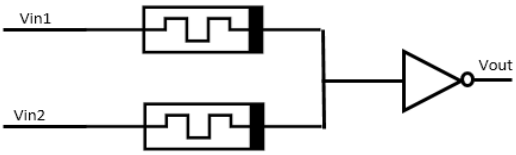

Figure 5 - NAND gate design

NOR gate design is the same design of the OR gate connected to CMOS inverter as there is no memristor based NOT gate.

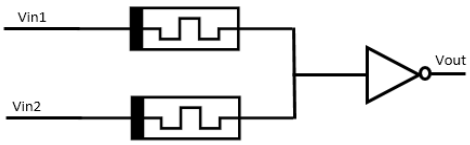

Figure 6 - NOR gate design

XNOR gate design is the same design of the XOR gate connected to CMOS inverter as there is no memristor based NOT gate.

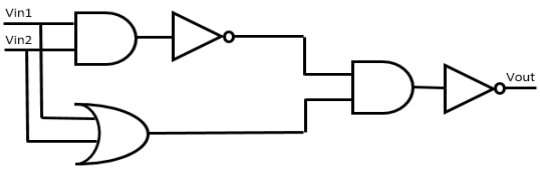

Figure 7 - XNOR gate design

C. Simulation Results

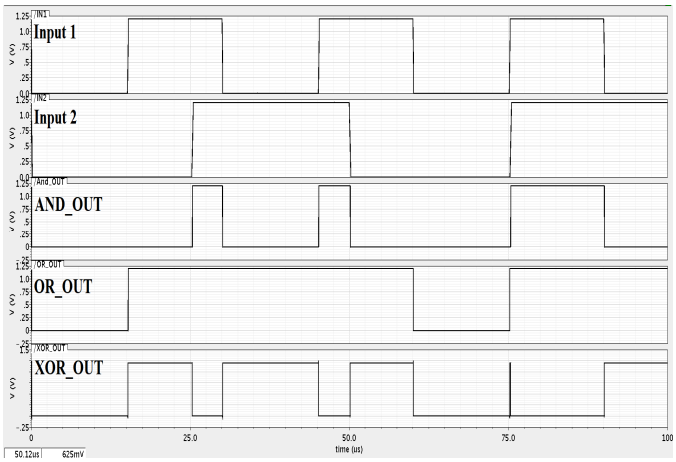

Figure 8. Transient response of AND, OR and XOR gates respectively showing all possible combinations. The output of the gates leveled using a buffer showing correct logic output.

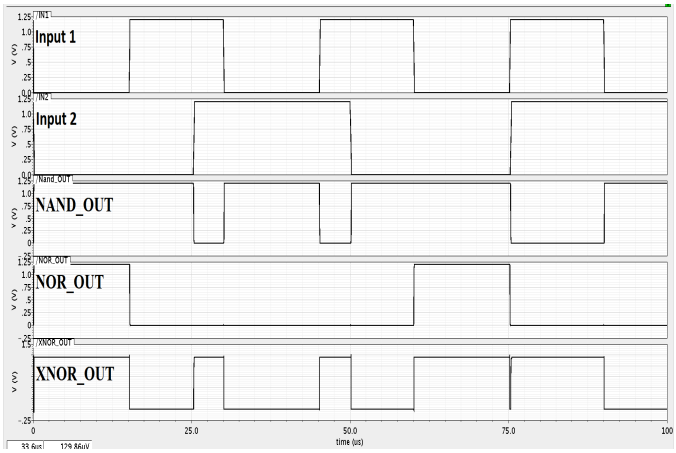

Figure 9. Transient response of NAND, NOR and XNOR gates respectively showing all possible combinations.

V. Power Dissipation Calculation

In CMOS based designs, it was proved that CMOS consume more power as it is always connected to the power supply and that is called by static power dissipation. On the other hand, memristor based designs consume no static power. However, in Hybrid CMOS memristor designs there is a static power leakage due to CMOS elements existence.For hybrid design, the power is calculated by integrating the sum of input currents across one clock cycle and multiply it by the output voltage of the circuit. The following equation can represent this method

$$P = \frac{1}{T}\int_{T}^{0} Vout\ (t) * (I_{input\ 1}(t) + I_{input\ 2}(t))\, d(t) \qquad (9)$$

The currents mentioned in the equation represent the current flows in two states, the first state is the output logic transition from high to low and back, the other state is the steady state of the output at logic high. Normally the current at transitions are significantly high with respect to the steady state current. However, the current at steady state is very small (almost zero), it cannot be neglected as the overall power consumption is already low.

There is a tradeoff between power reduction and circuit complexity as power can be reduced significantly by adding more buffering with CMOS gates. Adding buffers will reduce both static power and dynamic power, improve the fan out, and reduce the working voltage.

VI. Comparison Results

All the simulated Hybrid CMOS memristor designs and CMOS-based designs results are measured on the same set of inputs which where two square waves with different periods to ensure simulating the full functionality of each gate with the same level of supply 1.2 volts. The power calculation results is depending on the values of the output signal which means it will vary for the different input sets so we use the same input sets to get effective comparison between the methodologies.

Table 1 - Timing measurements for CMOS-based designs Tpd-HL and Tpd-LH is the propagation delay for High-to-Low and Low-To-High respectively

	Tpd-HL (nsec)	Tpd-LH (nsec)	Raising time (nsec)	Falling time (nsec)	Avg. delay (nsec)
AND	5.4	5.6	17.9	19.1	18.5
OR	11.3	15	15.34	16.7	16.02
XOR	17.4	22	123.2	99.89	111.545
NAND	5.69	5.6	111.2	101.3	106.25
NOR	12.27	12.24	119	104.6	111.8
XNOR	7.22	6.27	1.21	10	5.605

Table 2 - Power and area calculations for CMOS-based designs where number of MOSFETS indicates the area of the design in our study

	Power (nWatt)	No. of MOSFETs
AND	**144.7**	**6**
OR	**76.2**	**6**
XOR	**110**	**20**
NAND	**77.02**	**4**
NOR	**60.72**	**4**
XNOR	**131.1**	**14**

Table 3 - Timing measurements for hybrid CMOS memristor designs where Tpd-HL and Tpd-LH is the propagation delay for High-to-Low and Low-To-High respectively

	Tpd-HL (nsec)	Tpd-LH (nsec)	Raising time (nsec)	Falling time (nsec)	Avg. delay (nsec)
AND	**4**	**4.16**	**4.7**	**0.682**	**2.691**
OR	**2.5**	**1.6**	**0.069**	**5.27**	**2.67**
XOR	**16**	**18.3**	**0.096**	**0.163**	**0.129**
NAND	**44.33**	**58.24**	**0.196**	**1.6**	**0.898**
NOR	**0.443**	**0.84**	**3.145**	**0.371**	**1.76**
XNOR	**58.636**	**38.76**	**0.079**	**0.0676**	**0.0731**

Table 4 - Power AND area calculations for Hybrid CMOS memristor designs where number of MOSFETS and memristor indicate the area of the design in our study

	Power (nWatt)	No. of memristor	No. of MOSFETs
AND	**10.99**	**2**	**0**
OR	**23.42**	**2**	**0**
XOR	**12.36**	**6**	**18**
NAND	**3.56**	**2**	**2**
NOR	**1.876**	**2**	**2**
XNOR	**5.508**	**6**	**20**

VII. CONCLUSION AND FUTURE WORK

Through this paper, we simulated hybrid CMOS memristor based AND, OR, XOR, NAND, NOR and XNOR logic gates to be able to compare between this methodology and the pure CMOS-based logic gates methodology from several sides. We used TSMC 65nm in CMOS design part.

From the power consumption side, we proposed a way to measure it for the pure memristor-based designs and the hybrid CMOS memristor based designs. The pure memristor based designs are AND and OR gates while the hybrid CMOS memristor based designs are the rest of the simulated gates.

We conclude that the hybrid CMOS memristor methodology and the pure memristor based methodology are more effective than the pure CMOS-based designs as Hybrid CMOS memristor methodology doesn't need all time presence of power supply unlike CMOS based methodology which needs a power supply voltage differs from the input voltages.

The Hybrid methodology is also more sensitive to input changes than CMOS designs and this leads to the need of waiting some time until the output settle in order to avoid dynamic hazards which makes CMOS designs are faster than Hybrid designs, it is concluded from the obtains results in Table 1 and Table 3 which say that the propagation delay in Hybrid CMOS designs can be greater than pure CMOS designs based on the input values however the average delay of Hybrid CMOS memristor designs is always less than the obtained delay from pure CMOS based designs.

From area point of view, the current threshold of memristor model is directly proportional to area. As the used memristor model has no current threshold it is supposed to have less area than the other models. Also, we can indicate the area of the different methodologies from number of devices used in each design according to the complexity of the design. From the result of the analysis, we can see that the hybrid CMOS memristor based logic gates are effective for power consumption and sensitivity point of views compared to TSMC 65 nm CMOS-based designs.

In addition to gates characteristics comparison, we can also conclude that VTEAM model is more effective in digital design than TEAM model-based designs as the obtained results are better than - in power consumption side - the results mentioned in this paper [9] which simulates using TEAM model and CMOS 180 nm process technology.

As the Hybrid CMOS memristor design methodology is effective in many sides we plan to use it to simulate more complex digital designs and adapt this methodology to get the most effectiveness of this methodology in the digital design field.

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