FPGA Implementation of Cyclostationary Feature Detector for Cognitive Radio OFDM Signals

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Abstract— **Spectrum sensibility is the predominant function in CR designer to detect the spectrum holes of Primary radio, so it's astringent and complex task. The spectral sensor must have entire awareness about spectrum environment with a trivial delay and adequate complexity. The cyclostationarity of OFDM signals offer some statistics that will determine the status of the spectrum. Therefore, it's reliable at low S/N ratio. In this paper, CORDIC scheme is used to design a Spatial Sign Function (SSF) and complex exponential for Implementation of Cyclostationary Feature Detector. Therefore, the design complexity can be minimized by reducing the number of multipliers. Also, the system efficiency can be improved. For simulation and testing, Quartus 15 is used for Altera high-speed Arria V GZ kit.**

Keywords— Spatial Sign Function; CORDIC; OFDM signals; Cyclostationary - Arria V GZ;

I. INTRODUCTION

Cognitive Radios using the void bands of the Primary radio to enhance the efficiency of the spectrum. Cognitive radio (secondary radio) is smart reconfigurable radio system which opportunistic a licensed spectrum to beat on the lacking of existing spectrum [1, 2]. Reliability of Cognitive Radio is needed to identify automatically of an unoccupied licensed spectrum by scanning the spectrum environment. This task can be performed by Spectrum Sensing which is a main Cognitive radio module. There are parameters that reduce the efficiency of Sensing like noise, shadowing, multipath fading etc., which must be overcoming by a complex spectrum sensing. Spectrum sensing has many types like Energy Detector, Cyclostationary Detector and Matched Filter Detector etc. [2, 6, 11]. The differentiable between these sensing types relying on:

- Sensing time, low sensing time increase the time obtainable for secondary data communication.
- Complexity, energy consumption by secondary radio battery not only depending on the environment of the radio but also the complexity of the scanning type.
- Reliability, the sensing type performance must be preventing the degradation of the system at low Signal to Noise ratio (S/N).

Orthogonal Frequency Division Multiplexing (OFDM) is a digital modulation using in high data rate [3]. OFDM has invulnerability to multipath fading because of using a cyclic prefix (CP). The OFDM symbols contain a pilot subcarrier that is used for the phase of noise and offset of frequency compensation after demodulation carried out. These redundancy sources provide regularities into the signal statistics which can be taken for detection, especially at lower Signal to Noise Ratio (SNR). Because of the advantages of OFDM, it has found widespread use in different commercial communications IEEE standards 802.11g/n [4] and LTE [5].

Spectrum sensing can be carried out using Energy detectors (EDs) [6,7], that are ideal theory for spectrum sensing as it has a simple design but it is not convenient for application which demands a signal detection at low SNR, as it's very susceptible to error in the noise variance estimation, regardless of the number of samples, otherwise, the Matched Filter Detector [8] is an optimum detector for known signals, so it's more complex and hard to design.

Cyclostationary signals have statistical properties that vary periodically with time which can be seen as many interleaved stationary processes, such as mean and autocorrelation [3, 9, 10, 15]. OFDM symbols with a cyclic prefix provide this stationarity for detection, meanwhile, autocorrelation function. Reducing the complexity of Cyclostationary feature detector is acceptable to enhance the sensing time and reduce the consumption power, this reduction comes from choosing the Altera Arria V GZ kit is superior and using CORDIC scheme to decrease the multiplication complexity of Spatial Sign Function (SSF) instead of FFT [7, 11, 12, 14]. CORDIC is well convenient for implementation, as it depends on add and shift operation. Many computing tasks like exponential, hyperbolic, complex multiplication, and square root, etc. can be implemented using CORDIC algorithm [12].

The rest of paper is organized as follows: Section II shows OFDM Cyclostationarity Signals, Section III explains Spatial Sign Cyclic Correlation Estimator, Section IV presents the Hypothesis Testing, Section V introduces the proposed implementation for cyclostationary detector, results discussions in Section VI. Finally, Conclusions are made in section VII.

II. OFDM CYCLOSTATIONARITY SIGNALS

$x(t)$ is a signal named cyclostationary in wide-sense, when mean and autocorrelation are cyclic, such that

$$m_x(t+T_0) = m_x(t) \quad (1)$$

$$R_{xx}(t,\tau) = R_{xx}(t+T_0,\tau) \quad (2)$$

Where τ is the lag, T_0 is the cyclic period, m_x is the mean value and R_{xx} is the autocorrelation function, by taking the Fourier Series for Eq. (2).

$$R_{xx}(t,\tau) = \sum_\lambda R_x^\lambda(\tau)e^{j2\pi\lambda t} \quad (3)$$

Where λ is the cyclic frequency and used to identify the transmitted signals [13], and cyclic autocorrelation function $R_x^\lambda(\tau)$ denotes by:

$$R_x^\lambda(\tau) = \lim_{T\to\infty}\frac{1}{T_0}\int_{-T/2}^{T/2} R_x(t,\tau)e^{-j2\pi\lambda t} \quad (4)$$

The periodicity of $R_x(t,\tau)$ in time t with duration T_0 , rewritten equation (4) [13] we get:

$$R_x^\lambda(\tau) = \frac{1}{T}\int_{-T/2}^{T/2} R_x(t,\tau)e^{-j2\pi\lambda t}\, dt\left(\frac{\pi}{2}-\theta\right) \quad (5)$$

Where T is the total observation period. By converting CAF into a frequency domain using Fourier transform we obtained Spectral Correlation Function (SCF)

$$S_x^\lambda(f) = \int_{-\infty}^{\infty} R_x^\lambda(\tau)\, e^{-j2\pi\lambda t}d\tau \quad (6)$$

Normalized the correlation function between $f+\frac{\lambda}{2}$ and $f-\frac{\lambda}{2}$ over Δt duration, so SCF can be described by [14]:

$$S_x^\lambda(f) = \lim_{T\to\infty}\lim_{\Delta t\to\infty}\frac{1}{\Delta t}\int_{-\frac{\Delta t}{2}}^{\frac{\Delta t}{2}}\frac{1}{T}X_T\left(t,f+\frac{\lambda}{2}\right) X_T^*\left(t,f+\frac{\lambda}{2}\right)dt \quad (7)$$

The advantage of SCF in spectrum sensing is insensitive to noise, because of the noise is a stationary process, so the SCF of noise $S_x^\lambda(f)$ is zero when $\alpha = 0$. To detect the cyclic frequency and omit the channel effect, a normalized SCF called Spectral Coherence Function (SOF) is produced [14].

III. SPATIAL SIGN CYCLIC CORRELATION ESTIMATOR

The cyclic prefix supports robust Cyclostationary effects making it a perfect for estimation in 802.11p primary users, furthermore, the CAF supports effective computation by calculating the cyclostationary properties of the cyclic prefix. Regrettably, the complexity of inversion and estimation for the signal noise covariance matrix is needed in the detection method. Avoiding estimation of the noise probability density function and implementation of Spatial Sign Cyclic Correlation Estimator (SSCCE) are required to save hardware and power than traditional technique [7], therefore the test statistic is normalized by CORDIC.

The SSCCE detector [16] depends on the monitoring components of the cyclic frequency in the autocorrelation of the SSF for input data. If the data signal is $x(n)$ then the SSF is studied as: -

$$s(n) = \begin{cases}\frac{x(n)}{|x(n)|}, & x(n) := 0\\ 0, & x(n) = 0\end{cases} \quad (8)$$

Therefore, the SSCCE can be calculated as introduced in [16]

$$\hat{R}(\tau,\alpha) = \frac{1}{N}\sum_{n=0}^{N-1} s(n)\, s^*(n+\tau)e^{-j\frac{2\pi\alpha n}{N}} \quad (9)$$

Where, N is the number of observations, α is the cyclic frequency, and τ is a discrete time delay. The SSF nonlinearity does not influence the autocorrelation periodicity for circularly symmetric complex Gaussian processes a precise paradigm for systems of OFDM. This result extends to spatial sign cyclic covariance at nonzero cyclic frequencies. So, the influence function residue bounded uniformly.

The SSCCE covariance function for white noise $W[n]$ can be computed as

$$\sum_{R_S^\alpha(\tau)} = E[|S(W[n])|^2|S(W[n+\tau])|^2] \quad (10)$$

The SSF normalization feature guarantee that:

$$E[|S(W[n])|^2|S(W[n+\tau])|^2] = 1 \quad (11)$$

IV. HYPOTHESIS TESTING

The hypotheses test stated that:

$$H_0 : x(t) = n(t)$$

$$H_1 : x(t) = s(t) + n(t) \quad (12)$$

Where, $s(t)$ is the transmitted primary signal, $x(t)$ is the received signal, and $n(t)$ is a noise process.

A vector of the estimated SSCCE functions for different lag is shown as

$$\widehat{r_s} = [\widehat{R_S^\alpha}(\tau_1),\ldots,\widehat{R_S^\alpha}(\tau_k)] \quad (13)$$

The test statistic can be summed simply as

$$T(\widehat{r_s}) = \frac{N}{2}\left|\widehat{R_S^\alpha}(\tau_1) + \widehat{R_S^{\alpha\phi}}(\tau_k)\right|^2 \quad (14)$$

V. THE IMPLEMENTATION of CYCLOSTATIONARY DETECTOR

The cyclostationary scheme is divided into multiple designs to simplify the implementation process, which result in increasing design reusability. Fig.2. shows the block diagram of cyclostationary detector. All blocks will be explained in details. Timing OFDM PHY Modulation Parameters for 802.11a are showed in table 1.

A. The SSF Implementation

The SSF calculates the vector input signal, as follows:

$$S(x[n]) = \sqrt{Re(x[n])^2 + Im(x[n])^2} \qquad (15)$$

The square root function and the two square terms make this method more complex and expensive in digital hardware logic. Avoiding this operation obtained by using the CORDIC scheme by obtaining the phase of the Cartesian input (Vector CORDIC), after that converting the angle to Cartesian again (Rotation CORDIC) with a normalized magnitude as shown in Fig.1.

B. Shift Register

In autocorrelation function calculation, the Shift Register dual lag (with $\tau = 64\, samples$) is designed by block RAM resources, that are available in FPGA. More resources and power intensive can be avoided because of using flip-flop-based shift registers. The output of the shift register is zero lag component, lag component and a dual lag component which are fed into complex multipliers to generate the autocorrelation coefficient are shown in Fig.1.

C. Numerically Controlled Oscillator

The cyclic down conversion estimation of the autocorrelation coefficients demands a multiplication by a pair of complex exponentials. We can use the NCO from IP core in Quartus to implement the complex exponential.

D. Moving Average Filter

Regrettably, the computation of the SSCCE test statistic output needs all *N* samples based on the threshold value before making the decision. Enhancing the detection algorithm, by replacing the simple average with a moving average, which is easy to be implemented in digital logic. The SSCCE implementation sets the maximum number of samples to 1024 samples. Scaling the data length after addition and multiplication is required to maintain a constant bus width.

E. Multiplier

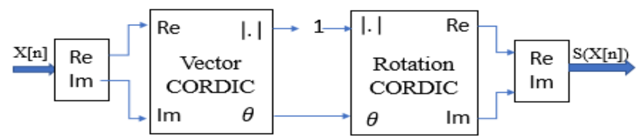
The calculation of the autocorrelation coefficients in the SSCCE design demands complex multiplier and using real multipliers for the squaring operation. Fortunately, most modern FPGAs contains embedded fast multipliers.

F. Decision

The threshold is calculating according to the desired value

$$\lambda = F_{\gamma}^{-1}(1 - P_{FA}) \qquad (16)$$

Where, F_{γ}^{-1} is the inverse gamma cumulative distribution function with scale and shape factor k equal to one [17], and P_{FA} is the probability of falsely detecting the primary signal when the primary signal is actually absent.



$$S(x) = \cos\theta + j\sin\theta \quad and \quad \theta = \tan^{-1}\frac{Im}{Re}$$

Fig.1. the block diagram of implementation SSF using CORDIC

TABLE I. TIMING OFDM PHY MODULATION PARAMETERS FOR 802.11a

Parameter	***Value***
Total subcarriers N_{ST}	52
Data subcarriers N_{SD}	48
Pilot subcarriers N_{SP}	4 (subcarriers ±21, ±7)
Subcarrier Frequency Spacing F_{SP}	312.5 KHz (20M/64)
Symbol Duration T_{SYM}	4 µs (T_{GI} +T_{FFT})
Data Interval Time T_{DATA}	3.2 µs (1/F_{SP})
Guard Interval (GI) Time T_{GI}	0.8 µs (T_{FFT}/4)
IFFT/FFT Period T_{FFT}	3.2 µs (1/F_{SP})
Preamble $T_{PREAMBLE}$	16 µs (T_{SHORT} +T_{LONG})
Short Training Sequence T_{SHORT}	8 µs (10xT_{FFT}/4)
Long Training Sequence T_{LONG}	8 µs (T_{GI2} + 2xT_{FFT})
Training symbol GI T_{GI2}	1.6 µs (T_{FFT}/2)

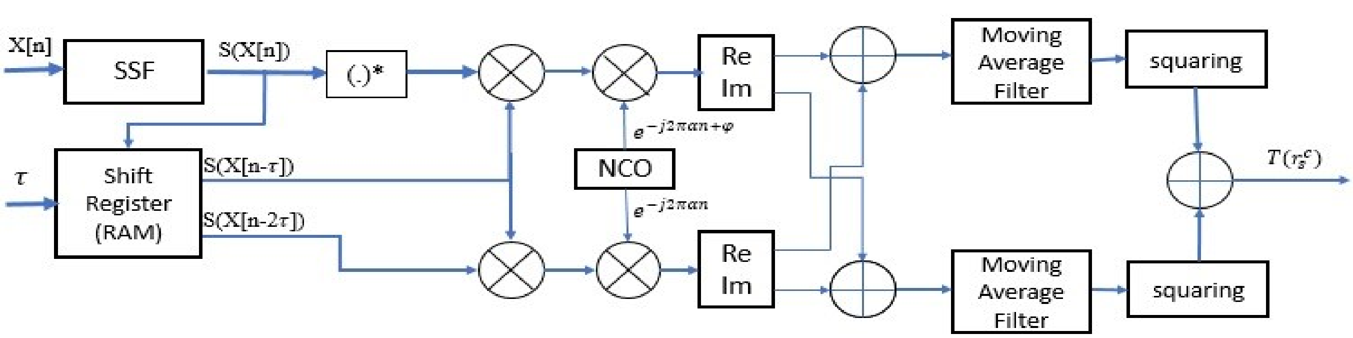


Fig.2 The block diagram of cyclostationary feature detector based on SSCCE

V. RESULTS AND DISCUSSION

In this work, the hardware platforms of cyclostationary feature detector based on SSCCE are performed. The RTL codes are written by a high-speed hardware description language (VHDL). Quartus 15 is used to carry out the designs on Arria V GZ FPGA Kit. The simulations are done using Modelsim 10.3d and verified the results by the Matlab software. Table II shows the implementation cost per design block in terms of Logic Elements, Block Random Access Memories (BRAMs), Flip Fops and DSP blocks for 8-bit with 6-bit fraction.

TABLE II. RESOURCE UTILIZATION OF THE CYCLOSTATIONARY IMPLEMENTATION

	Logic Elements	Flip Flops	Block RAM Bits	No.of Multipliers
SSF	226	425	0	0
Shift Register	40	34	1024	0
NCO	217	456	0	0
Moving Average	190	63	36436	0
Real Multiplier	0	18	0	2
Complex Multiplier	0	189	0	8
Total Resources	664	1185	37888	10

TABLE III. RESULTS COMPARISON

	No. of DSP Multiplier
REF [5]	28
REF [18]	14
Proposed design	10

The total resources of the proposed design are less than 1% from overall kit resources, which means that the resources are efficiently used. The total number of the logic elements are quite low because of the add operation is the predominant operation. The block RAM is the largest resources, which is driven foremost by the moving average filter. In this paper, the exponential signal generation from NCO design depends on the Rotation CORDIC from IP Quartus core, therefore, SSF and NCO take more Flip-Flops because of the shift operation in CORDIC algorithm. Table III shows the multipliers comparison with the related works, the total number of multipliers of the proposed design is 10 multiplier this leads to less complexity of the design, and it has fewer logic elements with respect to using FFT.

VII. CONCLUSIONS

This paper has presented an improved CORDIC test for SSCCE Detector that used for OFDM identification in spectrum sensing. The cyclostationary sensing algorithm has a complex computation like matrix inversion and FFT that can be overcome by using CORDIC which is suited for hardware implementation in SSF and NCO design. With these modifications, a smaller number of multipliers and fewer logic gates have been used. Furthermore, the proposed design has shown in lowering the computational complexity, that makes it convenient in practical application.

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