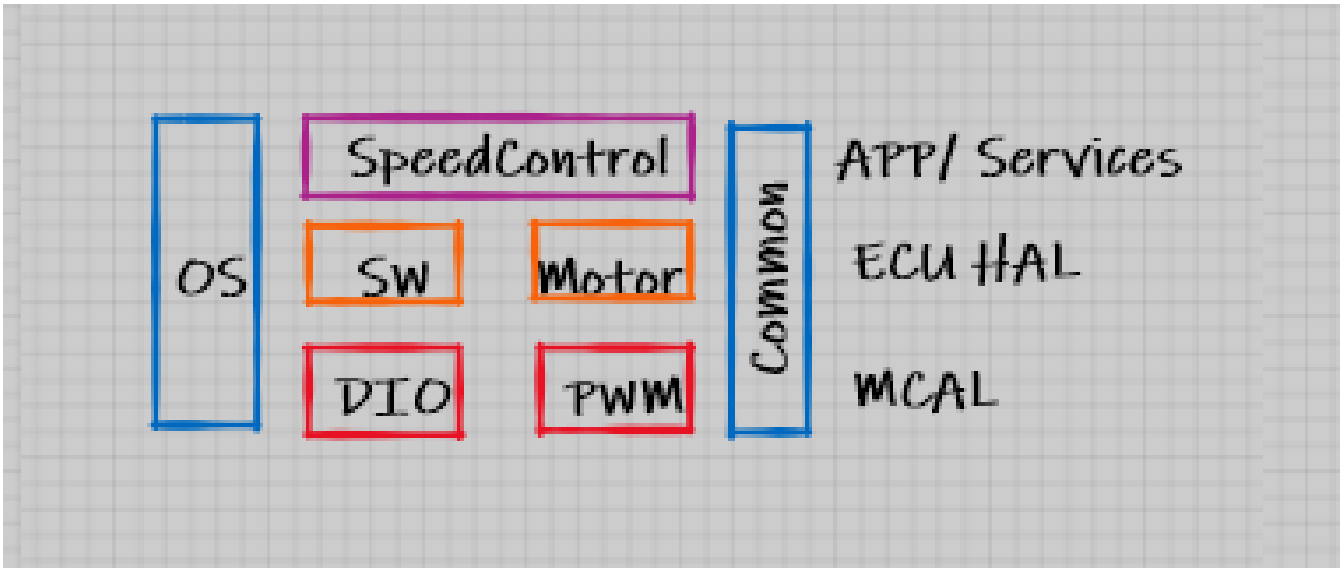
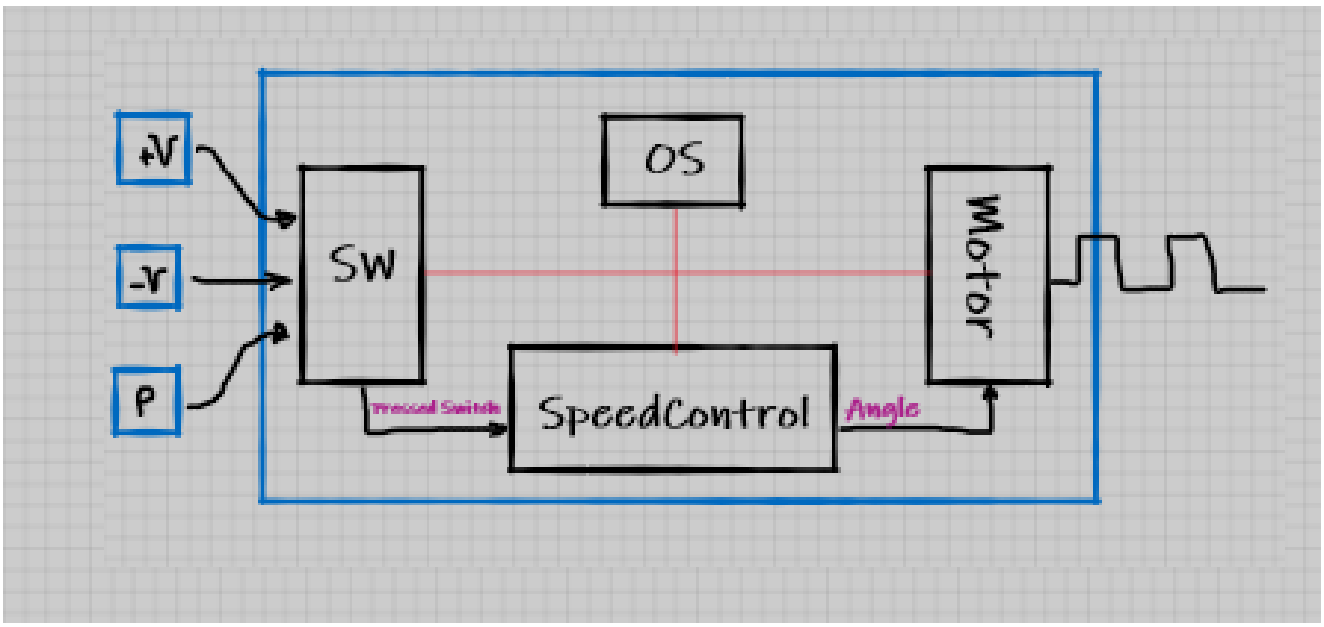
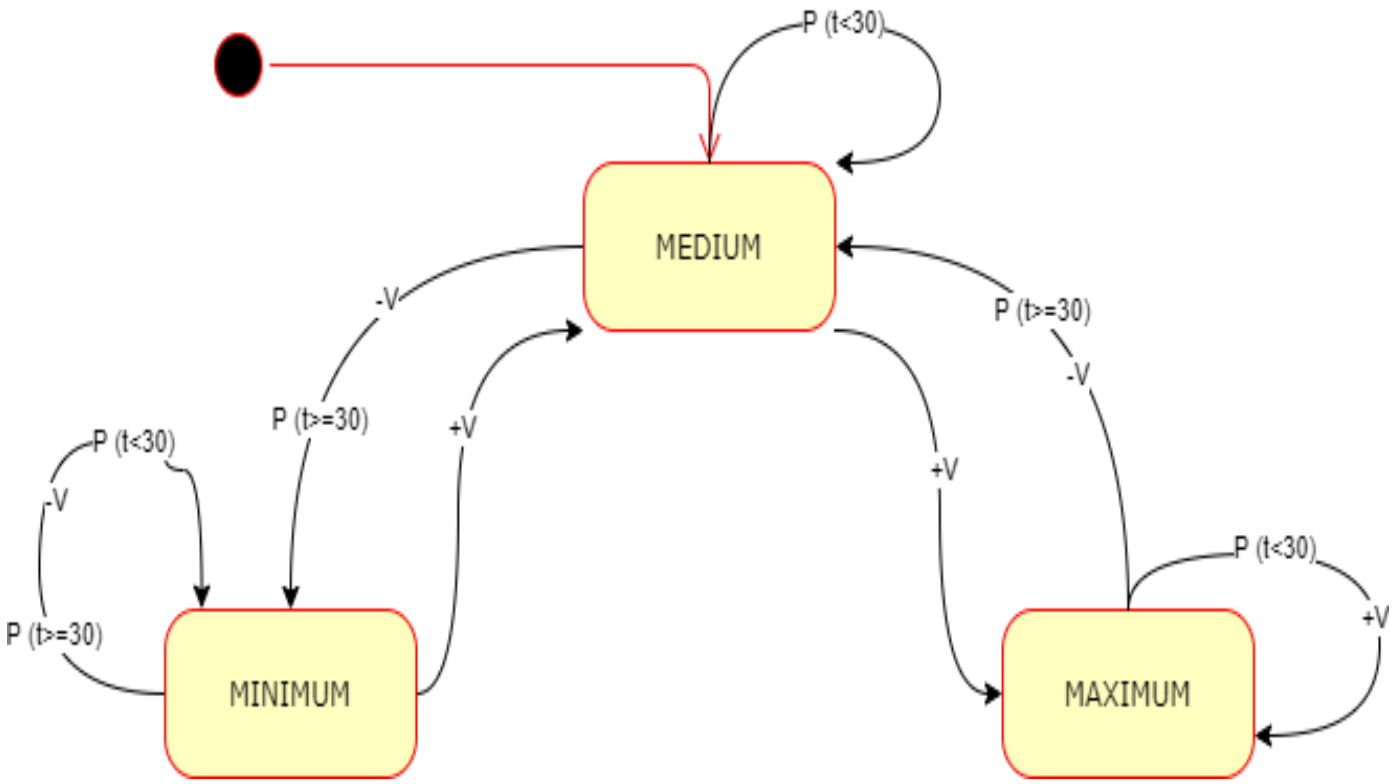
Static Architecture



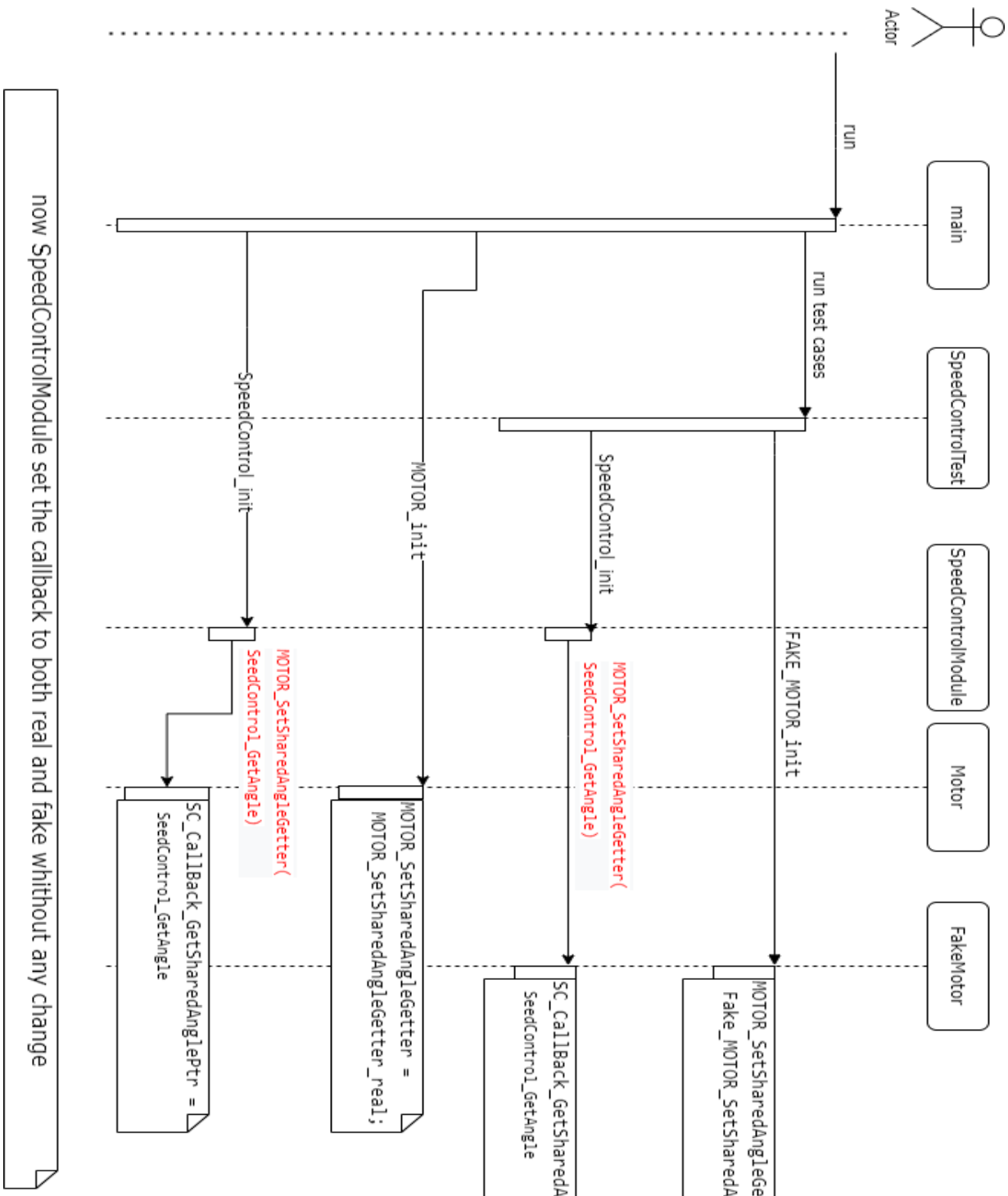


Dynamic Design

State machine for the Module:



Sequence diagram for setting the callback in the real and fake motor to get the angle:



APIs for modules

- Switch:
  - SWITCH_init
  - SWITCH_update
  - SWITCH_GetPressedSwitch
- SpeedControl
  - SpeedControl_init
  - SpeedControl_update
  - SpeedControl_GetSpeedState
  - SpeedControl_GetAngle
- Motor:
  - MOTOR_init
  - MOTOR_update
  - MOTOR_SetSharedAngleGetter
- OS:
  - YO_eInit
  - YO_vCreateTask
  - YO_vStartScheduler

Approach 1: Timing Analysis

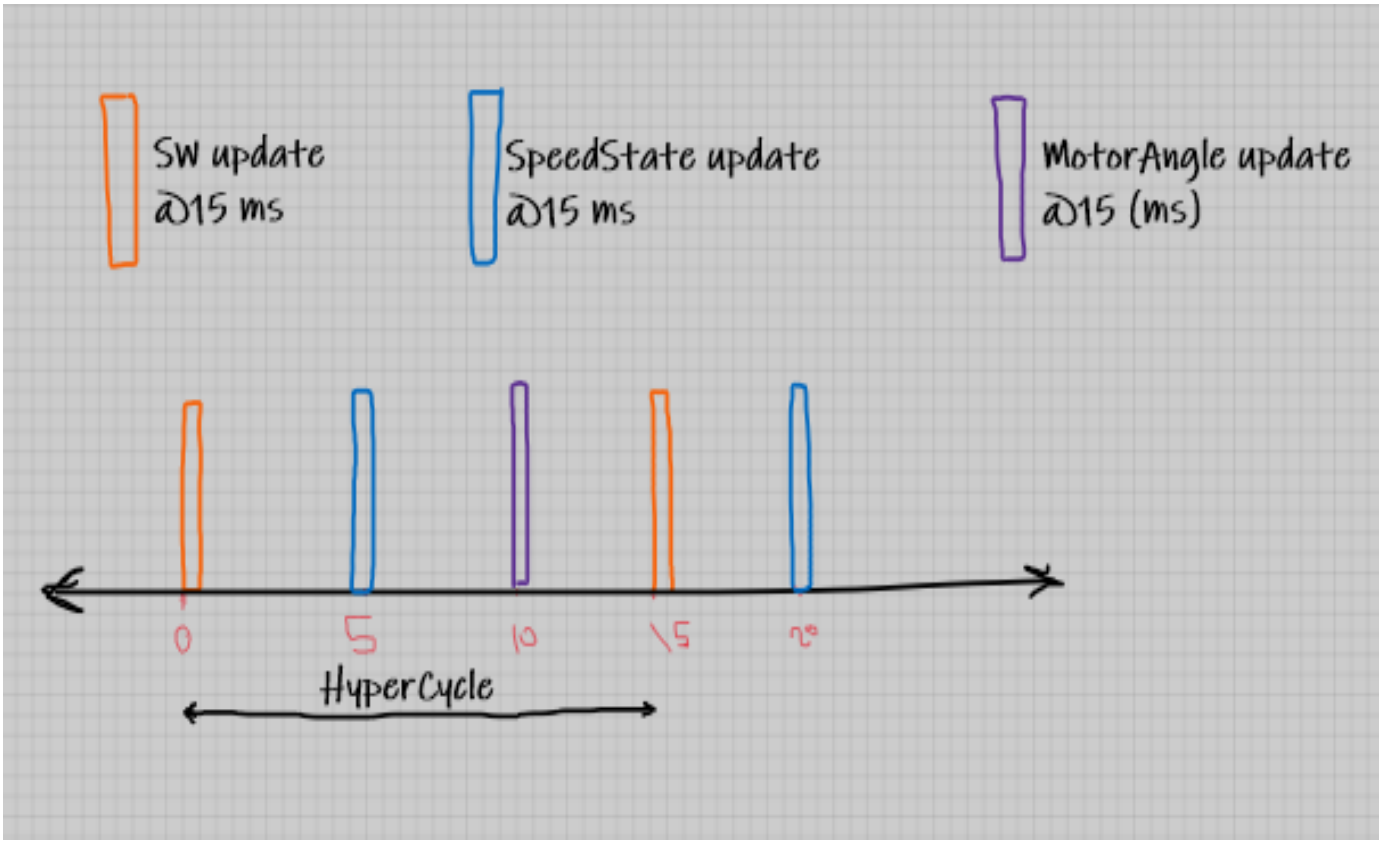
Task	Actions	BCET (ms)	WCET(ms)	Period of Action (ms)	Period of task (ms)
SW	Update samples	~0	~0	15	15
	Update SW state	~0	~1	15	
SC		~0	~1	15	15
MU		~0	~1	15	15
				Tick (ms)	5
				Major Cycle (ms)	15

Average CPU load = (3)/15= 20%

Max sleep time = 4ms

Adv: Faster

Approach 1: Schedulability Check



Approach 2: Timing Analysis

Task	Actions	BCET (ms)	WCET(ms)	Period of Action (ms)	Period of task (ms)
SW	Update samples	~0	~0	10	10
	Update SW state	~0	~1	10	
SC		~0	~1	20	20
MU		~0	~1	20	20
				Tick (ms)	10
				Major Cycle (ms)	20

Average CPU load = (4)/20= 20%

Max sleep time = 9 ms

Adv: longer life time (! maybe)

Approach 2: Schedulability Check