

CMPN201

Microprocessors 1

# Team Members:

* Khaled Mamdouh Mohamed Fadel 1190321
* Anas Sherif Elkheshen 1190375
* Seif Mohamed Albaghdady 1190119
* Ahmed Maher Ahmed 1190260
* Shadi Gamal Elsayed 1180570

## Submitted to: **DR.Khalid AlSoradi, Eng.Aya**

|  |  |  |  |
| --- | --- | --- | --- |
| Feature | Working or not | Known Bugs | Copied or not |
| NOP | Working | None | Not Copied |
| CLC | Working | None | Not Copied |
| AND with immediate mode | Working | None | Not Copied |
| AND with register addressing mode | Working | None | Not Copied |
| AND with direct addressing mode | Working | None | Not Copied |
| AND with register indirect addressing mode | Working | None | Not Copied |
| MOV with immediate mode | Working | None | Not Copied |
| MOV with register addressing mode | Working | None | Not Copied |
| MOV with direct addressing mode | Working | None | Not Copied |
| MOV with register indirect addressing mode | Working | None | Not Copied |
| ADD with immediate mode | Working | None | Not Copied |
| ADD with register addressing mode | Working | None | Not Copied |
| ADD with direct addressing mode | Working | None | Not Copied |
| ADD with register indirect addressing mode | Working | None | Not Copied |
| ADC with immediate mode | Working | None | Not Copied |
| ADC with register addressing mode | Working | None | Not Copied |
| ADC with direct addressing mode | Working | None | Not Copied |
| ADC with register indirect addressing mode | Working | None | Not Copied |
| PUSH | Working | None | Not Copied |
| POP | Working | None | Not Copied |
| INC | Working | None | Not Copied |
| DEC | Working | None | Not Copied |
| MUL register | Working | None | Not Copied |
| MUL register addressing | Working | None | Not Copied |
| MUL direct addressing | Working | None | Not Copied |
| DIV register | Working | Overflow for large numbers | Not Copied |
| DIV register addressing | Working | Overflow for large numbers | Not Copied |
| DIV direct addressing | Working | Overflow for large numbers | Not Copied |
| IMUL register | Working | None | Not Copied |
| IMUL register addressing | Working | None | Not Copied |
| IMUL direct addressing | Working | None | Not Copied |
| IDIV register | Working | Overflow for large numbers | Not Copied |
| IDIV register addressing | Working | Overflow for large numbers | Not Copied |
| IDIV direct addressing | Working | Overflow for large numbers | Not Copied |
| ROR with immediate addressing | Working | None | Not Copied |
| ROR with register | Working | None | Not Copied |
| ROR with register addressing | Working | None | Not Copied |
| ROR with direct addressing | Working | None | Not Copied |
| ROL with immediate addressing | Working | None | Not Copied |
| ROL with register | Working | None | Not Copied |
| ROL with register addressing | Working | None | Not Copied |
| ROL with immediate addressing | Working | None | Not Copied |
| SHR with immediate addressing | Working | None | Not Copied |
| SHR with register | Working | None | Not Copied |
| SHR with register addressing | Working | None | Not Copied |
| SHR with direct addressing | Working | None | Not Copied |
| SHL with immediate addressing | Working | None | Not Copied |
| SHL with register | Working | None | Not Copied |
| SHL with register addressing | Working | None | Not Copied |
| SHL with direct addressing | Working | None | Not Copied |
| RCR with immediate addressing | Working | None | Not Copied |
| RCR with register | Working | None | Not Copied |
| RCR with register addressing | Working | None | Not Copied |
| RCR with direct addressing | Working | None | Not Copied |
| RCL with immediate addressing | Working | None | Not Copied |
| RCL with register | Working | None | Not Copied |
| RCL with register addressing | Working | None | Not Copied |
| RCL with direct addressing | Working | None | Not Copied |