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VLSI 2

32-point FFT

Submitted by:

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Assumptions

- **Input is 8 bits 1 for sign 3 for integer and 4 for fraction**
- **The representation of the negative input is the 2's complement**
- **Before the input get to the designed 32point FFT it get padded to 24 bits 1 for sign 11 for integer and 12 for the fraction without effecting the 2's complement representation**
- **We assumed the pipeline to work with 25MHz instead of 20MHz to have full utilization of the MAC blocks will gaining more speed noting that it will also work properly if the pipeline frequency is 20MHz**

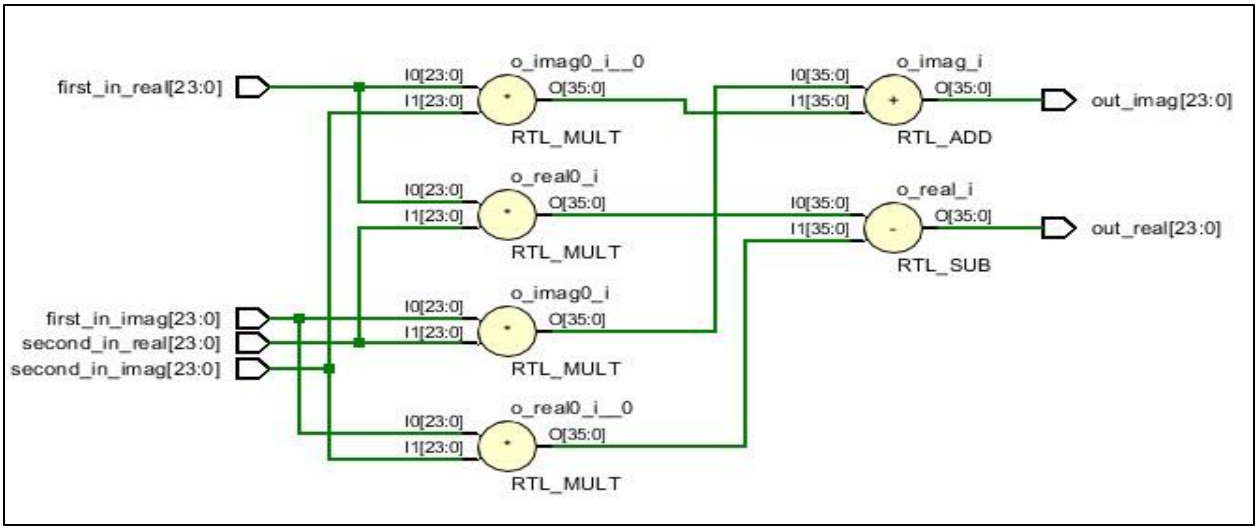
Note: this design can handle also complex inputs not only real

Design Methodology

For this design we tried as much as possible to isolate the modules apart from each other and we adopted a hierarchy work flow to ensure each module is working correctly and to ease the debugging steps noting also that we didn't use glue logic in this project.

Design flow

- **First we designed a complex multiplier as seen in figure(1)**
- **then we design a MAC module to evaluate 2 outputs of the FFT given 2 inputs and the twiddle factor as seen in figure(2)**
- **then we used this module as a core to build a module called MAC Controlled that can use the high speed of the MAC to preform 4 evaluations steps in one clock by using 3 MUX at the input and 2 REGISTERS files at the output controlled by a counter and a decoder as seen in figure(3)**
- **then for the TOP design we used 4 MAC blocks at each layer and a REGISTER BANK to hold the value between the layers as seen in figure(4)**



[2]

Figure 1: Complex multiplier

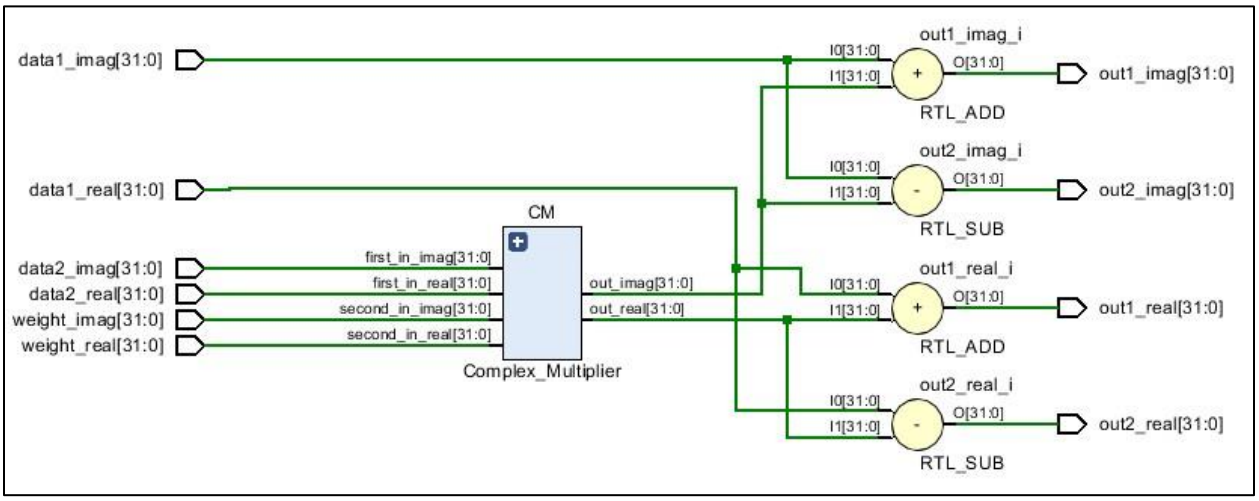


Figure 2: MAC

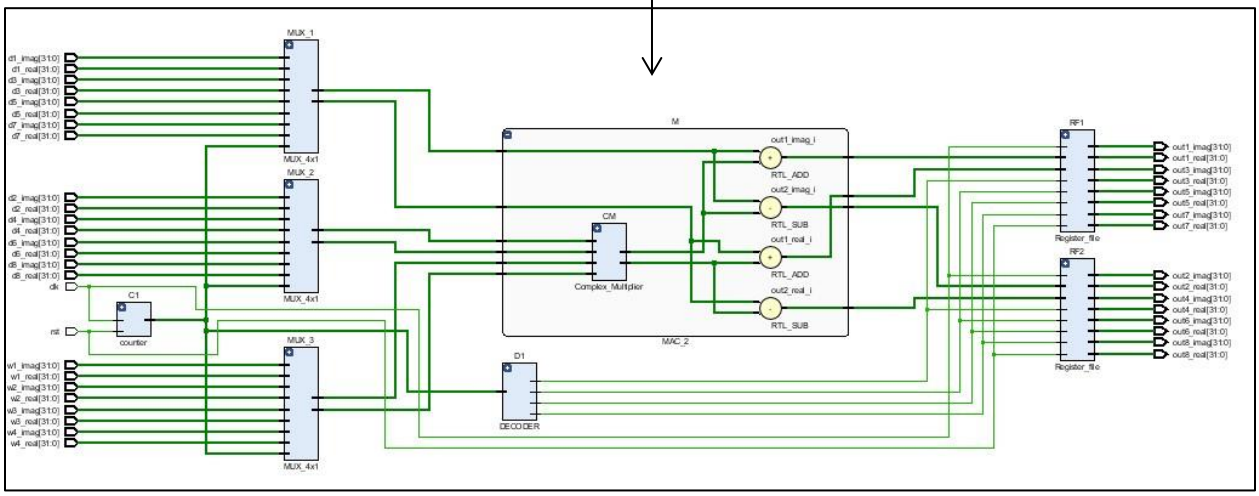


Figure 3: MAC controlled

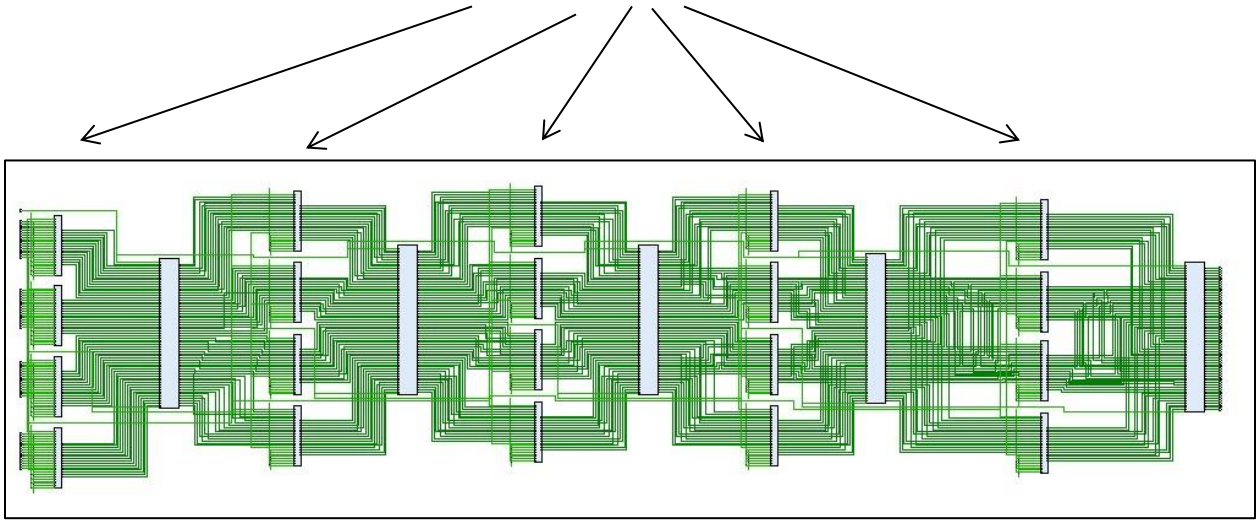


Figure 4: TOP

Simulation INPUTs

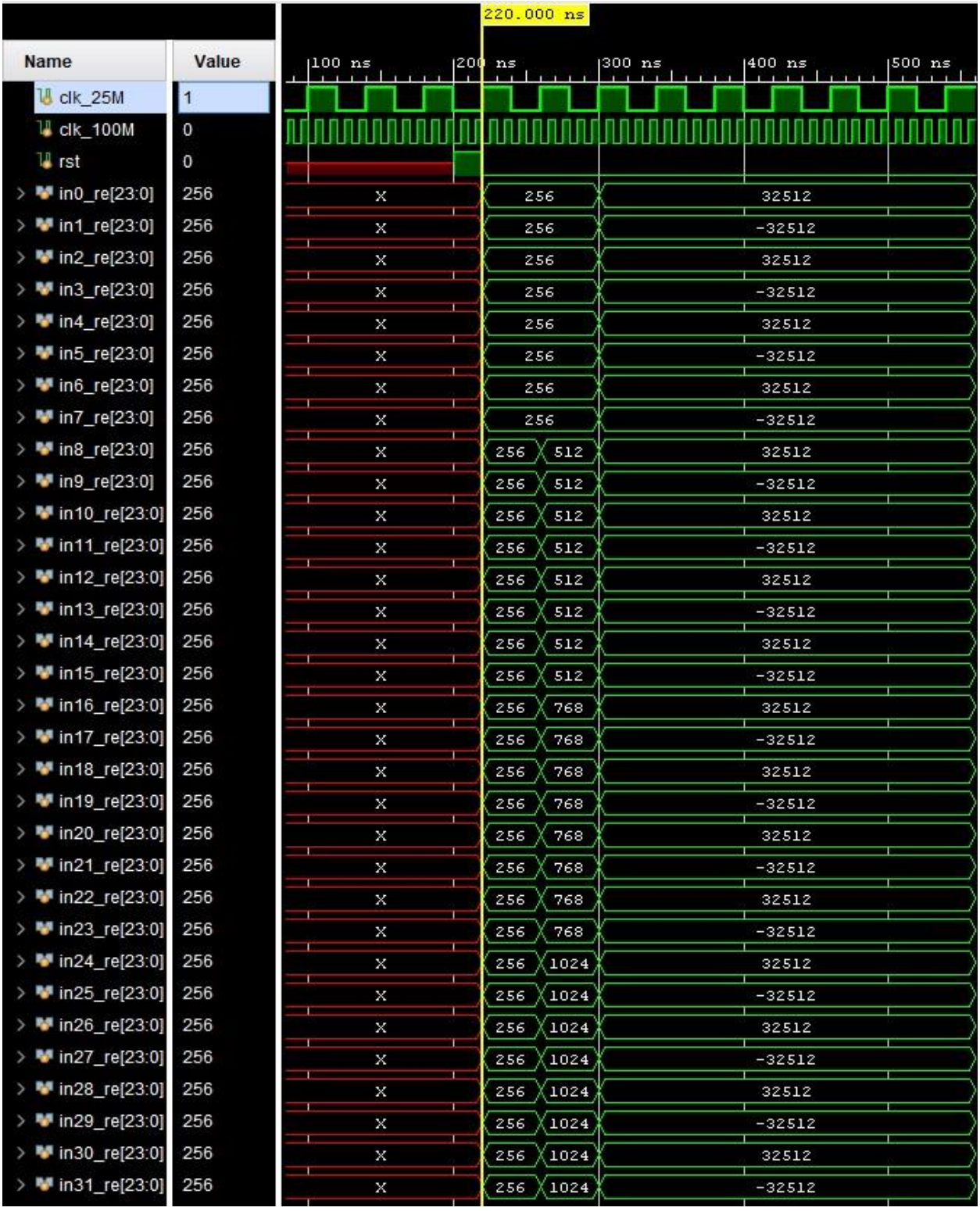


Figure 5: real input part

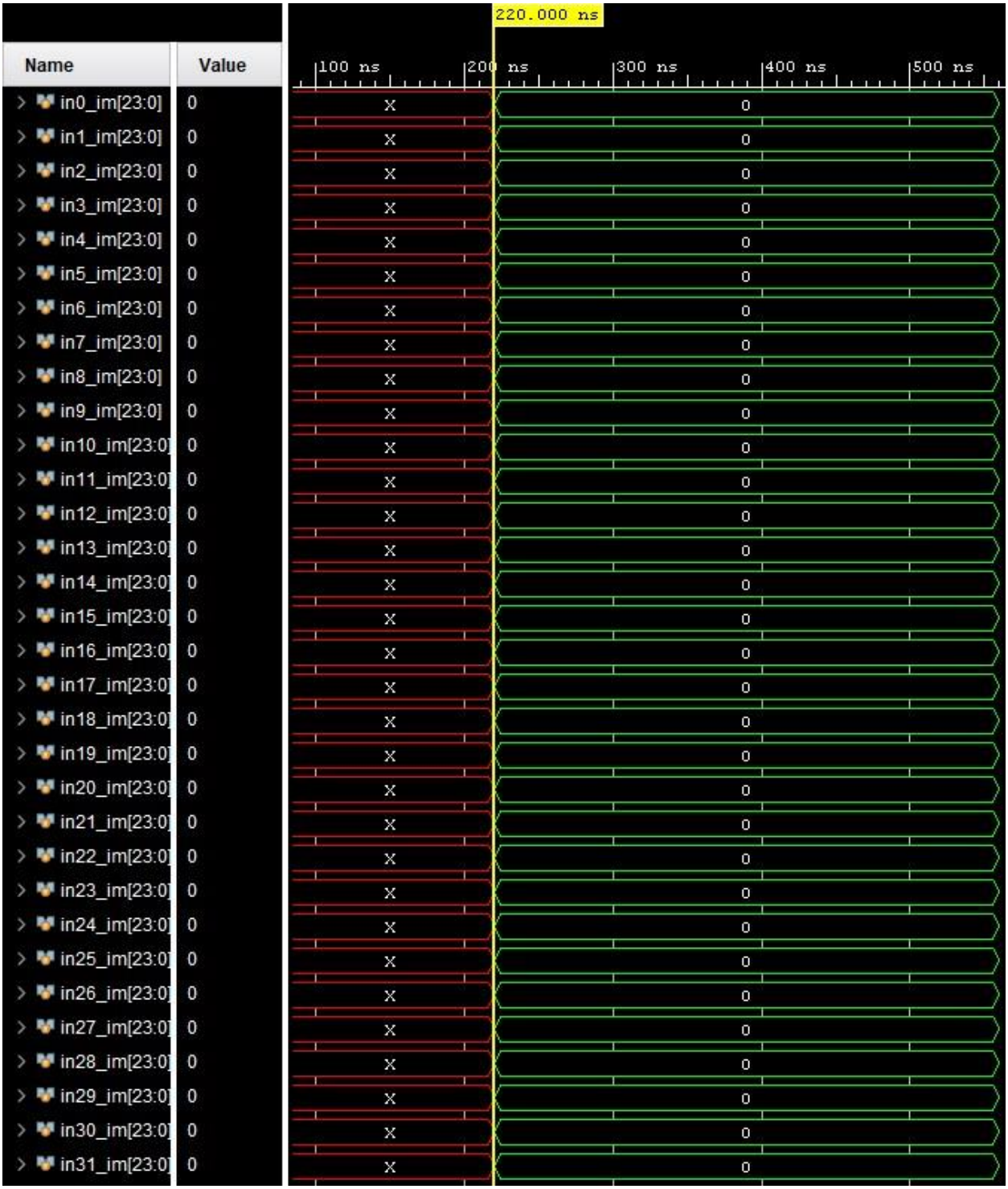


Figure 6: imag input part

Behavioral simulation OUTPUTs

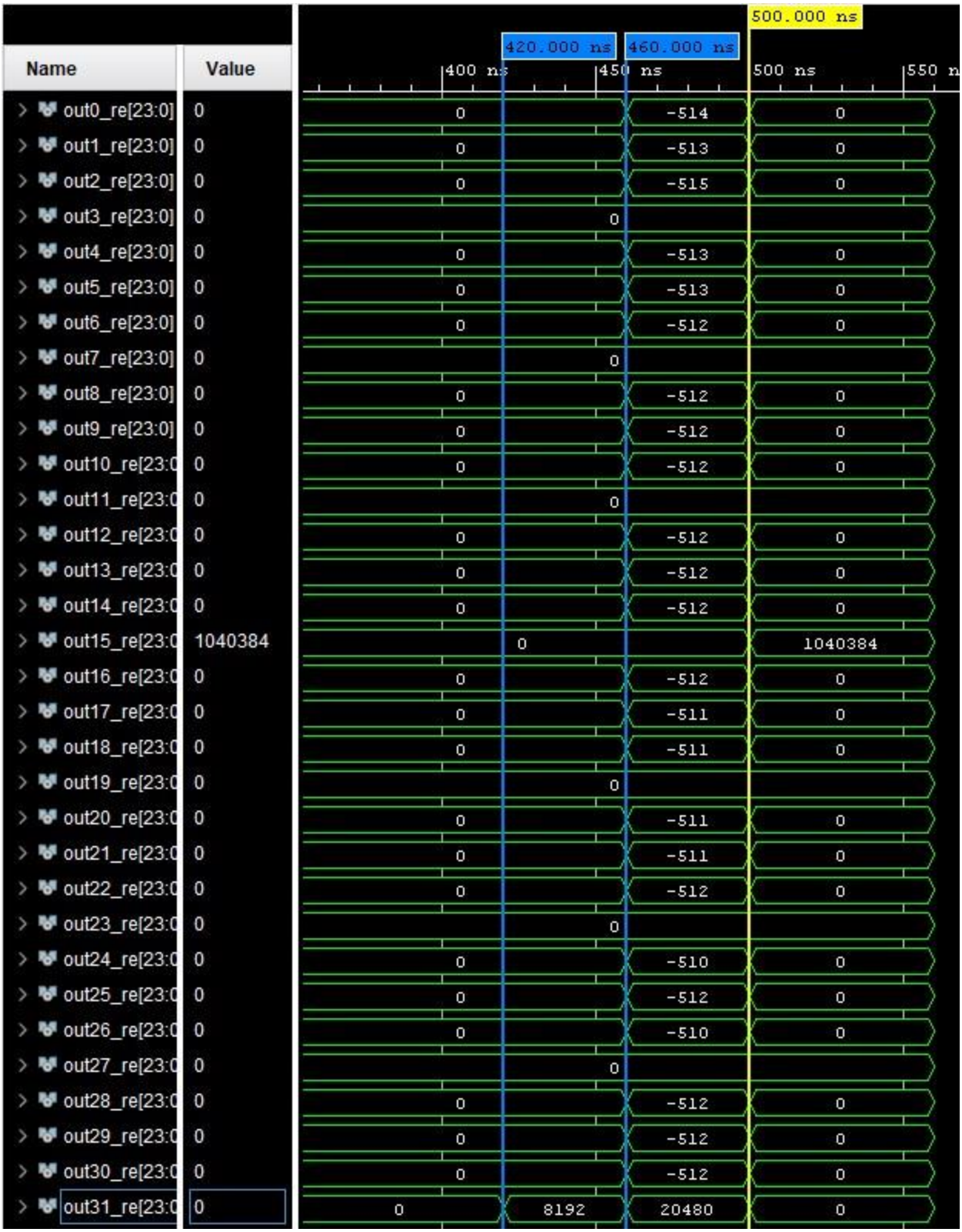


Figure 7: real output part

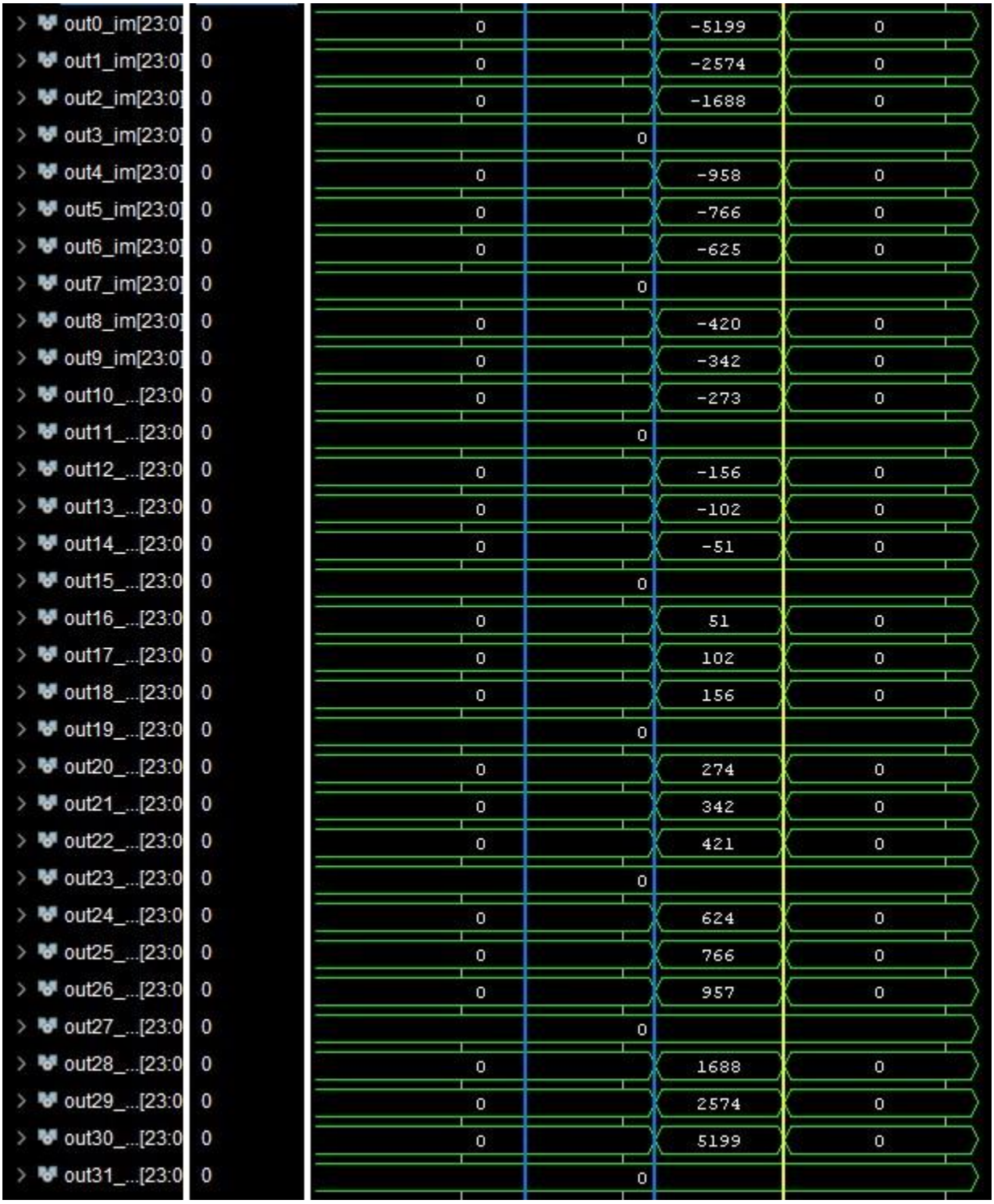


Figure 8: imag output part

Note: as shown in the 2 figures above the throughput of the FFT is 25MHz since we used only 4 clocks of the MAC instead of using 5 since that gives as full utilization of the MACs blocks

Post synthesis simulation OUTPUTs

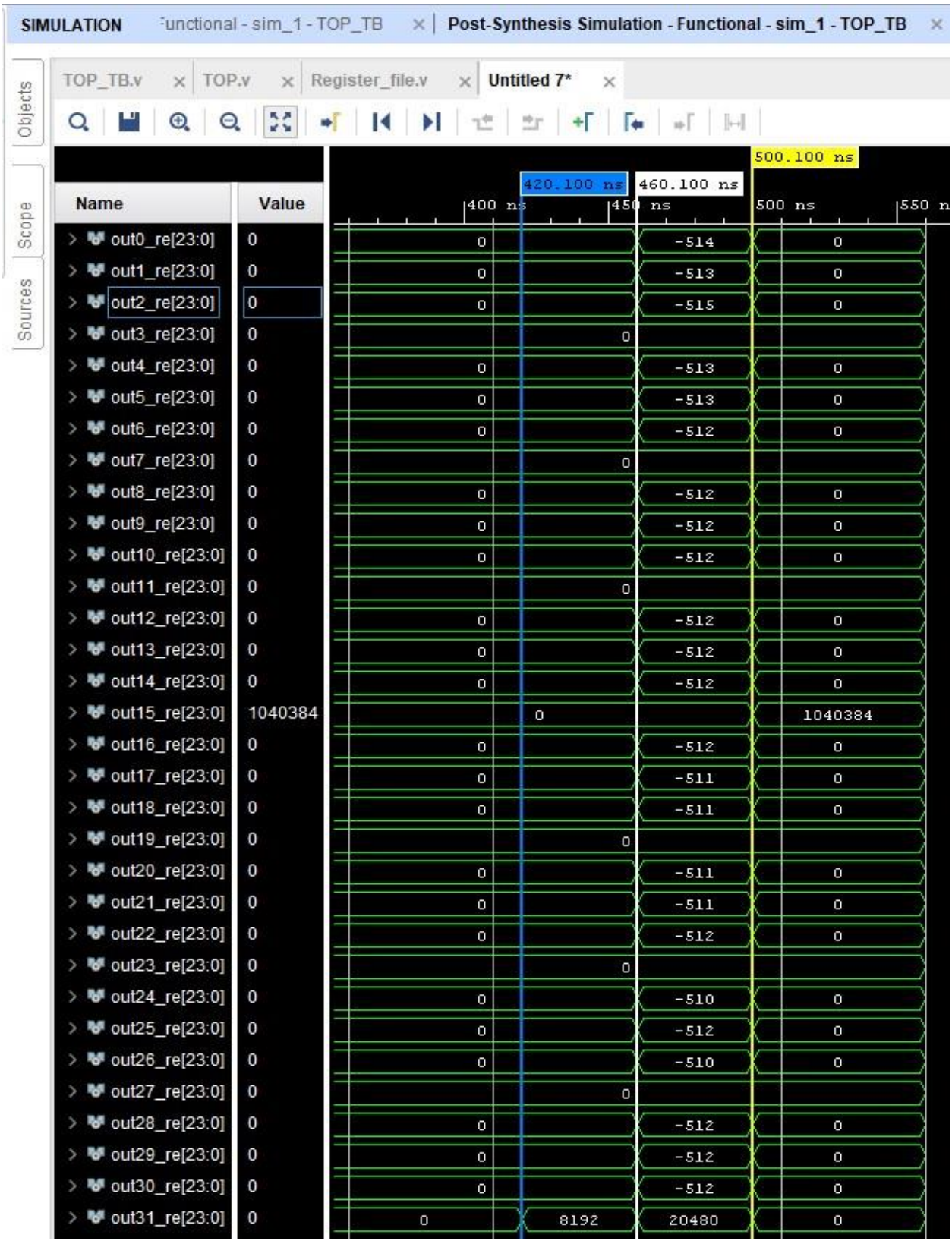


Figure 9: post synthesis real output

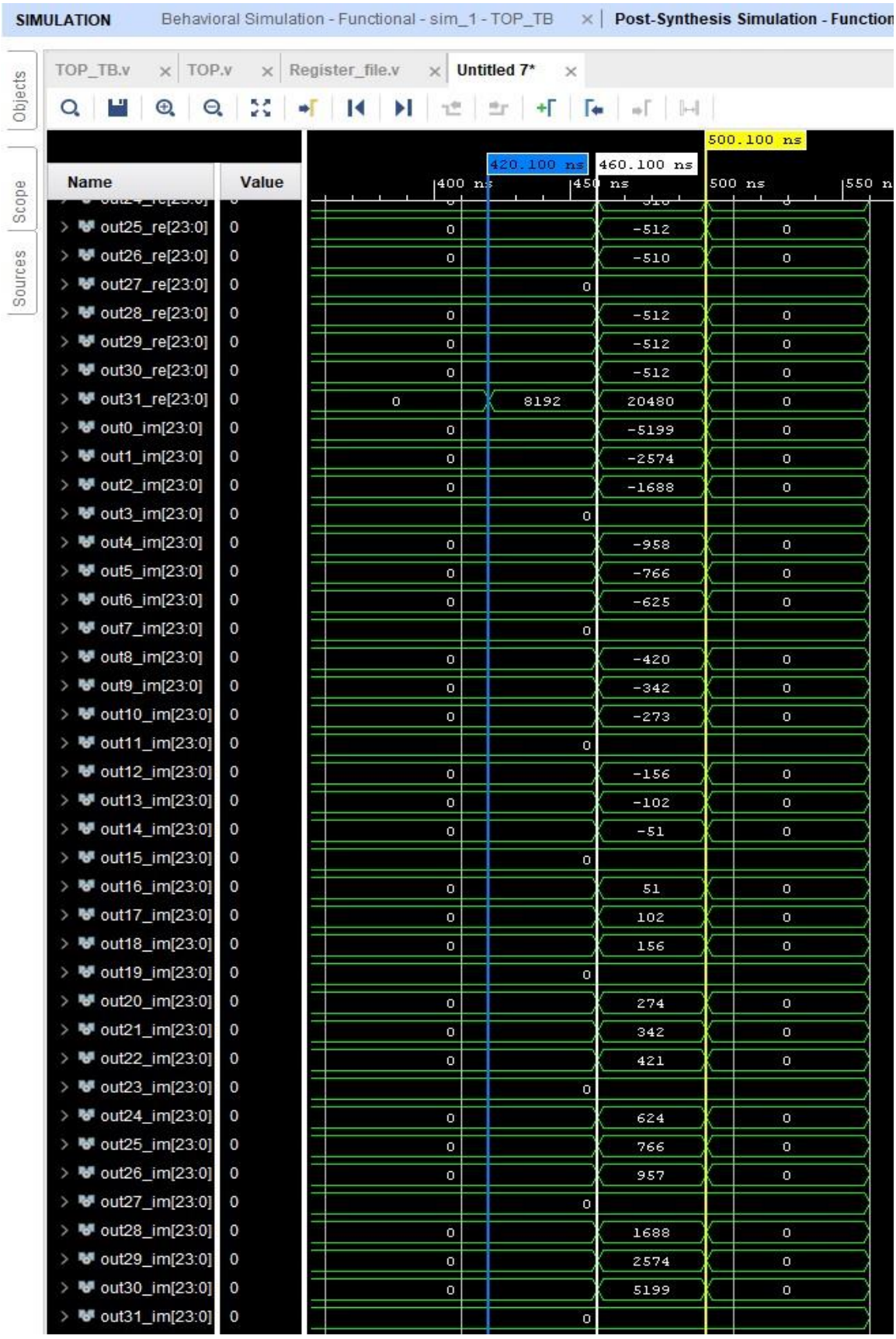


Figure 10: post synthesis imag part

Note: the output didn't change from the behavioral to the post synthesis simulations

RESULT table (result of the 3rd input with the fixed point)

	Input		Expected output		Pre-synth output		Post-synth output	
n	Real	Imag	Real	Imag	Real	Imag	Real	Imag
0	7.9375	0	0	0	0	0	0	0
1	-7.9375	0	0	0	0	0	0	0
2	7.9375	0	0	0	0	0	0	0
3	-7.9375	0	0	0	0	0	0	0
4	7.9375	0	0	0	0	0	0	0
5	-7.9375	0	0	0	0	0	0	0
6	7.9375	0	0	0	0	0	0	0
7	-7.9375	0	0	0	0	0	0	0
8	7.9375	0	0	0	0	0	0	0
9	-7.9375	0	0	0	0	0	0	0
10	7.9375	0	0	0	0	0	0	0
11	-7.9375	0	0	0	0	0	0	0
12	7.9375	0	0	0	0	0	0	0
13	-7.9375	0	0	0	0	0	0	0
14	7.9375	0	0	0	0	0	0	0
15	-7.9375	0	254	0	254	0	254	0
16	7.9375	0	0	0	0	0	0	0
17	-7.9375	0	0	0	0	0	0	0
18	7.9375	0	0	0	0	0	0	0
19	-7.9375	0	0	0	0	0	0	0
20	7.9375	0	0	0	0	0	0	0
21	-7.9375	0	0	0	0	0	0	0
22	7.9375	0	0	0	0	0	0	0
23	-7.9375	0	0	0	0	0	0	0
24	7.9375	0	0	0	0	0	0	0
25	-7.9375	0	0	0	0	0	0	0
26	7.9375	0	0	0	0	0	0	0
27	-7.9375	0	0	0	0	0	0	0
28	7.9375	0	0	0	0	0	0	0
29	-7.9375	0	0	0	0	0	0	0
30	7.9375	0	0	0	0	0	0	0
31	-7.9375	0	0	0	0	0	0	0

Noting: this output is shown to proof functionality and also to test the minimum number of bits needed to use with this design as we inputted the maximum and the minimum inputs alternately so here we found out that 1 bit for sign and 8 for integer is the minimum to use without having overflow in the values and we used 3 bits more for integer as a safety margin and also to be able to use the same module with higher inputs too, with the 12 bit used for fraction is to give more accuracy in the output.

Resource usage

Name	CLB LUTs (230400)	CLB Registers (460800)	CARRY8 (28800)	DSPs (1728)	Bonded IOB (360)	GLOBAL CLOCK BUFFERs (544)
> TOP	9096	21032	872	320	2563	2

Figure 11: utilization

Critical path

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay
Path 1	5.065	18	19	140	MAC_C120/C1/sel_reg_reg[0]/C	MAC_C120/RF1/...mag_reg[25]/D	4.780
Path 2	5.065	18	19	140	MAC_C120/C1/sel_reg_reg[0]/C	MAC_C120/RF1/r...real_reg[25]/D	4.780
Path 3	5.065	18	19	140	MAC_C120/C1/sel_reg_reg[0]/C	MAC_C120/RF1/...mag_reg[25]/D	4.780
Path 4	5.065	18	19	140	MAC_C120/C1/sel_reg_reg[0]/C	MAC_C120/RF1/r...real_reg[25]/D	4.780
Path 5	5.065	18	19	140	MAC_C120/C1/sel_reg_reg[0]/C	MAC_C120/RF2/...mag_reg[25]/D	4.780
Path 6	5.065	18	19	140	MAC_C120/C1/sel_reg_reg[0]/C	MAC_C120/RF2/r...real_reg[25]/D	4.780
Path 7	5.065	18	19	140	MAC_C120/C1/sel_reg_reg[0]/C	MAC_C120/RF2/...mag_reg[25]/D	4.780
Path 8	5.065	18	19	140	MAC_C120/C1/sel_reg_reg[0]/C	MAC_C120/RF2/r...real_reg[25]/D	4.780
Path 9	5.068	18	19	140	MAC_C120/C1/sel_reg_reg[0]/C	MAC_C120/RF1/...mag_reg[31]/D	4.777
Path 10	5.068	18	19	140	MAC_C120/C1/sel_reg_reg[0]/C	MAC_C120/RF1/r...real_reg[31]/D	4.777

Figure 12: critical path

Timing Summary

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.065 ns	Worst Hold Slack (WHS):	NA	Worst Pulse Width Slack (WPWS):	4.725 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	NA	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA	Number of Failing Endpoints:	0
Total Number of Endpoints:	31064	Total Number of Endpoints:	NA	Total Number of Endpoints:	21034

All user specified timing constraints are met.

Figure 13: Timing Summary