Combinational Circuit Design

Design the following circuits with Verilog using assign statements.

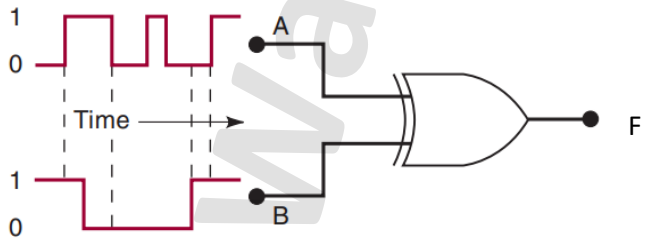
1) A four-bit binary number is represented as A3A2A1A0, where A3, A2, A1, and A0 represent the individual bits and A0 is equal to the LSB. Design a logic circuit using Verilog that will produce a HIGH output whenever the binary number is greater than 0010 and less than 1000.

- The design takes 1 input **A** (4-bits) and output **out** (1-bit)

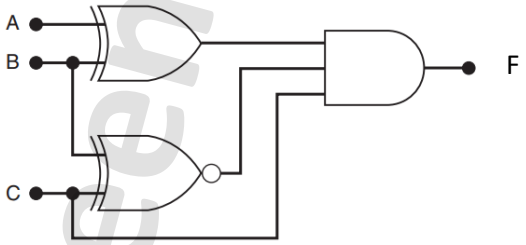
2) (a) Draw with your pen on a piece of paper the output waveform F for the circuit of Figure below.

(b) Repeat with the B input held LOW.

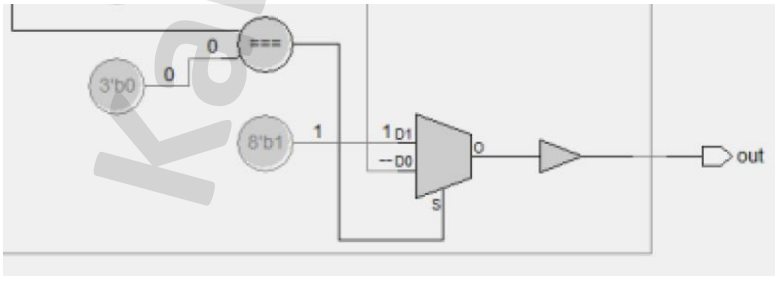
(c) Repeat with B held HIGH.



3) Design the following circuit using Verilog and determine the input conditions needed to produce F = 1



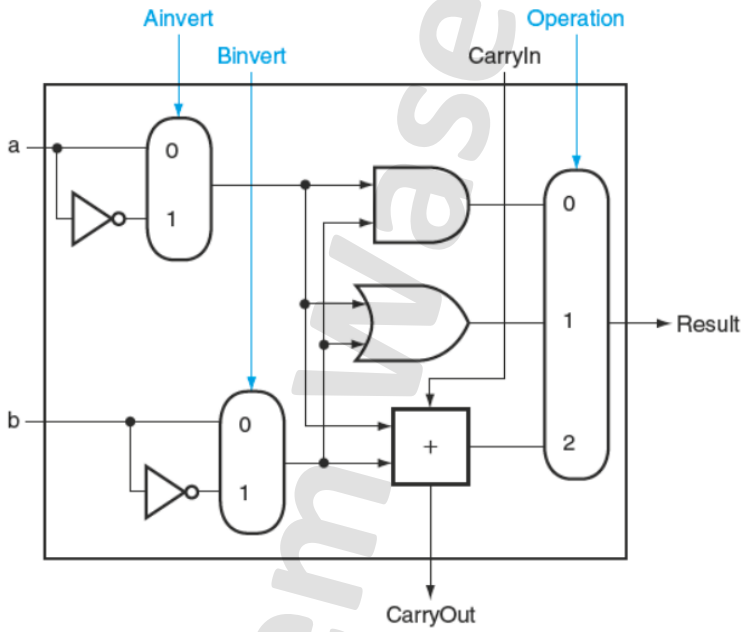
4) The following schematic snippet is from the 3 to 8 decoder in the notes



The select input of the multiplexer shown is connected to a comparator that checks whether a 3-bit input “in” bus equals 3'b000. How can this comparator be implemented using just one basic logic gate, such that it outputs 1 only when all bits of the input are 0?

5) Implement the following 1-bit ALU. If you are unfamiliar with the concept of an ALU, you can find more information by clicking here. Use conditional operator for the multiplexers. For the 3-to-1 Mux, you can use the following format for the conditional operator.

assign <output_signal> = <condition1> ? <value1> : <condition2> ? <value2> : <default_value>);



Port Name	Type	Size	Description
A	Input	1 bit	Input a
B			Input b
Ainvert			Select signal for the multiplexer to select a or a complement
Binvert			Select signal for the multiplexer to select b or b complement
CarryIn			Carry in
Operation		2 bits	Select signal for the multiplexer to drive the Result output
CarryOut	Output	1 bit	Carry out
Result		1 bit	Output of the multiplexer

Deliverables: The assignment should be submitted as a PDF file with this format <your_name>_Assignment1_extended for example Kareem_Waseem_Assignment1_extended.

Note that your document should be organized as 5 sections corresponding to each design above, and in each section, I am expecting the Verilog code for the design, and waveform snippets forcing different input values to verify the functionality of the design.