

Assignment_4

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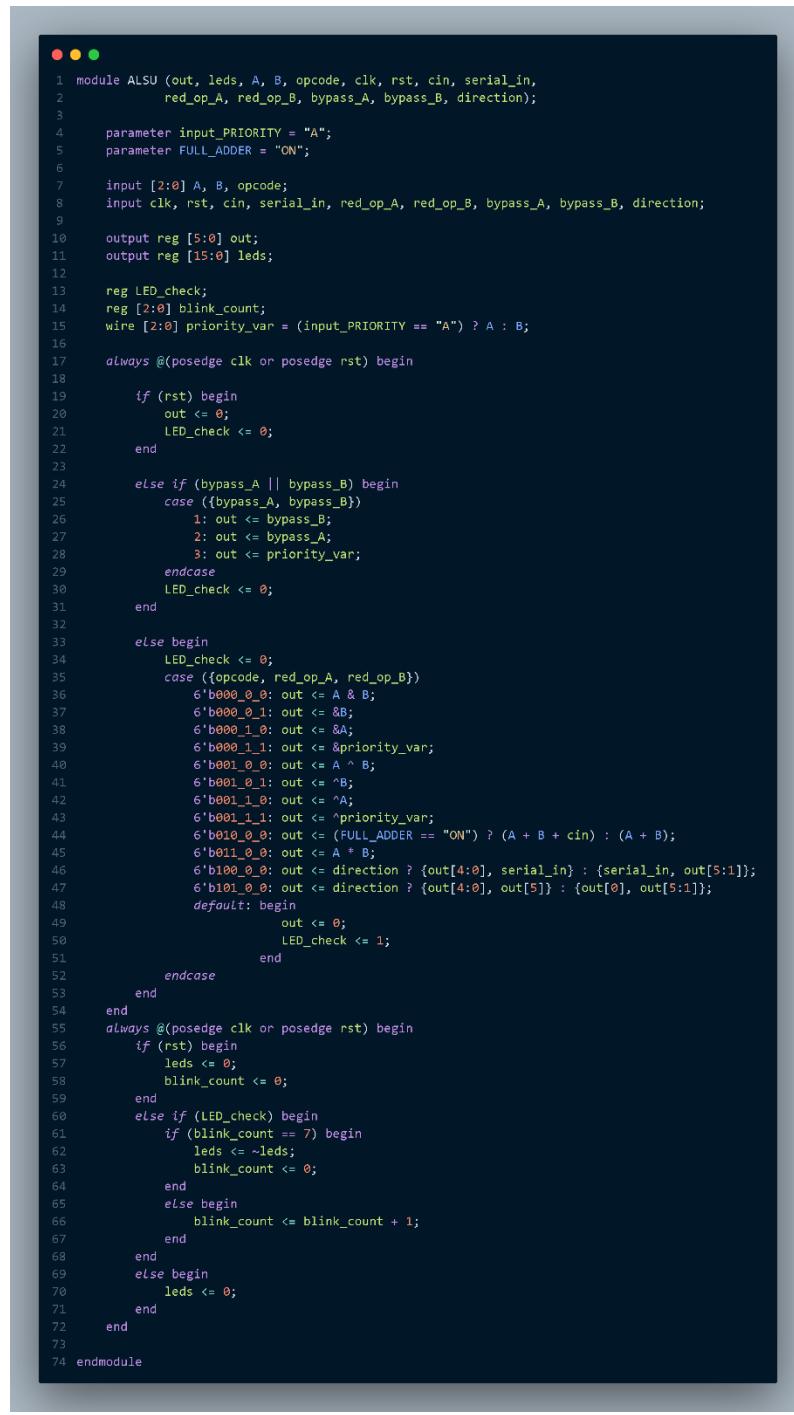
Sheet ID: 16

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Q1)

Verilog code:

a) RTL design:



```
1 module ALSU (out, leds, A, B, opcode, clk, rst, cin, serial_in,
2             red_op_A, red_op_B, bypass_A, bypass_B, direction);
3
4     parameter input_PRIORITY = "A";
5     parameter FULL_ADDER = "ON";
6
7     input [2:0] A, B, opcode;
8     input clk, rst, cin, serial_in, red_op_A, red_op_B, bypass_A, bypass_B, direction;
9
10    output reg [5:0] out;
11    output reg [15:0] leds;
12
13    reg LED_check;
14    reg [2:0] blink_count;
15    wire [2:0] priority_var = (input_PRIORITY == "A") ? A : B;
16
17    always @(posedge clk or posedge rst) begin
18
19        if (rst) begin
20            out <= 0;
21            LED_check <= 0;
22        end
23
24        else if (bypass_A || bypass_B) begin
25            case ({bypass_A, bypass_B})
26                1: out <= bypass_B;
27                2: out <= bypass_A;
28                3: out <= priority_var;
29            endcase
30            LED_check <= 0;
31        end
32
33        else begin
34            LED_check <= 0;
35            case ({opcode, red_op_A, red_op_B})
36                6'b000_0_0: out <= A & B;
37                6'b000_0_1: out <= ~B;
38                6'b000_1_0: out <= ~A;
39                6'b000_1_1: out <= priority_var;
40                6'b001_0_0: out <= A ^ B;
41                6'b001_0_1: out <= ~B;
42                6'b001_1_0: out <= ~A;
43                6'b001_1_1: out <= ~priority_var;
44                6'b010_0_0: out <= (FULL_ADDER == "ON") ? (A + B + cin) : (A + B);
45                6'b011_0_0: out <= A ^ B;
46                6'b100_0_0: out <= direction ? {out[4:0], serial_in} : {serial_in, out[5:1]};
47                6'b101_0_0: out <= direction ? {out[4:0], out[5]} : {out[0], out[5:1]};
48            default: begin
49                out <= 0;
50                LED_check <= 1;
51            end
52        endcase
53    end
54
55    always @(posedge clk or posedge rst) begin
56        if (rst) begin
57            leds <= 0;
58            blink_count <= 0;
59        end
60        else if (LED_check) begin
61            if (blink_count == 7) begin
62                leds <= ~leds;
63                blink_count <= 0;
64            end
65            else begin
66                blink_count <= blink_count + 1;
67            end
68        end
69        else begin
70            leds <= 0;
71        end
72    end
73
74 endmodule
```

b) Testbench code:

```
● ● ●
1 module ALSU_tb ();
2
3     parameter input_PRIORITY_tb = "A";
4     parameter FULL_ADDER_tb = "ON";
5
6     reg [2:0] A_tb, B_tb, opcode_tb;
7     reg clk_tb, rst_tb, cin_tb, serial_in_tb, red_op_A_tb, red_op_B_tb, bypass_A_tb, bypass_B_tb, direction_tb;
8
9     reg [5:0] out_exp;
10
11    wire [5:0] out_tb;
12    wire [15:0] leds_tb;
13
14    ALSU #(input_PRIORITY_tb, .FULL_ADDER(FULL_ADDER_tb)) DUT (out_tb, leds_tb, A_tb, B_tb,
15        opcode_tb, clk_tb, rst_tb, cin_tb, serial_in_tb, red_op_A_tb, red_op_B_tb, bypass_A_tb, bypass_B_tb, direction_tb);
16
17    initial begin
18        clk_tb = 0;
19        forever begin
20            #5 clk_tb = ~clk_tb;
21        end
22    end
23
24    initial begin
25        rst_tb = 1;
26        cin_tb = 0; serial_in_tb = 0; red_op_A_tb = 0; red_op_B_tb = 0;
27        bypass_A_tb = 0; bypass_B_tb = 0; direction_tb = 0;
28        A_tb = 0; B_tb = 0; opcode_tb = 0;
29
30        @(negedge clk_tb);
31        if(out_tb != 0 || leds_tb != 0)begin
32            $display("error Output is not reset");
33        end
34        #10;
35
36        rst_tb = 0; bypass_A_tb = 1; bypass_B_tb = 1;
37        repeat(10)begin
38            A_tb = $random;
39            B_tb = $random;
40            opcode_tb = $urandom_range(0,5);
41            @(negedge clk_tb);
42            @(negedge clk_tb);
43            if(out_tb != A_tb || leds_tb != 0)begin
44                $display("error Output is not bypassed");
45            end
46        end
47        #10;
48
49        bypass_A_tb = 0; bypass_B_tb = 0; opcode_tb = 0;
50        repeat(10)begin
51            A_tb = $random;
52            B_tb = $random;
53            red_op_A_tb = $random;
54            red_op_B_tb = $random;
55
56            if(red_op_A_tb)begin
57                out_exp = &A_tb;
58            end
59            else if (red_op_B_tb) begin
60                out_exp = &B_tb;
61            end
62            else begin
63                out_exp = A_tb & B_tb;
64            end
65
66            @(negedge clk_tb);
67            @(negedge clk_tb);
68            if(out_tb != out_exp || leds_tb != 0)begin
69                $display("error Output is not and");
70            end
71        end
72        #10;
73    end
```

//rest of code in next page

```
1      opcode_tb = 1;
2      repeat(10)begin
3          A_tb = $random;
4          B_tb = $random;
5          red_op_A_tb = $random;
6          red_op_B_tb = $random;
7
8          if(red_op_A_tb)begin
9              out_exp = ^A_tb;
10         end
11         else if (red_op_B_tb) begin
12             out_exp = ^B_tb;
13         end
14         else begin
15             out_exp = A_tb ^ B_tb;
16         end
17
18         @(negedge clk_tb);
19         @(negedge clk_tb);
20         if(out_tb != out_exp || leds_tb != 0)begin
21             $display("error Output is not Xor");
22         end
23     end
24
25     #10;
26
27     opcode_tb = 2; red_op_A_tb = 0; red_op_B_tb = 0;
28     repeat(10)begin
29         A_tb = $random;
30         B_tb = $random;
31         cin_tb = $random;
32
33         out_exp = A_tb + B_tb + cin_tb;
34
35         @(negedge clk_tb);
36         @(negedge clk_tb);
37         if(out_tb != out_exp || leds_tb != 0)begin
38             $display("error Output is not adding");
39         end
40     end
41
42     #10;
43
44     opcode_tb = 3;
45     repeat(10)begin
46         A_tb = $random;
47         B_tb = $random;
48
49         out_exp = A_tb * B_tb;
50
51         @(negedge clk_tb);
52         @(negedge clk_tb);
53         if(out_tb != out_exp || leds_tb != 0)begin
54             $display("error Output is not multiplying");
55         end
56     end
57
58     #10;
59
60     opcode_tb = 4;
61     repeat(10)begin
62         A_tb = $random;
63         B_tb = $random;
64         direction_tb = $random;
65         serial_in_tb = $random;
66         @(negedge clk_tb);
67         @(negedge clk_tb);
68     end
69
70     #10;
71
72     opcode_tb = 5;
73     repeat(10)begin
74         A_tb = $random;
75         B_tb = $random;
76         direction_tb = $random;
77         serial_in_tb = $random;
78         @(negedge clk_tb);
79         @(negedge clk_tb);
80     end
81
82     #10;
83
84     $finish;
85   end
86
87
88 endmodule
```

Simulation Tool

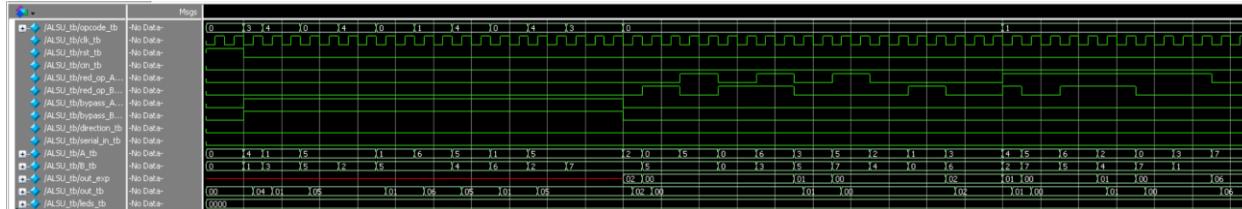
a) Do file



```
1 vlib work
2 vlog q1.v q1_tb.v
3 vsim -voptargs=+acc work.ALSU_tb
4 add wave *
5 run -all
6 #quit -sim
```

b) Questasim

```
~~~~~_
# End time: 22:00:19 on Jul 20,2025, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
# vsim -voptargs="+acc" work.ALSU_tb
# Start time: 22:00:19 on Jul 20,2025
# ** Note: (vsim-3812) Design is being optimized...
# Loading work.ALSU_tb(fast)
# Loading work.ALSU(fast)
# ** Note: $finish      : ql_tb.v(152)
#   Time: 1420 ns  Iteration: 0  Instance: /ALSU_tb
```



Synthesis Tool:

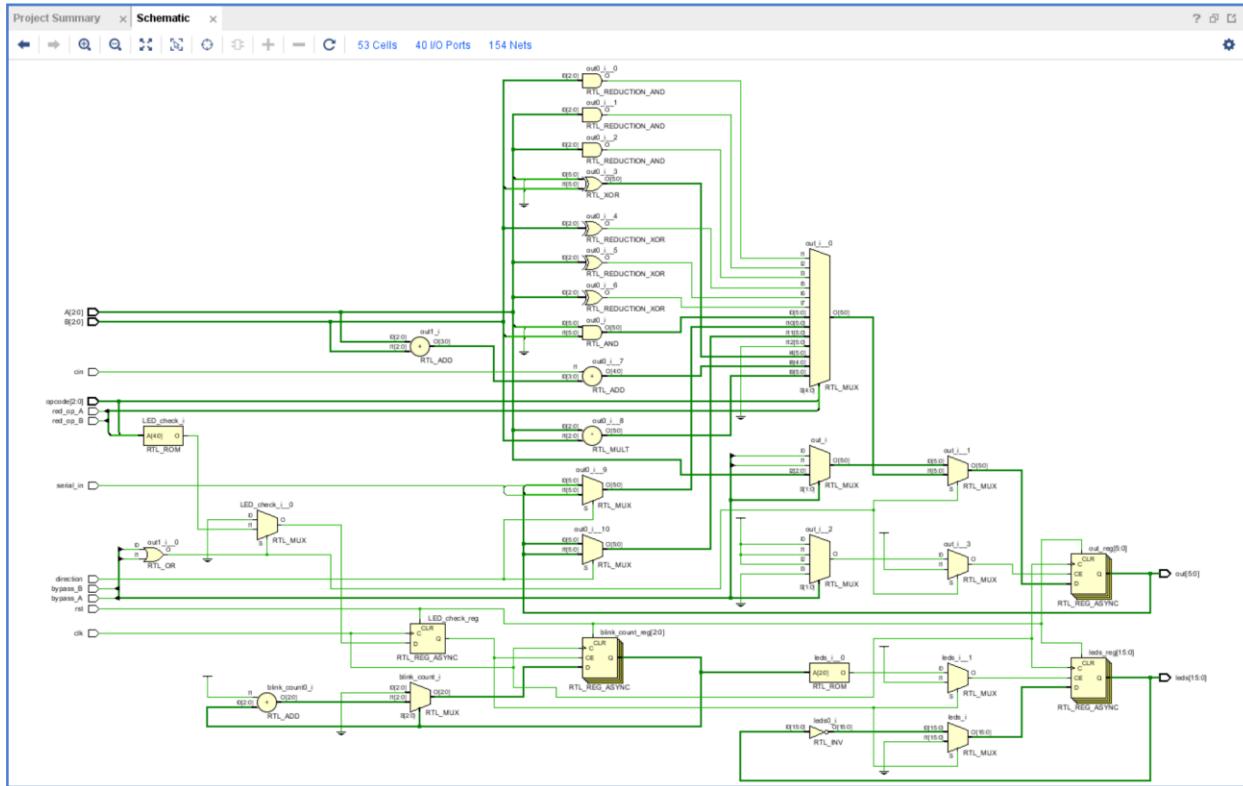
a) Constraint file

```

D:\OneDrive\Keren\mesin\Digital Design\Alu\Alu\Alu\Q1> Synthesis> constraint> C:\Carmen\Julyaya-Copylock
1 ## This file is a general .xdc for the Basys3 rev B board
2 ## To use it in a project:
3 ## - uncomment the lines corresponding to used pins
4 ## - rename the used parts (in each line, after get_ports) according to the top level signal names in the project
5
6 # Clock signal
7 set_property -dict { PACKAGE_PIN WS IOSTANDARD LVCMOS33 } [get_ports clk]
8 create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
9
10
11 ## Switches
12 set_property -dict { PACKAGE_PIN V17 IOSTANDARD LVCMOS33 } [get_ports {opcode[0]}]
13 set_property -dict { PACKAGE_PIN V16 IOSTANDARD LVCMOS33 } [get_ports {opcode[1]}]
14 set_property -dict { PACKAGE_PIN W16 IOSTANDARD LVCMOS33 } [get_ports {opcode[2]}]
15 set_property -dict { PACKAGE_PIN W17 IOSTANDARD LVCMOS33 } [get_ports {A[0]}]
16 set_property -dict { PACKAGE_PIN W15 IOSTANDARD LVCMOS33 } [get_ports {A[1]}]
17 set_property -dict { PACKAGE_PIN V15 IOSTANDARD LVCMOS33 } [get_ports {A[2]}]
18 set_property -dict { PACKAGE_PIN W14 IOSTANDARD LVCMOS33 } [get_ports {B[0]}]
19 set_property -dict { PACKAGE_PIN W13 IOSTANDARD LVCMOS33 } [get_ports {B[1]}]
20 set_property -dict { PACKAGE_PIN V2 IOSTANDARD LVCMOS33 } [get_ports {B[2]}]
21 set_property -dict { PACKAGE_PIN T3 IOSTANDARD LVCMOS33 } [get_ports {cin}]
22 set_property -dict { PACKAGE_PIN T2 IOSTANDARD LVCMOS33 } [get_ports {red_op_A}]
23 set_property -dict { PACKAGE_PIN R3 IOSTANDARD LVCMOS33 } [get_ports {red_op_B}]
24 set_property -dict { PACKAGE_PIN W3 IOSTANDARD LVCMOS33 } [get_ports {bypass_A}]
25 set_property -dict { PACKAGE_PIN U1 IOSTANDARD LVCMOS33 } [get_ports {bypass_B}]
26 set_property -dict { PACKAGE_PIN T1 IOSTANDARD LVCMOS33 } [get_ports {direction}]
27 set_property -dict { PACKAGE_PIN R2 IOSTANDARD LVCMOS33 } [get_ports {serial_in}]
28
29
30 ## LEDs
31 set_property -dict { PACKAGE_PIN U16 IOSTANDARD LVCMOS33 } [get_ports {leds[0]}]
32 set_property -dict { PACKAGE_PIN E19 IOSTANDARD LVCMOS33 } [get_ports {leds[1]}]
33 set_property -dict { PACKAGE_PIN U19 IOSTANDARD LVCMOS33 } [get_ports {leds[2]}]
34 set_property -dict { PACKAGE_PIN V19 IOSTANDARD LVCMOS33 } [get_ports {leds[3]}]
35 set_property -dict { PACKAGE_PIN W18 IOSTANDARD LVCMOS33 } [get_ports {leds[4]}]
36 set_property -dict { PACKAGE_PIN U15 IOSTANDARD LVCMOS33 } [get_ports {leds[5]}]
37 set_property -dict { PACKAGE_PIN U14 IOSTANDARD LVCMOS33 } [get_ports {leds[6]}]
38 set_property -dict { PACKAGE_PIN V14 IOSTANDARD LVCMOS33 } [get_ports {leds[7]}]
39 set_property -dict { PACKAGE_PIN V13 IOSTANDARD LVCMOS33 } [get_ports {leds[8]}]
40 set_property -dict { PACKAGE_PIN V9 IOSTANDARD LVCMOS33 } [get_ports {leds[9]}]
41 set_property -dict { PACKAGE_PIN W3 IOSTANDARD LVCMOS33 } [get_ports {leds[10]}]
42 set_property -dict { PACKAGE_PIN U9 IOSTANDARD LVCMOS33 } [get_ports {leds[11]}]
43 set_property -dict { PACKAGE_PIN P9 IOSTANDARD LVCMOS33 } [get_ports {leds[12]}]
44 set_property -dict { PACKAGE_PIN N9 IOSTANDARD LVCMOS33 } [get_ports {leds[13]}]
45 set_property -dict { PACKAGE_PIN P1 IOSTANDARD LVCMOS33 } [get_ports {leds[14]}]
46 set_property -dict { PACKAGE_PIN L1 IOSTANDARD LVCMOS33 } [get_ports {leds[15]}]
47
48 ## Configuration options, can be used for all designs
49 set_property CONFIG_VOLTAGE 3_3 [current_design]
50 set_property CFGVBS_VCCO [current_design]
51
52 ## SPI configuration mode options for QSPI boot, can be used for all designs
53 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
54 set_property BITSTREAM.CONFIG.CONFIGURE 33 [current_design]
55 set_property CONFIG_MODE SPIx4 [current_design]
56
57 create_debug_core u_ilia_0 ilia
58 set_property ALL_PROBE SAME_MU TRUE [get_debug_cores u_ilia_0]
59 set_property ALL_PROBE SAME_MU_CNT 1 [get_debug_cores u_ilia_0]
60 set_property C_ADV_TRIGGER False [get_debug_cores u_ilia_0]
61 set_property C_DATA_DEPTH 1024 [get_debug_cores u_ilia_0]
62 set_property C_EN_STRG_QUAL false [get_debug_cores u_ilia_0]
63 set_property C_INPUT_PIPE_STAGES 0 [get_debug_cores u_ilia_0]
64 set_property C_TRIGGER_EN false [get_debug_cores u_ilia_0]
65 set_property C_TRIGGEROUT_EN false [get_debug_cores u_ilia_0]
66 set_property port_width 1 [get_debug_ports u_ilia_0/clk]
67 connect_debug_port_u_ilia_0/clk [get_nets [list clk_IBUF_BUFG]]
68 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ilia_0/probe0]
69 set_property port_width 3 [get_debug_ports u_ilia_0/probe0]
70 connect_debug_port_u_ilia_0/probe0 [get_nets [list {opcode_IBUF[0]} {opcode_IBUF[1]} {opcode_IBUF[2]}]]
71 create_debug_port_u_ilia_0/probe
72 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ilia_0/probe1]
73 connect_debug_port_u_ilia_0/probe1 [get_nets [list {B_IBUF[0]} {B_IBUF[1]} {B_IBUF[2]}]]
74 create_debug_port_u_ilia_0/probe
75 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ilia_0/probe2]
76 set_property port_width 3 [get_debug_ports u_ilia_0/probe2]
77 connect_debug_port_u_ilia_0/probe2 [get_nets [list {A_IBUF[0]} {A_IBUF[1]} {A_IBUF[2]}]]
78 create_debug_port_u_ilia_0/probe
79 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ilia_0/probe3]
80 connect_debug_port_u_ilia_0/probe3 [get_nets [list bypass_A_IBUF]]
81 create_debug_port_u_ilia_0/probe
82 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ilia_0/probe4]
83 connect_debug_port_u_ilia_0/probe4 [get_nets [list bypass_B_IBUF]]
84 create_debug_port_u_ilia_0/probe
85 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ilia_0/probe5]
86 connect_debug_port_u_ilia_0/probe5 [get_nets [list direction_IBUF]]
87 create_debug_port_u_ilia_0/probe
88 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ilia_0/probe6]
89 connect_debug_port_u_ilia_0/probe6 [get_nets [list red_op_A_IBUF]]
90
91 connect_debug_port_u_ilia_0/probe6 [get_nets [list red_op_A_IBUF]]
92 create_debug_port_u_ilia_0/probe
93 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ilia_0/probe5]
94 set_property port_width 1 [get_debug_ports u_ilia_0/probe5]
95 connect_debug_port_u_ilia_0/probe5 [get_nets [list direction_IBUF]]
96 create_debug_port_u_ilia_0/probe
97 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ilia_0/probe6]
98 connect_debug_port_u_ilia_0/probe6 [get_nets [list red_op_A_IBUF]]
99
100 connect_debug_port_u_ilia_0/probe6 [get_nets [list red_op_A_IBUF]]
101 create_debug_port_u_ilia_0/probe
102 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ilia_0/probe7]
103 set_property port_width 1 [get_debug_ports u_ilia_0/probe7]
104 connect_debug_port_u_ilia_0/probe7 [get_nets [list red_op_B_IBUF]]
105 create_debug_port_u_ilia_0/probe
106 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ilia_0/probe8]
107 connect_debug_port_u_ilia_0/probe8 [get_nets [list rst_IBUF]]
108 create_debug_port_u_ilia_0/probe
109 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ilia_0/probe9]
110 connect_debug_port_u_ilia_0/probe9 [get_nets [list serial_in_IBUF]]
111 set_property C_CLK_INPUT_FREQ_HZ 300000000 [get_debug_cores dbg_hub]
112 set_property C_ENABLE_CLK_DIVIDER false [get_debug_cores dbg_hub]
113 set_property C_USER_SCAN_CHAIN 1 [get_debug_cores dbg_hub]
114 connect_debug_port_dbg_hub/clk [get_nets clk_IBUF_BUFG]
115

```

b) Elaboration



Elaborated Design (7 infos)

General Messages (7 infos)

- ⓘ [Synth 8-157] synthesizing module 'ALSU' [q1.v:1]
- ⓘ [Synth 8-155] case statement is not full and has no default [q1.v:25]
- ⓘ [Synth 8-6155] done synthesizing module 'ALSU' (1#1) [q1.v:1]
- ⓘ [Device 21-403] Loading part xc7a35ticpg236-1L
- ⓘ [Project 1-570] Preparing netlist for logic optimization
- ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- ⓘ [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

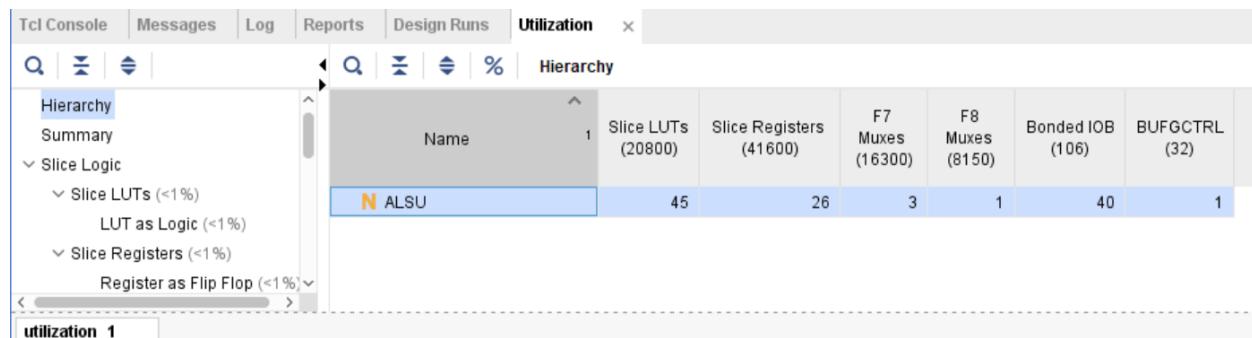
c) Synthesis

✓ **Synthesis** (1 warning, 20 infos)

- ① [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
- ① [Synth 8-6157] synthesizing module 'ALSU' [q1.v:1]
- ① [Synth 8-155] case statement is not full and has no default [q1.v:25]
- ① [Synth 8-155] done synthesizing module 'ALSU' (1#1) [q1.v:1]
- ① [Device 21-403] Loading part xc7a35tcpg236-1L
- ① [Project 1-238] Implementation specific constraints were found while reading constraint file [D:/other/Courses/Kareem_waseem_Digital-Design/Ass/Ass4/Q1/Synthesis/constraint/Constraints_basys3 - Copy.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [X:\ALSU_proplmp.xdc]. Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
- ① [Synth 8-5546] ROM "leds" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
- ① [Project 1-571] Translating synthesized netlist
- ① [Netlist 29-17] Analyzing 22 Unisim elements for replacement
- ① [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- > ① [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- ① [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- > ① [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
- ① [Common 17-83] Releasing license: Synthesis
- ① [Constraints 18-5210] No constraint will be written out.
- ① [Common 17-1381] The checkpoint 'D:/other/Courses/Kareem_waseem_Digital-Design/Ass/Ass4/Q1/Synthesis/Q1_p2/project_1/runs/synth_1/ALSU.dcp' has been generated.
- ① [runtdc-4] Executing : report_utilization_file ALSU_utilization_synth.rpt -pb ALSU_utilization_synth.pb
- ① [Common 17-206] Exiting Vivado at Sun Jul 20 23:15:47 2025...

✓ **Synthesized Design** (6 infos)

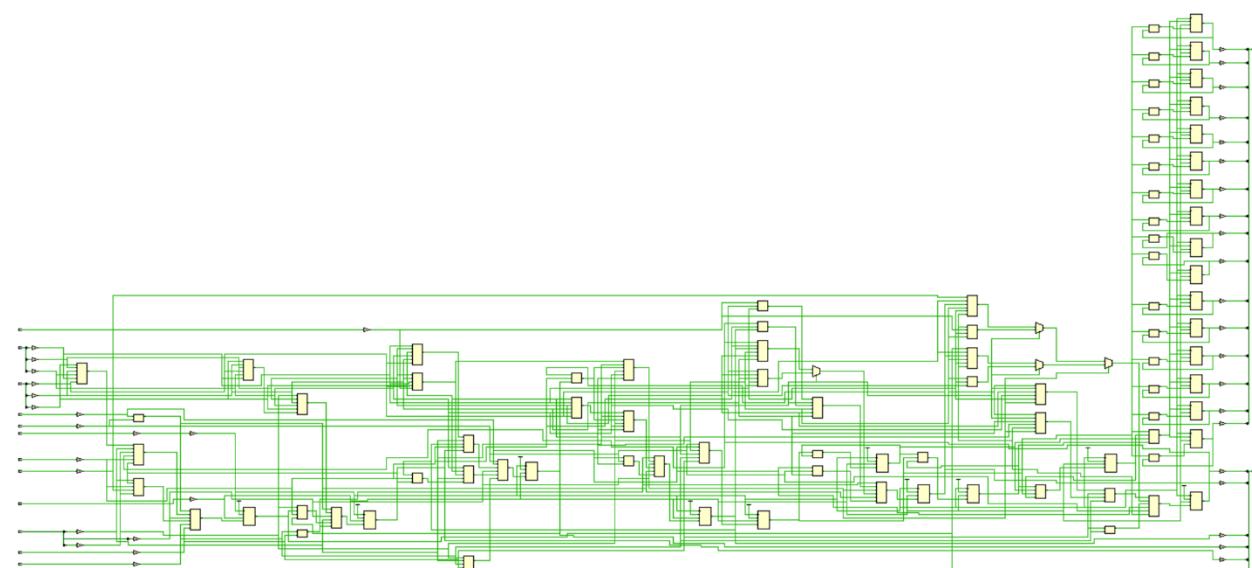
- ✓ General Messages (6 infos)
 - ① [Netlist 29-17] Analyzing 22 Unisim elements for replacement
 - ① [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - ① [Project 1-479] Netlist was created with Vivado 2018.2
 - ① [Project 1-570] Preparing netlist for logic optimization
 - ① [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - ① [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.



Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 7.121 ns	Worst Hold Slack (WHS): 0.139 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 41	Total Number of Endpoints: 41	Total Number of Endpoints: 27

All user specified timing constraints are met.



d) Implementation

Implementation (1 warning, 103 infos)

- Design Initialization (7 infos)
 - [Netlist 29-17] Analyzing 22 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Project 1-479] Netlist was created with Vivado 2018.2
 - [Device 21-403] Loading part xc7a35tcg236-1L
 - [Project 1-570] Preparing netlist for logic optimization
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - [Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed.
- Opt Design (35 infos)
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35l'
 - [Project 1-461] DRC finished with 0 Errors
 - [Project 1-462] Please refer to the DRC report (report_drc) for more information.
 - [IP_Flow 19-234] Refreshing IP repositories
 - [IP_Flow 19-1704] No user IP repositories specified
 - [IP_Flow 19-2131] Loaded Vivado IP repository 'D:\Prg\Vivado\Vivado2018.2\data\ip'.
 - [Chipscope 15-329] Generating Script for core instance : dsg_hub (1 more like this)
 - [IP_Flow 19-3806] Processing IP xilinx.com:ip:xsdbm:3.0 for cell dsg_hub_CV. (1 more like this)
 - [Opt 31-49] Retargeted 0 cells(s).
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s). (1 more like this)
 - [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
 - [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
 - [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
 - [Pwropt 34-8] Applying IDT optimizations ...
 - [Pwropt 34-10] Applying ODC optimizations ...
 - [Timing 38-35] Done setting XDC timing constraints. (1 more like this)
 - [Phyopt 32-61] Estimated Timing Summary | WNS=0.027 | TNS=0.000 |
 - [Pwropt 34-162] WRITE_MODE attribute of 0 BRAM(s) out of a total of 1 has been updated to save power. Run report_power_opt to get a complete listing of the BRAMs updated.
 - [Pwropt 34-201] Structural ODC has moved 0 WE to EN ports
 - [Common 17-83] Releasing license: Implementation
 - [Timing 38-480] Writing timing data to binary archive.
 - [Common 17-138] The checkpoint 'D:\other\Courses\Kareem_waseem_Digital-Design\Ass\Ass4\Q1\Synthesis\Q1_p2\project_1\project_1.rpt' has been generated.
 - [runrtl-4] Executing : report_drc -file ALSU_drc_opted.rpt -pb ALSU_drc_opted.pb -rpx ALSU_drc_opted.rpx
 - [IP_Flow 19-1839] IP Catalog is up to date.
 - [DRC 23-27] Running DRC with 2 threads (1 more like this)
 - [Corecl 2-168] The results of DRC are in file **ALSU_drc_opted.rpt**.
- Place Design (24 infos)
 - [Chipscope 16-240] Debug cores have already been implemented
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35l'
 - [DRC 23-27] Running DRC with 2 threads (1 more like this)
 - [Vivado_Td 4-198] DRC finished with 0 Errors (1 more like this)
 - [Vivado_Td 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
 - [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
 - [Phyopt 32-65] No nets found for high-fanout optimization.
 - [Phyopt 32-232] Optimized 0 net. Created 0 new instance.
 - [Phyopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell
 - [Place 45-31] BUFG insertion identified 0 candidate nets, 0 success, 0 skipped for placement/routing, 0 skipped for timing, 0 skipped for netlist change reason.
 - [Place 30-746] Post Placement Timing Summary WNS=4.576. For the most accurate timing information please run report_timing.
 - [Common 17-83] Releasing license: Implementation
 - [Timing 38-480] Writing timing data to binary archive.
 - [Common 17-138] The checkpoint 'D:\other\Courses\Kareem_waseem_Digital-Design\Ass\Ass4\Q1\Synthesis\Q1_p2\project_1\project_1.rns\impl_1\ALSU_placed.dcp' has been generated.
 - [runrtl-4] Executing : report_io -file ALSU_io_placed.rpt (2 more like this)
- Route Design (1 warning, 37 infos)
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35l'
 - [Vivado_Td 4-198] DRC finished with 0 Errors
 - [Vivado_Td 4-199] Please refer to the DRC report (report_drc) for more information.
 - [Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs
 - [Route 35-416] Intermediate Timing Summary | WNS=4.616 | TNS=0.000 | WHS=-0.155 | THS=-89.680| (4 more like this)
 - [Route 35-57] Estimated Timing Summary | WNS=4.217 | TNS=0.000 | WHS=0.027 | THS=0.000
 - [Route 35-327] The final timing numbers are based on the router estimated timing analysis. For a complete and accurate timing signoff, please run report_timing_summary.
 - [Route 35-16] Router Completed Successfully
 - [Common 17-83] Releasing license: Implementation
 - [Timing 38-480] Writing timing data to binary archive.
 - [Common 17-138] The checkpoint 'D:\other\Courses\Kareem_waseem_Digital-Design\Ass\Ass4\Q1\Synthesis\Q1_p2\project_1\project_1.rns\impl_1\ALSU_routed.dcp' has been generated.
 - [IP_Flow 19-1839] IP Catalog is up to date.
 - [DRC 23-27] Running DRC with 2 threads (1 more like this)
 - [Corecl 2-168] The results of DRC are in file **ALSU_drc_routed.rpt**.
 - [runrtl-4] Executing : report_drc -file ALSU_drc_routed.rpt -pb ALSU_drc_routed.pb -rpx ALSU_drc_routed.rpx (7 more like this)
 - [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
 - [DRC 23-133] Running Methodology with 2 threads
 - [Corecl 2-1520] The results of Report Methodology are in file **ALSU_methodology_drc_routed.rpt**.
 - [Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met.
 - [Vivado_Td 4-545] No incremental reuse to report_no incremental placement and routing data was found.

> [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)

Implemented Design (1 warning, 9 infos)

- General Messages (1 warning, 9 infos)
 - [Netlist 29-17] Analyzing 155 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Project 1-479] Netlist was created with Vivado 2018.2
 - [Project 1-570] Preparing netlist for logic optimization
 - [Timing 38-478] Restoring timing data from binary archive.
 - [Timing 38-479] Binary timing data restore complete.
 - [Project 1-856] Restoring constraints from binary archive.
 - [Project 1-853] Binary constraint restore complete.
 - [Project 1-111] Unisim Transformation Summary: A total of 72 instances were transformed. CFGLUT5 => CFGLUT5 (SRLC32E, SRL16E); 72 instances RAM32M => RAM32M (RAMD32, RAMD32, RAMD32, RAMD32, RAMS32, RAMS32); 6 instances
 - [Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met.

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing Utilization

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCAN2 (4)
ALSU	1483	2251	13	1	737	1342	141	911	0.5	40	2	1
dbg_hub (dbg_hub)	476	727	0	0	243	452	24	308	0	0	1	1
u_ilia_0 (u_ilia_0)	962	1498	10	0	479	845	117	586	0.5	0	0	0

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing Utilization

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (2)

Check Timing (39)

Intra-Clock Paths

Inter-Clock Paths

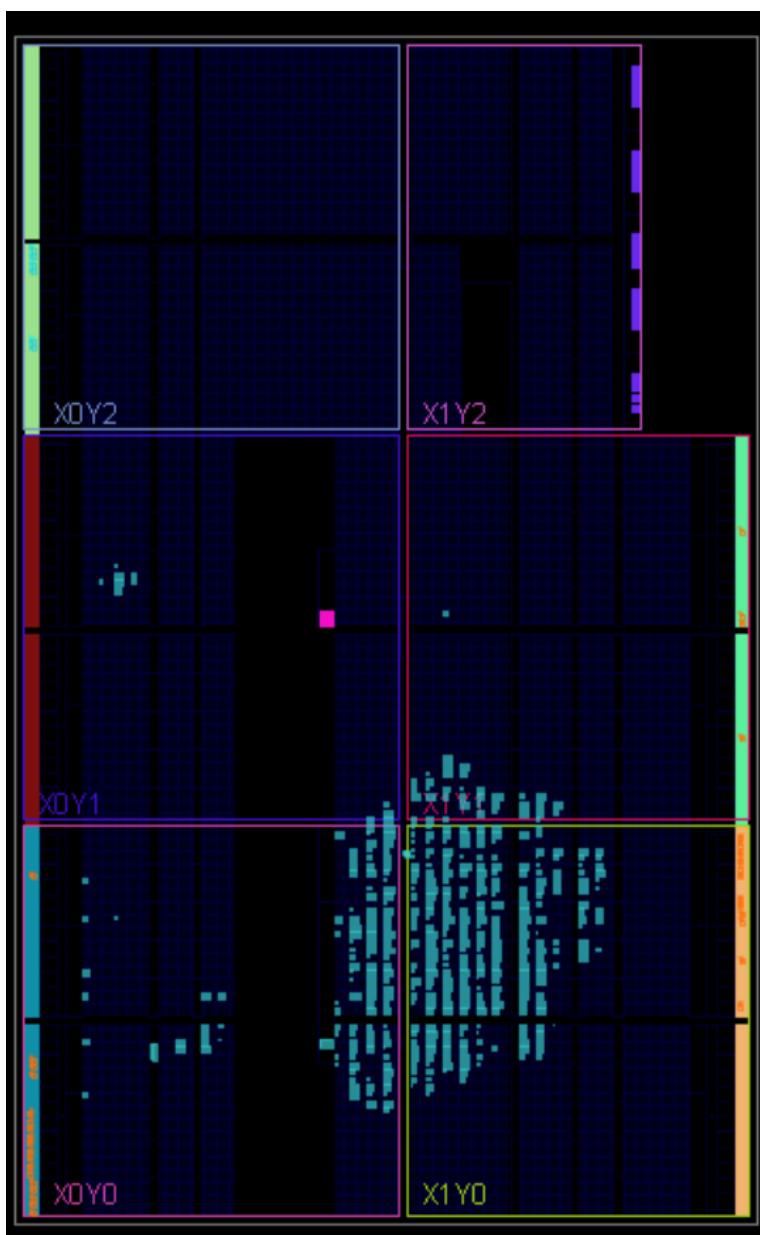
Setup Hold Pulse Width

Worst Negative Slack (WNS): 4.220 ns Total Negative Slack (TNS): 0.000 ns Number of Failing Endpoints: 0 Total Number of Endpoints: 4377

Worst Hold Slack (WHS): 0.028 ns Total Hold Slack (THS): 0.000 ns Number of Failing Endpoints: 0 Total Number of Endpoints: 4361

Worst Pulse Width Slack (WPWS): 3.750 ns Total Pulse Width Negative Slack (TPWS): 0.000 ns Number of Failing Endpoints: 0 Total Number of Endpoints: 2500

All user specified timing constraints are met.



Linting Tool

a)

The screenshot shows the Questa Lint 2021.1 interface. The main window displays a Verilog module named `ALSU`. The code defines parameters `input_PRIORITY`, `A`, and `FULL_ADDER`, and various logic blocks including `LED_check`, `blink_count`, and a priority selection logic. The `always` block handles the output `out` based on `rst` and bypass conditions. The `Info` section of the Lint Summary table shows four entries: `async_reset_active_high`, `condition_const`, and `multi_ports_in_single_line`, each with a count of 1.

Name	Count
Resolved(verified, fixed, waived)	4
Info	4
async_reset_active_high	1
condition_const	2
multi_ports_in_single_line	1

Below the main window, a separate window titled "Lint Checks" is open, showing a table with columns: Severity, Status, Check, Alias, Message, Module, Category, State, Owner, and STARC Reference. The table is currently empty.

Q2)

Verilog code:

a) RTL design

```
1 module DSP48A1_simplified (P, A, B, D, C, clk, rst_n);
2   parameter OPERATION = "ADD";
3
4   input [17:0] A, B, D;
5   input [47:0] C;
6   input clk, rst_n;
7   output reg [47:0] P;
8
9   reg [17:0] A_reg, B_reg, D_reg;
10  reg [47:0] C_reg;
11  reg [18:0] DB;
12  reg [47:0] DBA;
13
14  always @(posedge clk) begin
15    A_reg <= A; B_reg <= B; D_reg <= D; C_reg <= C;
16  end
17  always @(posedge clk or negedge rst_n) begin
18    if(!rst_n)begin
19      DB <= 0;
20      DBA <= 0;
21      P <= 0;
22    end
23    else begin
24      if(OPERATION == "ADD")begin
25        DB <= D_reg + B_reg;
26        DBA <= DB * A_reg;
27        P <= DBA + C_reg;
28      end
29      else begin
30        DB <= D_reg - B_reg;
31        DBA <= DB * A_reg;
32        P <= DBA - C_reg;
33      end
34    end
35  end
36
37 endmodule
```

b) Testbench:

```
1 module DSP48A1_simplified_tb ();
2   parameter OPERATION_tb = "ADD";
3
4   reg [17:0] A_tb, B_tb, D_tb;
5   reg [47:0] C_tb;
6   reg clk_tb, rst_n_tb;
7   wire [47:0] P_tb;
8
9   DSP48A1_simplified #(OPERATION_tb) DUT (P_tb, A_tb, B_tb, D_tb, C_tb, clk_tb, rst_n_tb);
10
11 initial begin
12   clk_tb = 0;
13   forever begin
14     #5 clk_tb = ~clk_tb;
15   end
16 end
17
18 initial begin
19   $monitor("A=%0d B=%0d D=%0d C=%0d P=%0d", A_tb, B_tb, D_tb, C_tb, P_tb);
20
21   rst_n_tb = 0; A_tb = 10; B_tb = 5; D_tb = 7; C_tb = 20;
22   #10 rst_n_tb = 1;
23   #100;
24   rst_n_tb = 0; A_tb = 6; B_tb = 20; D_tb = 15; C_tb = 100;
25   #10 rst_n_tb = 1;
26   #100;
27   $finish;
28 end
29
30
31
32 endmodule
```

Simulation Tool

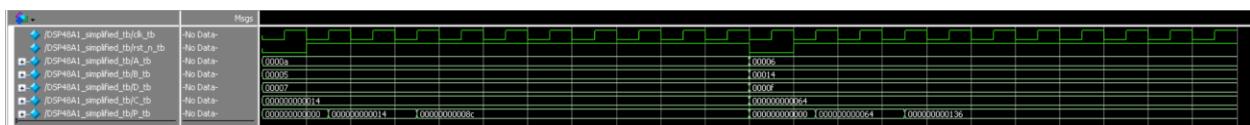
a) Do file



```
1 vlib work
2 vlog q2.v q2_tb.v
3 vsim -voptargs=+acc work.DSP48A1_simplified_tb
4 add wave *
5 run -all
6 #quit -sim
```

b) Questasim

```
# vsim -voptargs="+acc" work.DSP48A1_simplified_tb
# Start time: 12:50:45 on Jul 24,2025
# ** Note: (vsim-3813) Design is being optimized due to module recompilation...
# Loading work.DSP48A1_simplified_tb(fast)
# Loading work.DSP48A1_simplified(fast)
# A=10 B=5 D=7 C=20 P=0
# A=10 B=5 D=7 C=20 P=20
# A=10 B=5 D=7 C=20 P=140
# A=6 B=20 D=15 C=100 P=0
# A=6 B=20 D=15 C=100 P=100
# A=6 B=20 D=15 C=100 P=310
# *** Note: $finish : q2_tb.v(28)
#   Time: 220 ns Iteration: 0 Instance: /DSP48A1_simplified_tb
```



Synthesis Tool:

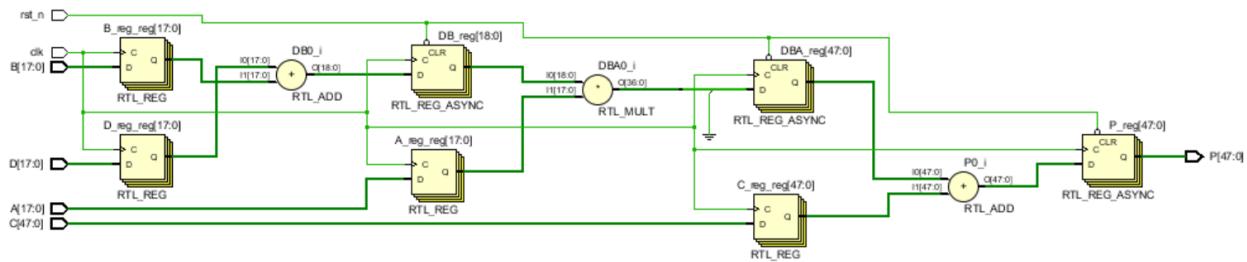
a) Constraint file

```
5
6 ## Clock signal
7 set_property -dict { PACKAGE_PIN W5 IOSTANDARD LVCMOS33 } [get_ports clk]
8 create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
9
```

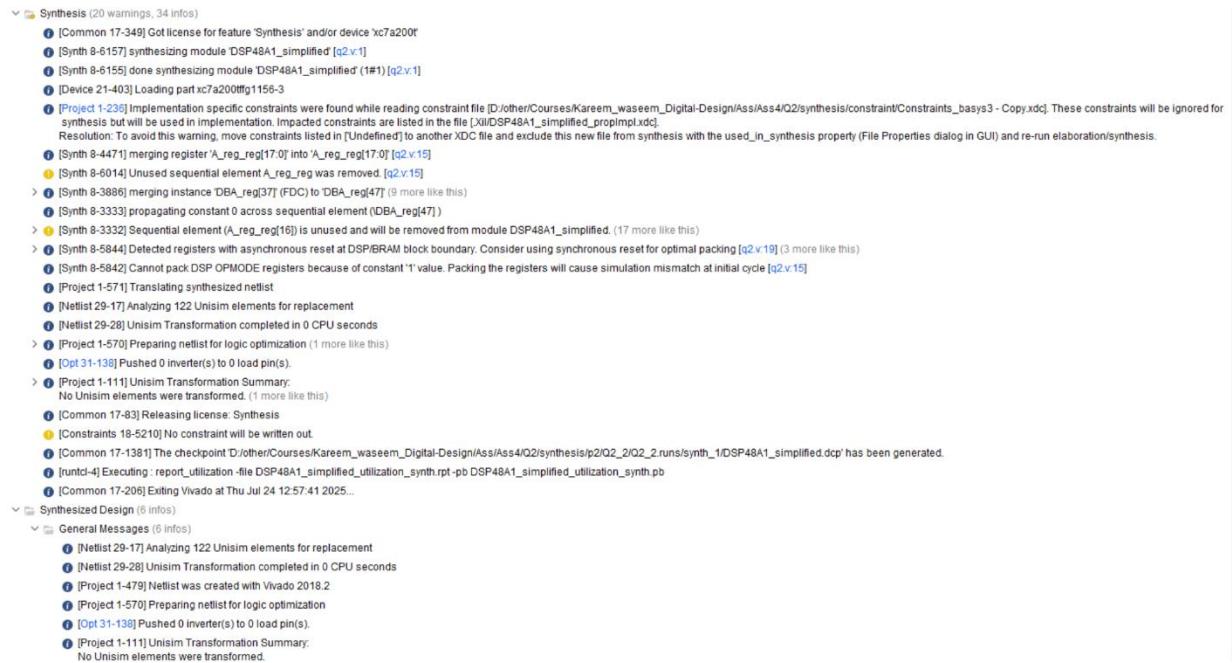
b) Elaboration

✓ Elaborated Design (5 infos)
✓ General Messages (6 infos)

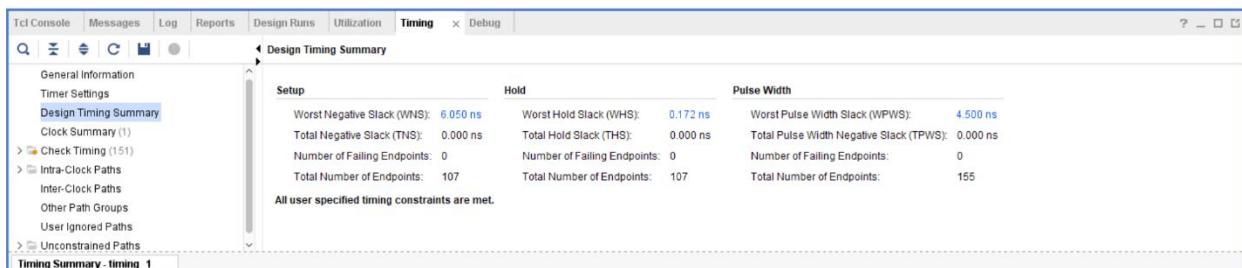
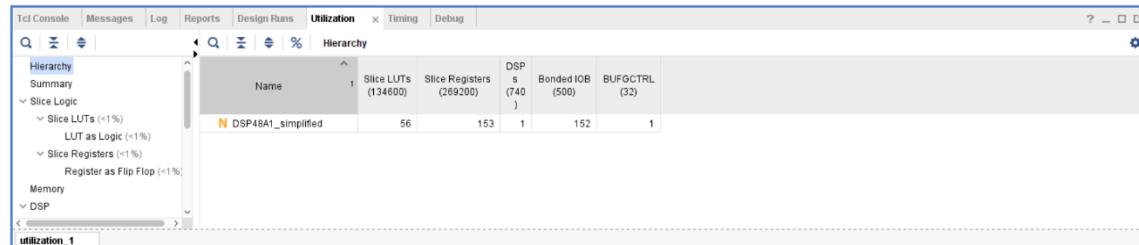
- ➊ [Synth 8-6157] synthesizing module 'DSP48A1_simplified' [q2.v:1]
- ➋ [Synth 8-6155] done synthesizing module 'DSP48A1_simplified' (1#1) [q2.v:1]
- ➌ [Device 21-403] Loading part xc7a200tfg1156-3
- ➍ [Project 1-570] Preparing netlist for logic optimization
- ➎ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- ➏ [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.



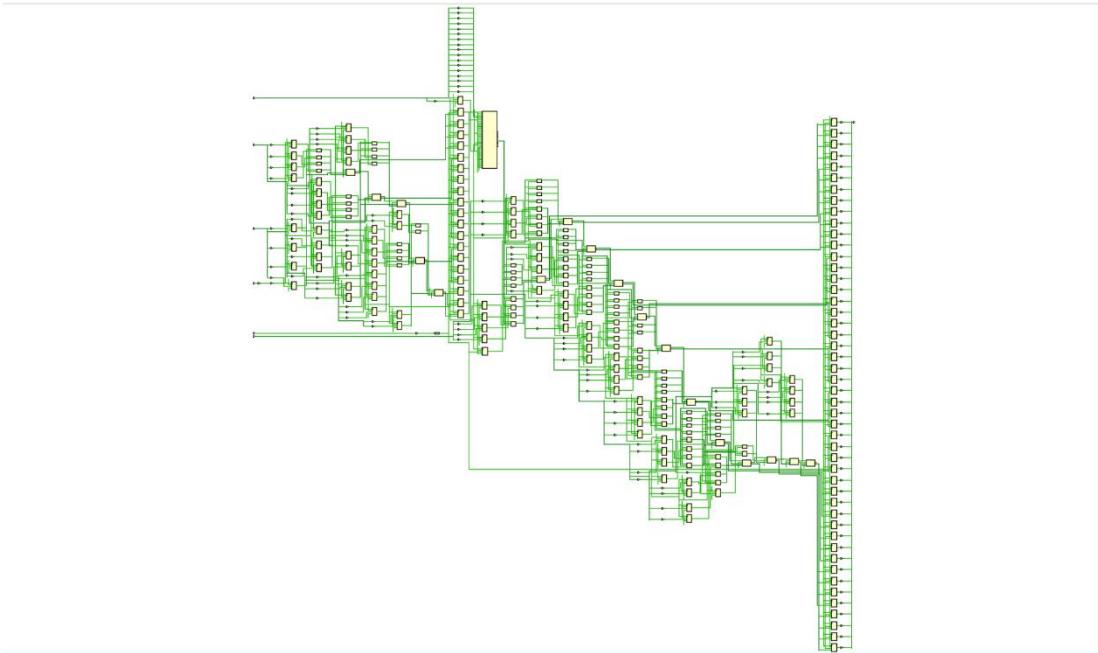
c) Synthesis

A screenshot of the Vivado IDE showing the synthesis log. The log window displays 20 warnings and 34 infos. Key messages include:

- [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
- [Synth 8-6157] synthesizing module 'DSP48A1_simplified' [q2.v.1]
- [Synth 8-6155] done synthesizing module 'DSP48A1_simplified' (1#1) [q2.v.1]
- [Device 21-403] Loading part xc7a200tff1156-3
- [Project 1-233] Implementation specific constraints were found while reading constraint file [D:/other/Courses/Kareem_waseem_Digital-Design/Ass/Ass4/Q2/synthesis/constraint/Constraints_basys3 - Copy.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [xil/DSP48A1_simplified_propimpl.xdc]. Resolution: To avoid this warning, move constraints listed in [Undefined:] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
- [Synth 8-4471] merging register 'A_reg_reg[17:0]' into 'A_reg_reg[17:0]' [q2.v.15]
- [Synth 8-6014] Unused sequential element A_reg_reg was removed. [q2.v.15]
- [Synth 8-3886] merging instance DBA_reg[37] (FDC) to DBA_reg[47] (9 more like this)
- [Synth 8-3333] propagating constant 0 across sequential element (DBA_reg[47])
- [Synth 8-3332] Sequential element (A_reg_reg[16]) is unused and will be removed from module DSP48A1_simplified. (17 more like this)
- [Synth 8-5844] Deleted registers with asynchronous reset at DSP/BRAM block boundary. Consider using synchronous reset for optimal packing [q2.v.19] (3 more like this)
- [Synth 8-5842] Cannot pack DSP OPMODE registers because of constant '1' value. Packing the registers will cause simulation mismatch at initial cycle [q2.v.15]
- [Project 1-571] Translating synthesized netlist
- [Netlist 29-17] Analyzing 122 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- [Opt 31-138] Pushed 0 inverter(s) to load pin(s).
- [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
- [Common 17-83] Releasing license: Synthesis
- [Constraints 18-521] No constraint will be written out.
- [Common 17-1381] The checkpoint D:/other/Courses/Kareem_waseem_Digital-Design/Ass/Ass4/Q2/synthesis/p2/O2_2/O2_2_runs/synth_1/DSP48A1_simplified.dcp has been generated.
- [runit-4] Executing: report_utilization -file DSP48A1_simplified_utilization_rpt.rpt -pb DSP48A1_simplified_utilization_synth.pb
- [Common 17-206] Exiting Vivado at Thu Jul 24 12:57:41 2025...



Synthesis schematic:



d) Implementation

```
✓ Implementation (1 warning, 89 infos)
  ✓ Design Initialization (11 infos)
    ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    ⓘ [Project 1-479] Netlist was created with Vivado 2018.2
    ⓘ [Device 21-403] Loading part xc7a200tffg1156-3
    ⓘ [Project 1-570] Preparing netlist for logic optimization
    ⓘ [Timing 38-478] Restoring timing data from binary archive.
    ⓘ [Timing 38-479] Binary timing data restore complete.
    ⓘ [Project 1-858] Restoring constraints from binary archive.
    ⓘ [Project 1-853] Binary constraint restore complete.
    ⓘ [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.
    ⓘ [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
  ✓ Opt Design (23 infos)
    ⓘ [Common 17-349] Got license for feature 'Implementation' and/or device xc7a200t
    ⓘ [Project 1-481] DRC finished with 0 Errors
    ⓘ [Project 1-462] Please refer to the DRC report (report_drc) for more information.
    ⓘ [Opt 31-49] Retargeted 0 cell(s).
    ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s). (1 more like this)
    > ⓘ [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
    ⓘ [Opt 31-562] Phase BUFQ optimization created 0 cells of which 0 are BUFQs and removed 0 cells.
    ⓘ [IPwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
    ⓘ [Common 17-83] Releasing license: Implementation
    ⓘ [Timing 38-480] Writing timing data to binary archive.
    ⓘ [Common 17-1384] The checkpoint 'D:/other/Courses/Kareem_waseem_Digital-Design/Ass/Ass4/Q2/synthesis/p2/Q2_2/Q2_2/runs/impl_1/DSP48A1_simplified_opt.dcp' has been generated.
    ⓘ [runrtl-4] Executing : report_drc -file DSP48A1_simplified_drc_opted.rpt -pb DSP48A1_simplified_drc_opted.pb -rpx DSP48A1_simplified_drc_opted.rpx
    ⓘ [IP_Flow 19-234] Refreshing IP repositories
    ⓘ [IP_Flow 19-1704] No user IP repositories specified
    ⓘ [IP_Flow 19-2313] Loaded Vivado IP repository 'D:/Prg/Vivado/Vivado/2018.2/data/ip'.
    > ⓘ [DRC 23-27] Running DRC with 2 threads (1 more like this)
    ⓘ [Corecl 2-168] The results of DRC are in file DSP48A1_simplified_drc_opted.rpt
  ✓ Place Design (21 infos)
    ⓘ [Common 17-349] Got license for feature 'Implementation' and/or device xc7a200t
    > ⓘ [DRC 23-27] Running DRC with 2 threads (1 more like this)
    > ⓘ [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
    > ⓘ [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
```

① [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs
 ① [Phyopt 32-65] No nets found for high-fanout optimization.
 ① [Phyopt 32-232] Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell
 > ① [Timing 38-35] Done setting XDC timing constraints. (1 more like this)
 ① [Place 46-31] BUFG insertion identified 0 candidate nets, 0 success, 0 skipped for placement/routing, 0 skipped for timing, 0 skipped for netlist change reason.
 ① [Place 30-748] Post Placement Timing Summary WNS=6.550. For the most accurate timing information please run report_timing.
 ① [Common 17-83] Releasing license: Implementation
 ① [Timing 38-480] Writing timing data to binary archive.
 ① [Common 17-1381] The checkpoint D:/other/Courses/Kareem_waseem_Digital-Design/Ass/Ass4/Q2/synthesis/p2/Q2_2/Q2_2/runs/impl_1/DSP48A1_simplified_placed.dcp has been generated.
 > ① [runtl-4] Executing : report_io -file DSP48A1_simplified_io_placed.rpt (2 more like this)
 ✓ Route Design (1 warning, 34 infos)
 ① [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
 ✓ DRC (1 warning)
 ✓ Pin Planning (1 warning)
 ① [DRC CFBVBS-7] CONFIG_VOLTAGE with Config Bank VCCO: The CONFIG_MODE property of current_design specifies a configuration mode (SP1x4) that uses pins in bank 14. I/O standards used in this bank have a voltage requirement of 1.80. However, the CONFIG_VOLTAGE for current_design is set to 3.3. Ensure that your configuration voltage is compatible with the I/O standards in banks used by your configuration mode. Refer to device configuration user guide for more information. Pins used by config mode: V28 (IO_L1P_TO_D00_MOSI_14), V29 (IO_L1N_TO_D01_DIN_14), V26 (IO_L2P_TO_D02_14), V27 (IO_L2N_TO_D03_14), W26 (IO_L3P_TO_D05_PUDC_B_14), and Y27 (IO_L6P_TO_FCS_B_14)
 ① [Vivado_Td 4-198] DRC finished with 0 Errors, 1 Warnings
 ① [Vivado_Td 4-199] Please refer to the DRC report (report_drc) for more information.
 ① [Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs
 > ① [Route 35-416] Intermediate Timing Summary | WNS=6.484 | TNS=0.000 | WHS=-0.082 | THS=-1.458 | (2 more like this)
 ① [Route 35-57] Estimated Timing Summary | WNS=6.546 | TNS=0.000 | WHS=0.181 | THS=0.000
 ① [Route 35-327] The final timing numbers are based on the router estimated timing analysis. For a complete and accurate timing signoff, please run report_timing_summary.
 ① [Route 35-16] Router Completed Successfully
 ① [Common 17-83] Releasing license: Implementation
 ① [Timing 38-480] Writing timing data to binary archive.
 ① [Common 17-1381] The checkpoint D:/other/Courses/Kareem_waseem_Digital-Design/Ass/Ass4/Q2/synthesis/p2/Q2_2/Q2_2/runs/impl_1/DSP48A1_simplified_routed.dcp has been generated.
 > ① [DRC 23-27] Running DRC with 2 threads (1 more like this)
 ① [Coretl 2-168] The results of DRC are in file DSP48A1_simplified_drc_routed.rpt.
 > ① [runtl-4] Executing : report_drc -file DSP48A1_simplified_drc_routed.rpt -pb DSP48A1_simplified_drc_routed.pb -rpx DSP48A1_simplified_drc_routed.rpx (7 more like this)
 > ① [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
 ① [DRC 23-133] Running Methodology with 2 threads
 ① [Coretl 2-1520] The results of Report Methodology are in file DSP48A1_simplified_methodology_drc_routed.rpt.
 ① [Vivado_Td 4-545] No incremental reuse to report, no incremental placement and routing data was found.
 > ① [Timing 38-91] UpdateTimingParams: Speed grade: -3, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
 > ① [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)

✓ Implemented Design (9 infos)
 ✓ General Messages (9 infos)
 ① [Netlist 29-17] Analyzing 122 Unisim elements for replacement
 ① [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 ① [Project 1-479] Netlist was created with Vivado 2018.2
 ① [Project 1-570] Preparing netlist for logic optimization
 ① [Timing 38-478] Restoring timing data from binary archive.
 ① [Timing 38-479] Binary timing data restore complete.
 ① [Project 1-856] Restoring constraints from binary archive.
 ① [Project 1-853] Binary constraint restore complete.
 ① [Project 1-111] Unisim Transformation Summary:
 No Unisim elements were transformed.

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing Utilization

Hierarchy

Name	Slice LUTs (133800)	Slice Registers (267600)	Slice (3345 0)	LUT as Logic (133800)	LUT Flip Flop Pairs (133800)	DSP s (740)	Bonded IOB (500)	BUFOCTRL (32)
N DSP48A1_simplified	56	153	39	56	55	1	152	1

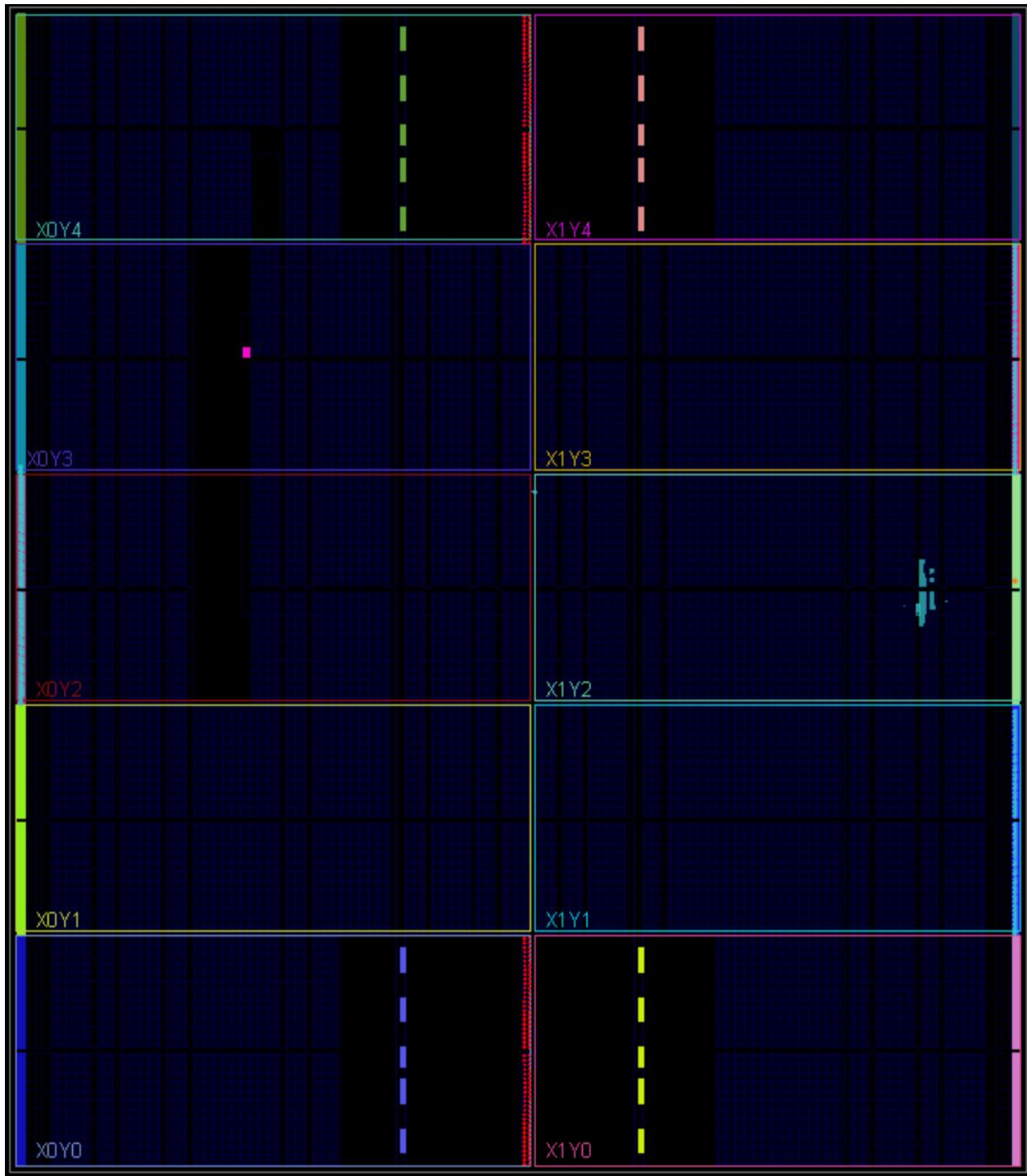
Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing Utilization

Design Timing Summary

Setup		Hold		Pulse Width	
General Information		Worst Negative Slack (WNS): 6.547 ns	Worst Hold Slack (WHS): 0.182 ns	Worst Pulse Width Slack (WPWS): 4.500 ns	
Timer Settings		Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns	
Design Timing Summary		Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	
Clock Summary (1)		Total Number of Endpoints: 107	Total Number of Endpoints: 107	Total Number of Endpoints: 155	
> Check Timing (151)					
> Intra-Clock Paths					

All user specified timing constraints are met.

Timing Summary - impl_1 (saved)



Linting:

Vuesta Lint 2021.1 (..git/Design/Ass/Ass4/Q2/Linting/lint.db)

File Edit View Lint Checks Window Help

Design Search: Type S... Instance DSP48A1... Module DSP48A1_simplified

D:/other/Courses/Kareem_waseem_Digital-Design/Ass/Ass4/Q2/Linting/q2.v [DSP48A1_simplified]

```
1 module DSP48A1_simplified (P, A, B, D, C, clkx, rst_n);
2     parameter OPERATION = "ADD";
3     ADD
4     input [17:0] A, B, D;
5     input [47:0] C;
6     input clk, rst_n;
7     output reg [47:0] P;
8
9     reg [17:0] A_reg, B_reg, D_reg;
10    reg [47:0] C_reg;
11    reg [18:0] DB;
12    reg [47:0] DBA;
13
14    always @ (posedge clk) begin
15        A_reg <= A; B_reg <= B; D_reg <= D; C_reg <= C;
16    end
17    always @ (posedge clk or negedge rst_n) begin
18        if(!rst_n)begin
19            DB <> 0;
20            DBA <= 0;
21            P <= 0;
22        end
23        else begin
24            if(OPERATION == "ADD")begin
25                DB <= D_reg + B_reg;
26                DBA <= DB * A_reg;
27                P <= DBA + C_reg;
28            end
29            else begin
30                DB <= D_reg - B_reg;
31                DBA <= DB * A_reg;
32                P <= DBA + C_reg;
33            end
34        end
35    end
36
```

Lint Summary
(Type Search Text (Press Enter))

Name	Count
Resolved(verified, fi...)	1
Info	1

Flow Na... D... Lint Checks

Filter: Type here

severity	Status	Check	Alias	Message	Module	Category	State	Owner	STARC Reference
Info	Waived	Fixed	Pending	Unspecified	Bug	Verified	Total : 1 Selected : 0		
Info	Info	multi_ports_in_single_line		Multiple ports are declared in one line. Module DSP48A1_simplified, File D:/other/Courses/Kareem_waseem_Digital-Design/Ass/Ass4/Q2/Linting/q2.v [DSP48A1_simplified]	DSP48A1_simplified	Rtl Design	resolved	unassigned	3.5.6.3

Transcript Message Viewer Lint Checks Design Metrics Design Information Status History Lint Dashboard

D:/other/Courses/Kareem_waseem_Digital-Design/Ass/Ass4/Q2/Linting/q2.v [DSP48A1_simplified]

Q3)

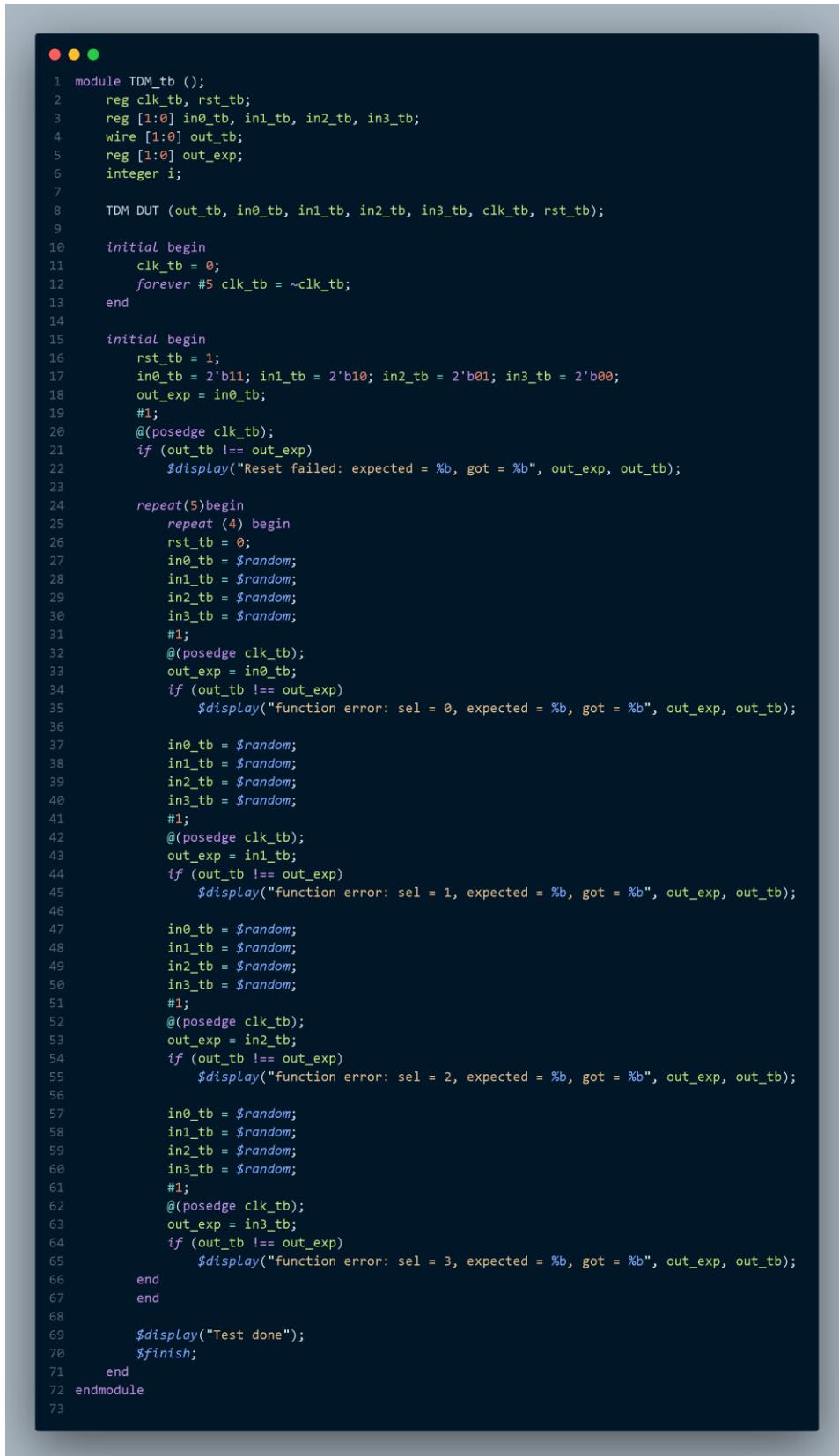
Verilog Code:

a) RTL design

```
● ● ●

1 module TDM (out, in0, in1, in2, in3, clk, rst);
2     input clk;
3     input rst;
4     input [1:0] in0, in1, in2, in3;
5     output reg [1:0] out;
6     reg [1:0] S;
7
8     always @(posedge clk or posedge rst) begin
9         if (rst)
10             S <= 2'b00;
11         else
12             S <= S + 1;
13     end
14
15    always @(*) begin
16        case (S)
17            2'b00: out = in0;
18            2'b01: out = in1;
19            2'b10: out = in2;
20            2'b11: out = in3;
21        endcase
22    end
23
24 endmodule
25
```

b) Testbench



```
1 module TDM_tb ();
2   reg clk_tb, rst_tb;
3   reg [1:0] in0_tb, in1_tb, in2_tb, in3_tb;
4   wire [1:0] out_tb;
5   reg [1:0] out_exp;
6   integer i;
7
8   TDM DUT (out_tb, in0_tb, in1_tb, in2_tb, in3_tb, clk_tb, rst_tb);
9
10 initial begin
11   clk_tb = 0;
12   forever #5 clk_tb = ~clk_tb;
13 end
14
15 initial begin
16   rst_tb = 1;
17   in0_tb = 2'b11; in1_tb = 2'b10; in2_tb = 2'b01; in3_tb = 2'b00;
18   out_exp = in0_tb;
19   #1;
20   @(posedge clk_tb);
21   if (out_tb !== out_exp)
22     $display("Reset failed: expected = %b, got = %b", out_exp, out_tb);
23
24 repeat(5)begin
25   repeat (4) begin
26     rst_tb = 0;
27     in0_tb = $random;
28     in1_tb = $random;
29     in2_tb = $random;
30     in3_tb = $random;
31     #1;
32     @(posedge clk_tb);
33     out_exp = in0_tb;
34     if (out_tb !== out_exp)
35       $display("function error: sel = 0, expected = %b, got = %b", out_exp, out_tb);
36
37     in0_tb = $random;
38     in1_tb = $random;
39     in2_tb = $random;
40     in3_tb = $random;
41     #1;
42     @(posedge clk_tb);
43     out_exp = in1_tb;
44     if (out_tb !== out_exp)
45       $display("function error: sel = 1, expected = %b, got = %b", out_exp, out_tb);
46
47     in0_tb = $random;
48     in1_tb = $random;
49     in2_tb = $random;
50     in3_tb = $random;
51     #1;
52     @(posedge clk_tb);
53     out_exp = in2_tb;
54     if (out_tb !== out_exp)
55       $display("function error: sel = 2, expected = %b, got = %b", out_exp, out_tb);
56
57     in0_tb = $random;
58     in1_tb = $random;
59     in2_tb = $random;
60     in3_tb = $random;
61     #1;
62     @(posedge clk_tb);
63     out_exp = in3_tb;
64     if (out_tb !== out_exp)
65       $display("function error: sel = 3, expected = %b, got = %b", out_exp, out_tb);
66   end
67 end
68
69 $display("Test done");
70 $finish;
71 end
72 endmodule
73
```

Simulation Tool

a) Do file



```
1 vlib work
2 vlog q3.v q3_tb.v
3 vsim -voptargs=+acc work.TDM_tb
4 add wave *
5 run -all
6 #quit -sim
```

b) Questasim

```
# Elapsed time: 00:00:00.00 on Sun Jul 24, 2025, Elapsed time: 0.000000
# Errors: 0, Warnings: 0
# vsim -voptargs=+acc" work.TDM_tb
# Start time: 16:40:59 on Jul 24,2025
# ** Note: (vsim-3813) Design is being optimized due to module recompilation...
# Loading work.TDM_tb(fast)
# Loading work.TDM(fast)
# Test done
# ** Note: $finish : q3_tb.v(70)
# Time: 805 ns Iteration: 1 Instance: /TDM_tb
```



Synthesis Tool:

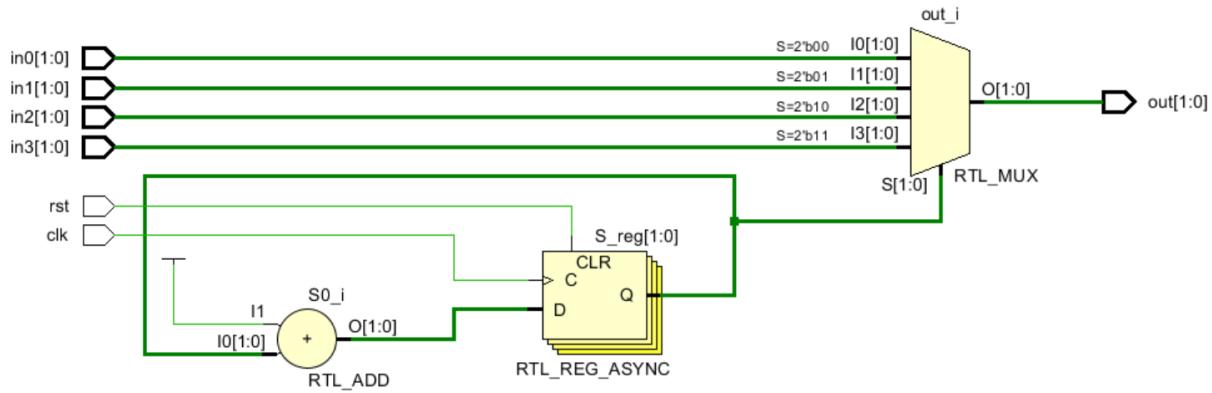
a) Constraint file

```
6  ## Clock signal
7  set_property -dict { PACKAGE_PIN W5    IOSTANDARD LVC MOS33 } [get_ports clk]
8  create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
9
10
11 ## Switches
12 set_property -dict { PACKAGE_PIN V17  IOSTANDARD LVC MOS33 } [get_ports {in0[0]}]
13 set_property -dict { PACKAGE_PIN V16  IOSTANDARD LVC MOS33 } [get_ports {in0[1]}]
14 set_property -dict { PACKAGE_PIN W16  IOSTANDARD LVC MOS33 } [get_ports {in1[0]}]
15 set_property -dict { PACKAGE_PIN W17  IOSTANDARD LVC MOS33 } [get_ports {in1[1]}]
16 set_property -dict { PACKAGE_PIN W15  IOSTANDARD LVC MOS33 } [get_ports {in2[0]}]
17 set_property -dict { PACKAGE_PIN V15  IOSTANDARD LVC MOS33 } [get_ports {in2[1]}]
18 set_property -dict { PACKAGE_PIN W14  IOSTANDARD LVC MOS33 } [get_ports {in3[0]}]
19 set_property -dict { PACKAGE_PIN W13  IOSTANDARD LVC MOS33 } [get_ports {in3[1]}]
20 #set_property -dict { PACKAGE_PIN V2    IOSTANDARD LVC MOS33 } [get_ports {sw[8]}]
21 #set_property -dict { PACKAGE_PIN T3    IOSTANDARD LVC MOS33 } [get_ports {sw[9]}]
22 #set_property -dict { PACKAGE_PIN T2    IOSTANDARD LVC MOS33 } [get_ports {sw[10]}]
23 #set_property -dict { PACKAGE_PIN R3    IOSTANDARD LVC MOS33 } [get_ports {sw[11]}]
24 #set_property -dict { PACKAGE_PIN W2    IOSTANDARD LVC MOS33 } [get_ports {sw[12]}]
25 #set_property -dict { PACKAGE_PIN U1    IOSTANDARD LVC MOS33 } [get_ports {sw[13]}]
26 #set_property -dict { PACKAGE_PIN T1    IOSTANDARD LVC MOS33 } [get_ports {sw[14]}]
27 #set_property -dict { PACKAGE_PIN R2    IOSTANDARD LVC MOS33 } [get_ports {sw[15]}]
28
29
30 ## LEDs
31 set_property -dict { PACKAGE_PIN U16  IOSTANDARD LVC MOS33 } [get_ports {out[0]}]
32 set_property -dict { PACKAGE_PIN E19  IOSTANDARD LVC MOS33 } [get_ports {out[1]}]
33
34
35 ## Buttons
36 set_property -dict { PACKAGE_PIN U18  IOSTANDARD LVC MOS33 } [get_ports rst]
```

b) Elaboration

Elaborated Design (6 infos)

- General Messages (6 infos)
 - [Synth 8-6157] synthesizing module 'TDM' [q3.v:1]
 - [Synth 8-6155] done synthesizing module 'TDM' (#1) [q3.v:1]
 - [Device 21-403] Loading part xc7a35tcpg236-1L
 - [Project 1-570] Preparing netlist for logic optimization
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.



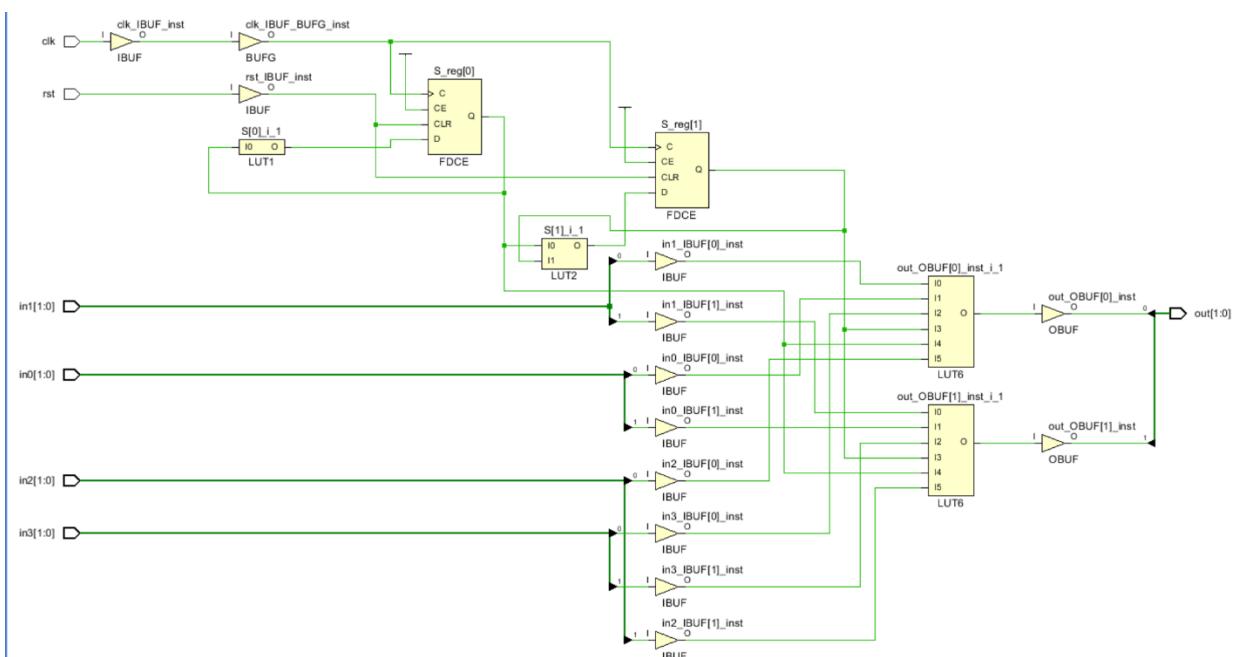
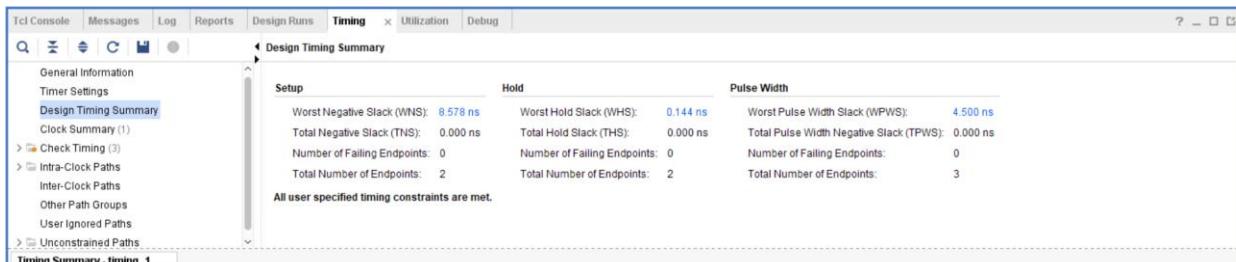
c) Synthesis

synthesis (1 warning, 17 infos)

- [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
- [Synth 8-6157] synthesizing module 'TDM' [q3.v1]
- [Synth 8-6155] done synthesizing module TDM (#1) [q3.v1]
- [Device 21-403] Loading part xc7a35tcpg236-1L
- [Project 1-236] Implementation specific constraints were found while reading constraint file [D:/other/Courses/Kareem_waseem_Digital-Design/Ass/Ass4/Q3/synthesis/Constraint/Constraints_basys3 - Copy.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [xil/TDM_propimpl.xdc]. Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
- [Project 1-571] Translating synthesized netlist
- [Netlist 29-17] Analyzing 10 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
- [Common 17-83] Releasing license: Synthesis
- [Constraints 18-5210] No constraint will be written out.
- [Common 17-1381] The checkpoint D:/other/Courses/Kareem_waseem_Digital-Design/Ass/Ass4/Q3/synthesis/p1/Q3_1/Q3_1/runs/synth_1/TDM.dcp has been generated.
- [rundl-4] Executing : report_utilization_rpt -pb TDM_utilization_synth.rpt -pb TDM_utilization_synth.pb
- [Common 17-206] Exiting Vivado at Thu Jul 24 17:06:29 2025..

Synthesized Design (6 infos)

- [Netlist 29-17] Analyzing 10 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-479] Netlist was created with Vivado 2018.2
- [Project 1-570] Preparing netlist for logic optimization
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

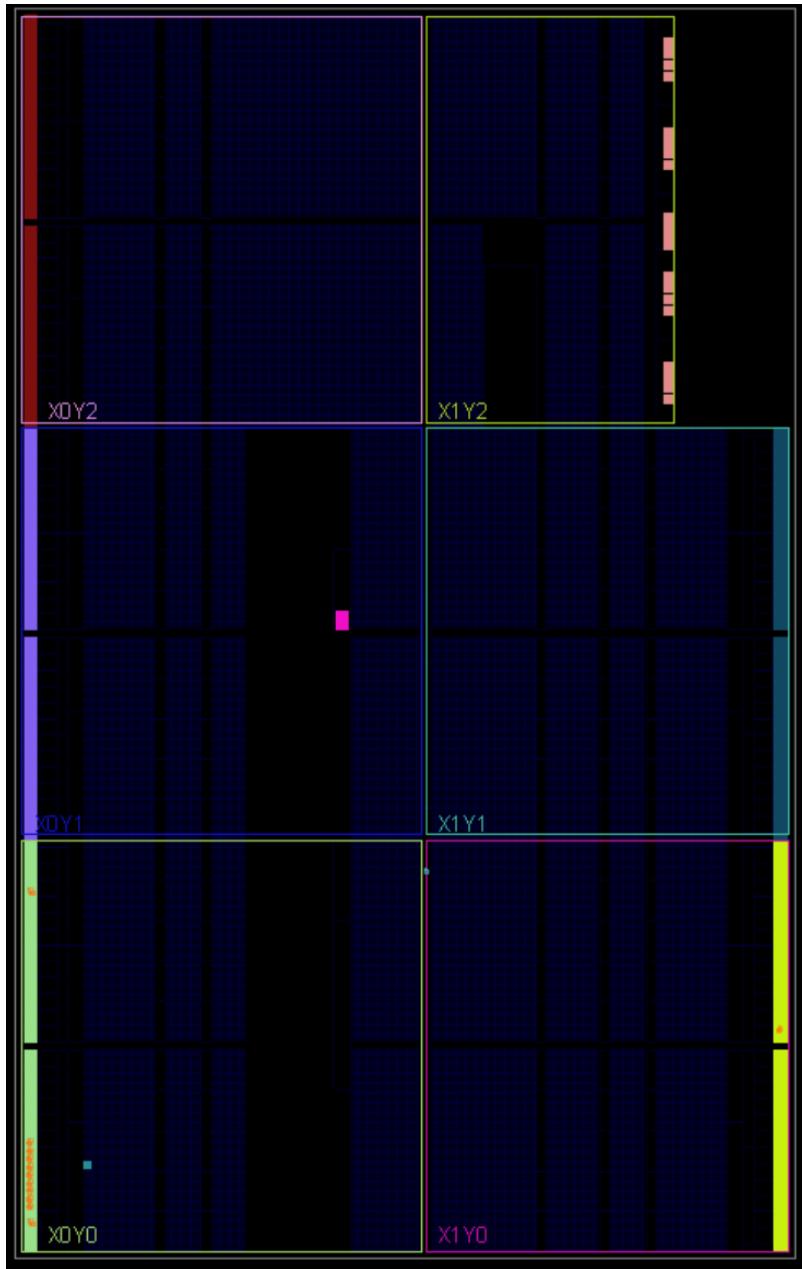


d) Implementation

Implementation (90 infos)
Design Initialization (11 infos)
<i>[Netlist 29-17] Analyzing 10 Unisim elements for replacement</i>
<i>[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds</i>
<i>[Project 1-479] Netlist was created with Vivado 2018.2</i>
<i>[Device 21-403] Loading part xc7a35tfcpg236-1L</i>
<i>[Project 1-570] Preparing netlist for logic optimization</i>
<i>[Timing 38-478] Restoring timing data from binary archive.</i>
<i>[Timing 38-479] Binary timing data restore complete.</i>
<i>[Project 1-856] Restoring constraints from binary archive.</i>
<i>[Project 1-853] Binary constraint restore complete.</i>
<i>[Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed.</i>
<i>[Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646</i>
Opt Design (23 infos)
<i>[Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35l'</i>
<i>[Project 1-461] DRC finished with 0 Errors</i>
<i>[Project 1-462] Please refer to the DRC report (report_drc) for more information.</i>
<i>[Opt 31-40] Retargeted 0 cell(s).</i>
> <i>[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s). (1 more like this)</i>
> <i>[Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)</i>
<i>[Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.</i>
<i>[Pwrop 34-132] Skipping clock gating for clocks with a period < 2.00 ns.</i>
<i>[Common 17-83] Releasing license: Implementation</i>
<i>[Timing 38-480] Writing timing data to binary archive.</i>
<i>[Common 17-1381] The checkpoint D:/other/Courses/Kareem_waseem_Digital-Design/Ass/Ass4/Q3/synthesis/p1/Q3_1/Q3_1.runs/impl_1/TDM_opt.dcp has been generated.</i>
<i>[runtd-4] Executing : report_drc -file TDM_drc_opted.rpt -pb TDM_drc_opted.rpx</i>
<i>[IP_Flow 19-234] Refreshing IP repositories</i>
<i>[IP_Flow 19-1704] No user IP repositories specified</i>
<i>[IP_Flow 19-2313] Loaded Vivado IP repository D:/Prg/Vivado/Vivado/2018.2/datalip.</i>
> <i>[DRC 23-27] Running DRC with 2 threads (1 more like this)</i>
<i>[Coretd 2-168] The results of DRC are in file TDM_drc_opted.rpt.</i>
Place Design (21 infos)
<i>[Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35l'</i>
> <i>[DRC 23-27] Running DRC with 2 threads (1 more like this)</i>
> <i>[Vivado_Td 4-198] DRC finished with 0 Errors (1 more like this)</i>
> <i>[Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)</i>
Route Design (35 infos)
<i>[Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35l'</i>
<i>[Vivado_Td 4-198] DRC finished with 0 Errors</i>
<i>[Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.</i>
<i>[Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs</i>
> <i>[Route 35-416] Intermediate Timing Summary WNS=8.387 TNS=0.000 WHS=0.008 THS=0.000 (3 more like this)</i>
<i>[Route 35-57] Estimated Timing Summary WNS=8.331 TNS=0.000 WHS=0.394 THS=0.000 </i>
<i>[Route 35-327] The final timing numbers are based on the router estimated timing analysis. For a complete and accurate timing signoff, please run report_timing_summary.</i>
<i>[Route 35-16] Router Completed Successfully</i>
<i>[Common 17-83] Releasing license: Implementation</i>
<i>[Timing 38-480] Writing timing data to binary archive.</i>
<i>[Common 17-1381] The checkpoint D:/other/Courses/Kareem_waseem_Digital-Design/Ass/Ass4/Q3/synthesis/p1/Q3_1/Q3_1.runs/impl_1/TDM_placed.dcp has been generated.</i>
<i>[runtd-4] Executing : report_lo -file TDM_lo_placed.rpt (2 more like this)</i>
<i>[DRC 23-27] Running DRC with 2 threads (1 more like this)</i>
<i>[Coretd 2-168] The results of DRC are in file TDM_drc_routed.rpt</i>
> <i>[runtd-4] Executing : report_drc -file TDM_drc_routed.rpt -pb TDM_drc_routed.pb -px TDM_drc_routed.rpx (7 more like this)</i>
> <i>[Timing 38-35] Done setting XDC timing constraints. (2 more like this)</i>
<i>[DRC 23-133] Running Methodology with 2 threads</i>
<i>[Coretd 2-1520] The results of Report Methodology are in file TDM_methodology_drc_routed.rpt.</i>
<i>[Vivado_Td 4-545] No incremental reuse to report, no incremental placement and routing data was found.</i>
> <i>[Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max, Timing Stage: Required. (1 more like this)</i>
<i>[Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)</i>
Implemented Design (9 infos)
General Messages (9 infos)
<i>[Netlist 29-17] Analyzing 10 Unisim elements for replacement</i>
<i>[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds</i>
<i>[Project 1-479] Netlist was created with Vivado 2018.2</i>
<i>[Project 1-570] Preparing netlist for logic optimization</i>
<i>[Timing 38-478] Restoring timing data from binary archive.</i>
<i>[Timing 38-479] Binary timing data restore complete.</i>
<i>[Project 1-856] Restoring constraints from binary archive.</i>
<i>[Project 1-853] Binary constraint restore complete.</i>
<i>[Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed.</i>

Hierarchy							
Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
TDM	3	2	1	3	1	12	1

Design Timing Summary		
General Information	Setup	Hold
Timer Settings	Worst Negative Slack (WNS): 8.358 ns	Worst Hold Slack (WHS): 0.411 ns
Design Timing Summary	Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns
Clock Summary (1)	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
> Check Timing (3)	Total Number of Endpoints: 2	Total Number of Endpoints: 2
> Intra-Clock Paths		
All user specified timing constraints are met.		



Linting:

The screenshot shows the Questa Lint 2021.1 interface. The main window displays a Verilog module named `TDM`. The code includes an always block with a case statement based on the value of `S`, which is updated via an if-else block triggered by the rising edge of `clk` or the falling edge of `rst`.

```
module TDM (out, in0, in1, in2, in3, clk, rst);
    input clk;
    input rst;
    input [1:0] in0, in1, in2, in3;
    output reg [1:0] out;
    reg [1:0] S;

    always @(posedge clk or posedge rst) begin
        if (rst)
            S <= 2'b00;
        else
            S <= S + 1;
    end

    always @(*) begin
        case (S)
            2'b00: out = in0;
            2'b01: out = in1;
            2'b10: out = in2;
            2'b11: out = in3;
        endcase
    end
endmodule
```

The right side of the interface shows the **Lint Summary** window, which lists two findings:

Name	Count
Resolved(verified, fi...)	2
Info	2

Below the summary is a detailed view of the lint checks, showing two entries:

Severity	Status	Check	Alias	Message	Module	Category	State	Owner	STAI
Info	Waived	async_reset_active_high		Asynchronous reset is active high. Reset rst, Module TDM, File D:/other/Courses/Kareem_waseem_Digital-Design/Ass/Ass4/Q3/Linting/q3.v	TDM	Clock	resolved	unass...	2.3.6.2
Info	Waived	multi_ports_in_single_line		Multiple ports are declared in one line. Module TDM, File D:/other/Courses/Kareem_waseem_Digital-Design/Ass/Ass4/Q3/Linting/q3.v	TDM	Rtl Design ...	resolved	unass...	3.5.6.3