

Assignment 5

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1) Q1

1.RTL code

1. TOP_Module

```
1 module control_unit (unlock_doors, accelerate_car, speed_limit, car_speed, leading_distance, clk, rst);
2   parameter MIN_DISTANCE = 7'd40;
3   parameter STOP = 2'b00;
4   parameter ACCELERATE = 2'b01;
5   parameter DECELERATE = 2'b10;
6
7   input [7:0] speed_limit, car_speed ;
8   input [6:0] leading_distance ;
9   input clk, rst;
10
11  output reg unlock_doors, accelerate_car;
12  reg [1:0] cs, ns;
13
14 //state memory
15 always @(posedge clk or posedge rst) begin
16   if(rst)begin
17     cs <= STOP;
18   end
19   else begin
20     cs <= ns;
21   end
22 end
23
24 //next state logic
25 always @(cs , speed_limit , car_speed , leading_distance) begin
26   case (cs)
27     STOP:
28       begin
29         if(leading_distance<MIN_DISTANCE)
30           ns=STOP;
31         else
32           ns=ACCELERATE;
33       end
34
35     ACCELERATE:
36       begin
37         if((leading_distance>=MIN_DISTANCE) && (car_speed<speed_limit))
38           ns=ACCELERATE;
39         else
40           ns=DECELERATE;
41       end
42
43
44     DECELERATE:
45       begin
46         if(car_speed == 0)
47           ns=STOP;
48         else if((leading_distance<MIN_DISTANCE) || (car_speed>speed_limit))
49           ns=DECELERATE;
50         else
51           ns=ACCELERATE;
52       end
53
54     default : ns = STOP;
55   endcase
56 end
57
58 //output logic
59 always @(cs) begin
60   case (cs)
61     STOP:
62       begin
63         unlock_doors = 1;
64         accelerate_car = 0;
65       end
66     ACCELERATE:
67       begin
68         unlock_doors = 0;
69         accelerate_car = 1;
70       end
71
72     DECELERATE:
73       begin
74         unlock_doors = 0;
75         accelerate_car = 0;
76       end
77   endcase
78 end
79 endmodule
```

2. Testbench code

```
 1 module control_unit_tb ();
 2     parameter MIN_DISTANCE_tb = 7'd40;
 3
 4     reg [7:0] speed_limit_tb, car_speed_tb ;
 5     reg [6:0] leading_distance_tb ;
 6     reg clk_tb, rst_tb;
 7
 8     wire unlock_doors_tb, accelerate_car_tb;
 9
10    control_unit #(.MIN_DISTANCE(MIN_DISTANCE_tb)) DUT (unlock_doors_tb, accelerate_car_tb, speed_limit_tb, car_speed_tb, leading_distance_tb, clk_tb, rst_tb);
11
12    initial begin
13        clk_tb = 0;
14        forever begin
15            #1 clk_tb = ~clk_tb;
16        end
17    end
18
19    initial begin
20        rst_tb = 1;
21        speed_limit_tb = 8'd60;
22        car_speed_tb = 8'd0;
23        leading_distance_tb = 7'd30;
24
25        #10 rst_tb = 0;
26
27        #10;
28        $display("Test1: STOP state, distance = %d, speed = %d, limit = %d, unlock = %b, accel = %b",
29                 leading_distance_tb, car_speed_tb, speed_limit_tb, unlock_doors_tb, accelerate_car_tb);
30
31        @(negedge clk_tb);
32        #10 car_speed_tb = 8'd30;
33        leading_distance_tb = 7'd50;
34        #10;
35        $display("Test 2: ACCELERATE state, distance = %d, speed = %d, limit = %d, unlock = %b, accel = %b",
36                 leading_distance_tb, car_speed_tb, speed_limit_tb, unlock_doors_tb, accelerate_car_tb);
37
38        @(negedge clk_tb);
39        #5 car_speed_tb = 8'd70;
40        leading_distance_tb = 7'd50;
41        #10;
42        $display("Test 3: DECELERATE state, distance = %d, speed = %d, limit = %d, unlock = %b, accel = %b",
43                 leading_distance_tb, car_speed_tb, speed_limit_tb, unlock_doors_tb, accelerate_car_tb);
44
45        @(negedge clk_tb);
46        #5 car_speed_tb = 8'd50;
47        leading_distance_tb = 7'd30;
48        #10;
49        $display("Test 4: DECELERATE state, distance = %d, speed = %d, limit = %d, unlock = %b, accel = %b",
50                 leading_distance_tb, car_speed_tb, speed_limit_tb, unlock_doors_tb, accelerate_car_tb);
51
52        @(negedge clk_tb);
53        #5 car_speed_tb = 8'd0;
54        leading_distance_tb = 7'd30;
55        #10;
56        $display("Test 5: DECELERATE to STOP, distance = %d, speed = %d, limit = %d, unlock = %b, accel = %b",
57                 leading_distance_tb, car_speed_tb, speed_limit_tb, unlock_doors_tb, accelerate_car_tb);
58
59
60        #10 $finish;
61    end
62
63 endmodule
```

3. Do file

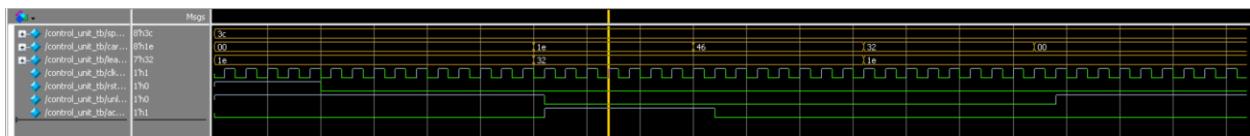
```
● ● ●  
1 vlib work  
2 vlog q1.v q1_tb.v  
3 vsim -voptargs+=acc work.control_unit_tb  
4 add wave *  
5 run -all  
6 #quit -sim
```

4. QuestaSim Snippets

Messages Snippet

```
# Top level modules:  
#     control_unit_tb  
# End time: 08:35:58 on Aug 18,2025, Elapsed time: 0:00:00  
# Errors: 0, Warnings: 0  
# vsim -voptargs="+acc" work.control_unit_tb  
# Start time: 08:35:58 on Aug 18,2025  
# ** Note: (vsim-3813) Design is being optimized due to module recompilation...  
# Loading work.control_unit_tb(fast)  
# Loading work.control_unit(fast)  
# Test1: STOP state, distance = 30, speed = 0, limit = 60, unlock = 1, accel = 0  
# Test 2: ACCELERATE state, distance = 50, speed = 30, limit = 60, unlock = 0, accel = 1  
# Test 3: DECELERATE state, distance = 50, speed = 70, limit = 60, unlock = 0, accel = 0  
# Test 4: DECELERATE state, distance = 30, speed = 50, limit = 60, unlock = 0, accel = 0  
# Test 5: DECELERATE to STOP, distance = 30, speed = 0, limit = 60, unlock = 1, accel = 0  
# ** Note: $finish : ql_tb.v(60)  
#     Time: 97 ns  Iteration: 0  Instance: /control_unit_tb
```

Waveform Snippet



5. Constraint File

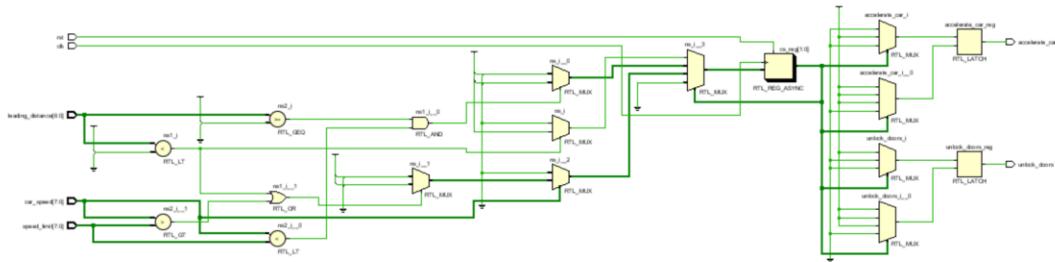
```
6  ## Clock signal  
7  set_property -dict { PACKAGE_PIN W5    IO_STANDARD LVCMS33 } [get_ports clk]  
8  create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]  
9  
10  
11  ##Buttons  
12  set_property -dict { PACKAGE_PIN U18    IO_STANDARD LVCMS33 } [get_ports rst]  
13  #set_property -dict { PACKAGE_PIN T18    IO_STANDARD LVCMS33 } [get_ports btnu]
```

6. Elaboration

Message tab

```
v Vivado Commands (3 infos, 4 status messages)
  v General Messages (3 infos, 4 status messages)
    i [IP_Flow 19-234] Refreshing IP repositories
    i [IP_Flow 19-1704] No user IP repositories specified
    i [IP_Flow 19-2313] Loaded Vivado IP repository 'D:/Prg/Vivado/Vivado/2018.2/data/ip'
  > i Command: synth_design -rtl -name rtl_1 (3 more like this)
v Elaborated Design (7 infos, 7 status messages)
  v General Messages (7 infos, 7 status messages)
    i [Synth 8-6157] synthesizing module 'control_unit' [q1.v:1]
    i [Synth 8-155] case statement is not full and has no default [q1.v:60]
    i [Synth 8-6155] done synthesizing module 'control_unit' (#1) [q1.v:1]
    i [Device 21-403] Loading part:xc7a35tcpg236-1L
    i [Project 1-570] Preparing netlist for logic optimization
  > i Processing XDC Constraints (5 more like this)
    i [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    i [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.
```

Schematic



7. Synthesis

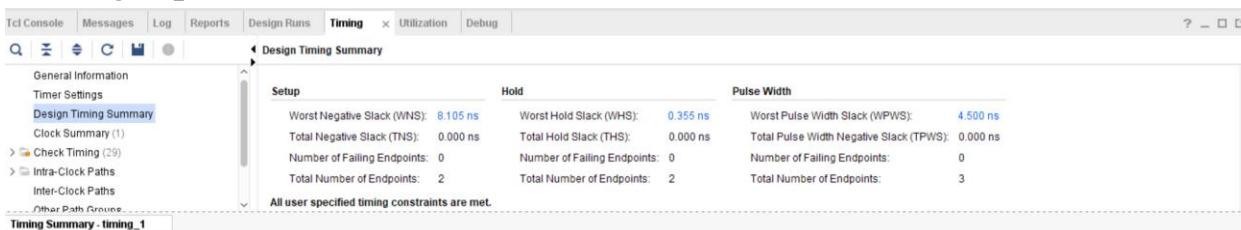
Message Tab

```
> [Synthesis] Command: synth_design -top control_unit -part xc7a35lcp236-1L (10 more like this)
  [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35l'
  [Synth 8-157] synthesizing module 'control_unit' [q1:v1]
  [Synth 8-155] case statement is not full and has no default [q1:v60]
  [Synth 8-155] done synthesizing module 'control_unit' (#1) [q1:v1]
  [Device 21-403] Loading part xc7a35lcp236-1L
  [Project 1-238] Implementation specific constraints were found while reading constraint file [D:/other/Courses/Kareem_waseem_Digital_Design/Ass/Ass5/Q1/synthesis/Constraints_basy3 - Copy.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [xil/control_unit_propimpl.xdc].
  Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
  [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'control_unit'
  > [Synth 8-554] ROM 'unlock_doors' won't be mapped to Block RAM because address size (2) smaller than threshold (5) (2 more like this)
  [Synth 8-335] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'control_unit'
  > [Synth 8-327] inferring latch for variable 'unlock_doors_reg' [q1:v63] (1 more like this)
  [Project 1-571] Translating synthesized netlist
  [Netlist 29-17] Analyzing 26 Unisim elements for replacement
  [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
  [Project 1-570] Preparing netlist for logic optimization (1 more like this)
  [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
  > [Project 1-111] Unisim Transformation Summary:
    No Unisim elements were transformed. (1 more like this)
  [Common 17-83] Releasing license: Synthesis
  [Constraints 18-5210] No constraint will be written out.
  [Common 17-138] The checkpoint D:/other/Courses/Kareem_waseem_Digital_Design/Ass/Ass5/Q1/synthesis/project_1/project_1.rpt has been generated.
  [jruntd-4] Executing : report_utilization -file control_unit_utilization_synth.rpt -pb control_unit_utilization_synth.pb
  [Common 17-206] Exiting Vivado at Mon Aug 18 08:48:56 2025...
```

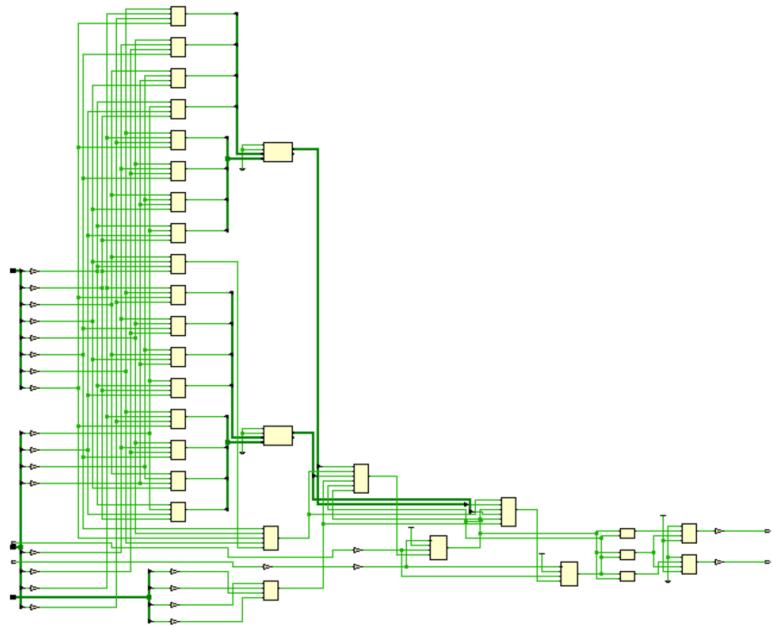
Utilization report



Timing report



Schematic



1. Netlist

```
18 // module control_unit
19 // (unlock_doors,
20 // accelerate_car,
21 // speed_limit,
22 // car_speed,
23 // leading_distance,
24 // clk,
25 // rst);
26 output unlock_doors;
27 output accelerate_car;
28 input [7:0]speed_limit;
29 input [7:0]car_speed;
30 input [6:0]leading_distance;
31 input clk;
32 input rst;
33
34 wire vconst0 ;
35 wire vconst1 ;
36 wire [FSM_sequential_cs[1].i_10_n_0];
37 wire [FSM_sequential_cs[1].i_11_n_0];
38 wire [FSM_sequential_cs[1].i_12_n_0];
39 wire [FSM_sequential_cs[1].i_13_n_0];
40 wire [FSM_sequential_cs[1].i_14_n_0];
41 wire [FSM_sequential_cs[1].i_15_n_0];
42 wire [FSM_sequential_cs[1].i_16_n_0];
43 wire [FSM_sequential_cs[1].i_17_n_0];
44 wire [FSM_sequential_cs[1].i_18_n_0];
45 wire [FSM_sequential_cs[1].i_19_n_0];
46 wire [FSM_sequential_cs[1].i_20_n_0];
47 wire [FSM_sequential_cs[1].i_21_n_0];
48 wire [FSM_sequential_cs[1].i_22_n_0];
49 wire [FSM_sequential_cs[1].i_3_n_0];
50 wire [FSM_sequential_cs[1].i_5_n_0];
51 wire [FSM_sequential_cs[1].i_6_n_0];
52 wire [FSM_sequential_cs[1].i_7_n_0];
53 wire [FSM_sequential_cs[1].i_8_n_0];
54 wire [FSM_sequential_cs[1].i_9_n_0];
55 wire [FSM_sequential_cs_reg[1].i_2_n_0];
56 wire [FSM_sequential_cs_reg[1].i_2_n_1];
57 wire [FSM_sequential_cs_reg[1].i_2_n_2];
58 wire [FSM_sequential_cs_reg[1].i_2_n_3];
59 wire [FSM_sequential_cs_reg[1].i_4_n_0];
60 wire [FSM_sequential_cs_reg[1].i_4_n_1];
61 wire [FSM_sequential_cs_reg[1].i_4_n_2];
62 wire [FSM_sequential_cs_reg[1].i_4_n_3];
63 wire GND_2;
64 wire VCC_2;
65 wire accelerate_car;
66 wire accelerate_car_OBUF;
67 wire accelerate_car_reg_i_1_n_0;
68 wire [7:0]car_speed;
69 wire [7:0]car_speed_IBUF;
70 wire clk;
71 wire clk_IBUF;
72 wire clk_IBUF_BUFG;
73 (* XIL_KEEP = "yes" *) wire [1:0]cs;
74 wire [6:0]leading_distance;
```

8. Implementation

Message Tab

The screenshot shows the Vivado IDE's Message Tab. The tab title is "Messages" and it contains a list of messages categorized by type: Warning (3), Info (213), and Status (459). The list includes:

- Design Initialization (11 infos, 7 status messages):
 - Command open_checkpoint D:/other/Courses/Kareem_waseem_Digital_Design/Ass/Ass5/Q1/synthesis/project_1/runs/impl_1/control_unit.dcp (6 more like this)
 - [Nellist 29-17] Analyzing 24 Unisim elements for replacement
 - [Nellist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Project 1-479] Nellist was created with Vivado 2018.2
 - [Device 21-403] Loading part xc7a35icpg236-1L
 - [Project 1-570] Preparing nellist for logic optimization
 - [Timing 38-478] Restoring timing data from binary archive
 - [Timing 38-479] Binary timing data restore complete
 - [Project 1-856] Restoring constraints from binary archive
 - [Project 1-853] Binary constraint restore complete
 - [Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed
 - [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
- Opt Design (23 infos, 45 status messages):
 - Command opt_design (44 more like this)
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35i'
 - [Project 1-461] DRC finished with 0 Errors
 - [Project 1-462] Please refer to the DRC report (report_drc) for more information.
 - [Opt 31-49] Retargeted 0 cell(s).
 - [Opt 31-138] Pushed 0 inverter(s) to load pin(s). (1 more like this)
 - [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
 - [Opt 31-662] Phase BUFQ optimization created 0 cells of which 0 are BUFQs and removed 0 cells.
 - [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
 - [Common 17-83] Releasing license: Implementation
 - [Timing 38-480] Writing timing data to binary archive.
 - [Common 17-1381] The checkpoint D:/other/Courses/Kareem_waseem_Digital_Design/Ass/Ass5/Q1/synthesis/project_1/runs/impl_1/control_unit.dcp has been generated.
 - [runlcl-4] Executing : report_drc -file control_unit_drc_opted.rpt -pb control_unit_drc_opted.pb -rpx control_unit_drc_opted.rpx
 - [IP_Flow 19-234] Refreshing IP repositories
 - [IP_Flow 19-1704] No user IP repositories specified
 - [IP_Flow 19-2313] Loaded Vivado IP repository 'D:/Prg/Vivado/Vivado/2018.2/data/ip'
 - [DRC 23-27] Running DRC with 2 threads (1 more like this)
 - [Corertl 2-168] The results of DRC are in file control_unit_drc_opted.rpt.
- Place Design (21 infos, 90 status messages):
 - Command place_design (89 more like this)
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35i'
 - [DRC 23-27] Running DRC with 2 threads (1 more like this)
 - [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
 - [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)

Utilization report

The screenshot shows the Vivado IDE's Utilization report. The report table shows the following resource utilization for the "control_unit" component:

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (815 0)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
control_unit	16	4	5	16	4	24	1

Timing report

The screenshot shows the Vivado IDE's Timing report. The report table shows the following timing constraints for the design:

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 8.713 ns	Worst Hold Slack (WHS): 0.296 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Falling Endpoints: 0	Number of Falling Endpoints: 0	Number of Falling Endpoints: 0
Total Number of Endpoints: 2	Total Number of Endpoints: 2	Total Number of Endpoints: 3

Device



Comment

One hot encoding:

The screenshot shows two windows from the Xilinx Vivado Design Suite. The top window is titled "Design Timing Summary" and displays timing constraints. It shows a summary table with columns for Setup, Hold, and Pulse Width. The setup table includes rows for Worst Negative Slack (WNS), Total Negative Slack (TNS), Number of Failing Endpoints, and Total Number of Endpoints. The hold table includes rows for Worst Hold Slack (WHS), Total Hold Slack (THS), Number of Failing Endpoints, and Total Number of Endpoints. The pulse width table includes rows for Worst Pulse Width Slack (WPWS), Total Pulse Width Negative Slack (TPWS), Number of Failing Endpoints, and Total Number of Endpoints. The bottom window is titled "Utilization" and displays resource usage. It shows a hierarchy table with columns for Name, Slice LUTs (20800), Slice Registers (41600), Bonded IOB (106), and BUFGCTRL (32). The hierarchy tree on the left shows categories like Slice Logic, Slice LUTs, Slice Registers, and Register as Latch.

Gray encoding:

The screenshot shows two windows from the Xilinx Vivado Design Suite. The top window is titled "Design Timing Summary" and displays timing constraints. It shows a summary table with columns for Setup, Hold, and Pulse Width. The setup table includes rows for Worst Negative Slack (WNS), Total Negative Slack (TNS), Number of Failing Endpoints, and Total Number of Endpoints. The hold table includes rows for Worst Hold Slack (WHS), Total Hold Slack (THS), Number of Failing Endpoints, and Total Number of Endpoints. The pulse width table includes rows for Worst Pulse Width Slack (WPWS), Total Pulse Width Negative Slack (TPWS), Number of Failing Endpoints, and Total Number of Endpoints. The bottom window is titled "Utilization" and displays resource usage. It shows a hierarchy table with columns for Name, Slice LUTs (20800), Slice Registers (41600), Bonded IOB (106), and BUFGCTRL (32). The hierarchy tree on the left shows categories like Slice Logic, Slice LUTs, Slice Registers, and Register as Latch.

It appears that best encoding in general for the design is one hot encoding

9. Linting

Lint snippet

```
module control_unit (unlock_doors, accelerate_car, speed_limit, car_speed, leading_distance, clk, rst);
    parameter MIN_DISTANCE = 7'd40;
    parameter STOP = 2'b00;
    parameter ACCELERATE = 2'b01;
    parameter DECELERATE = 2'b10;
    parameter ns = 2'b11;

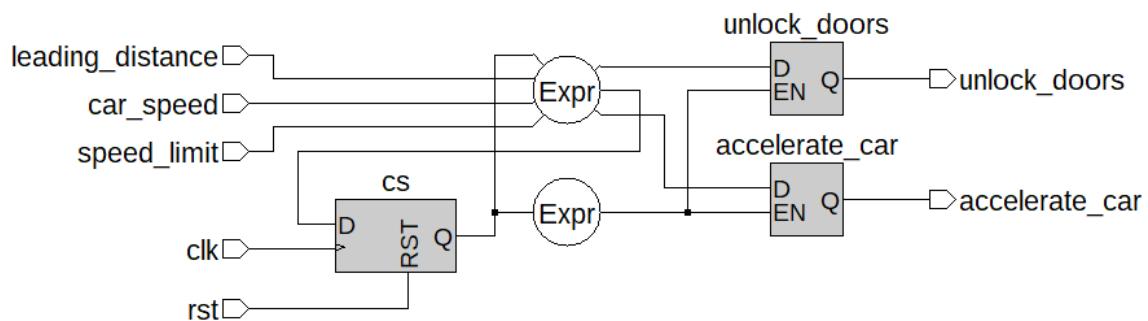
    input [7:0] speed_limit, car_speed ;
    input [6:0] leading_distance ;
    input clk, rst;
    output reg unlock_doors, accelerate_car;
    reg [1:0] cs, ns;

    //state memory
    always @(posedge clk or posedge rst) begin
        if(rst)begin
            cs <= STOP;
            ns <= 0;
        end
        else begin
            cs <= ns;
        end
    end

    //next state logic
    always @(*cs or speed_limit or car_speed or leading_distance) begin
        case (cs)
            STOP:
                ns = 0;
            ...
        endcase
    end
endmodule
```

Severity	Status	Check	Alias	Message	Module	Category	State	Owner	STARC Reference
Info	Waived	async_reset_active...		Asynchronous reset is active high. Reset rst...	control_unit	Clock	resolved unass...	2.3.6.2	
Info	Fixed	multi_ports_in_singl...		Multiple ports are declared in one line. Mod...	control_unit	Rtl Design ...	resolved unass...	3.5.6.3	

Lint Schematic



2) Q2

1.RTL code

1. TOP_Module

```
● ○ ●
1 module counter (y, rst, clk);
2   parameter A = 0;
3   parameter B = 1;
4   parameter C = 2;
5   parameter D = 3;
6
7   input rst, clk;
8   output reg [1:0] y;
9
10  reg [1:0] cs, ns;
11  //state memory
12  always @(posedge clk or posedge rst) begin
13    if(rst)
14      cs<=A;
15    else
16      cs<=ns;
17  end
18  //nextstate
19  always @ (cs) begin
20    case (cs)
21      A: ns=B;
22      B: ns=C;
23      C: ns=D;
24      D: ns=A;
25      default: ns=A;
26    endcase
27  end
28  //output
29  always @ (cs) begin
30    case (cs)
31      A: y=0;
32      B: y=1;
33      C: y=3;
34      D: y=2;
35      default: y=0;
36    endcase
37  end
38 endmodule
```

2) Reference module

```
● ● ●  
1 module gray_counter (gray_out, clk, rst);  
2     input clk, rst;  
3     output [1:0] gray_out;  
4  
5     reg [1:0] counter;  
6  
7     assign gray_out[1] = counter[1];  
8     assign gray_out[0] = ^counter;  
9  
10    always @(posedge clk or posedge rst)begin  
11        if (rst)  
12            counter <= 0;  
13        else  
14            counter <= counter + 1;  
15    end  
16  
17 endmodule
```

2. Testbench code

```
● ● ●
1 module counter_tb ();
2
3     reg rst_tb, clk_tb;
4     wire [1:0] y_tb;
5     wire [1:0] gray_out_tb;
6
7     counter DUT (y_tb, rst_tb, clk_tb);
8     gray_counter golden (gray_out_tb, clk_tb, rst_tb);
9
10    initial begin
11        clk_tb = 0;
12        forever begin
13            #1 clk_tb = ~clk_tb;
14        end
15    end
16
17    initial begin
18        rst_tb = 1;
19        #5;
20        rst_tb=0;
21        repeat(20)begin
22            @(negedge clk_tb);
23        end
24
25        $display("test done");
26        $finish;
27    end
28
29 endmodule
```

3. Do file



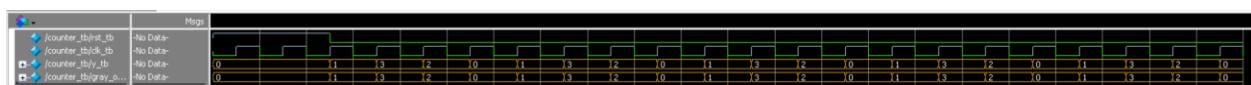
```
1 vlib work
2 vlog q2.v q4.v q2_tb.v
3 vsim -voptargs="+acc" work.counter_tb
4 add wave *
5 run -all
6 #quit -sim
```

4. QuestaSim Snippets

Messages Snippet

```
# Top level modules:
#   counter_tb
# End time: 06:20:43 on Aug 20,2025, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
# vsim -voptargs="+acc" work.counter_tb
# Start time: 06:20:43 on Aug 20,2025
# ** Note: (vsim-3812) Design is being optimized...
# ** Note: (vopt-143) Recognized 1 FSM in module "counter(fast)".
# Loading work.counter_tb(fast)
# Loading work.counter(fast)
# Loading work.gray_counter(fast)
# test done
# ** Note: $finish    : q2_tb.v(26)
#     Time: 44 ns  Iteration: 1  Instance: /counter_tb
```

Waveform Snippet



5. Constraint File

```

6 ## Clock signal
7 set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMS33 } [get_ports clk]
8 create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
9
10
11 ## LEDs
12 set_property -dict { PACKAGE_PIN U16   IOSTANDARD LVCMS33 } [get_ports {y[0]}]
13 set_property -dict { PACKAGE_PIN E19   IOSTANDARD LVCMS33 } [get_ports {y[1]}]
14 #set_property -dict { PACKAGE_PIN U19   IOSTANDARD LVCMS33 } [get_ports {Led[2]}]
15
16 ##Buttons
17 set_property -dict { PACKAGE_PIN U18   IOSTANDARD LVCMS33 } [get_ports rst]

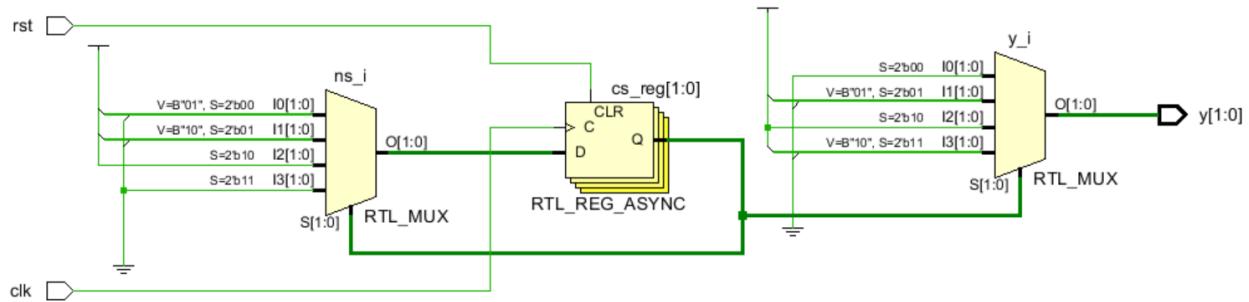
```

6. Elaboration

Message tab

- ✓ Elaborated Design (8 infos, 7 status messages)
 - ✓ General Messages (8 infos, 7 status messages)
 - ⓘ [Synth 8-6157] synthesizing module 'counter' [q2.v:1]
 - > ⓘ [Synth 8-226] default block is never used [q2.v:20] (1 more like this)
 - ⓘ [Synth 8-6155] done synthesizing module 'counter' (#1) [q2.v:1]
 - ⓘ [Device 21-403] Loading part xc7a35tcpg236-1L
 - ⓘ [Project 1-570] Preparing netlist for logic optimization
 - > ⓘ Processing XDC Constraints (6 more like this)
 - ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - ⓘ [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Schematic



7. Synthesis

Message Tab

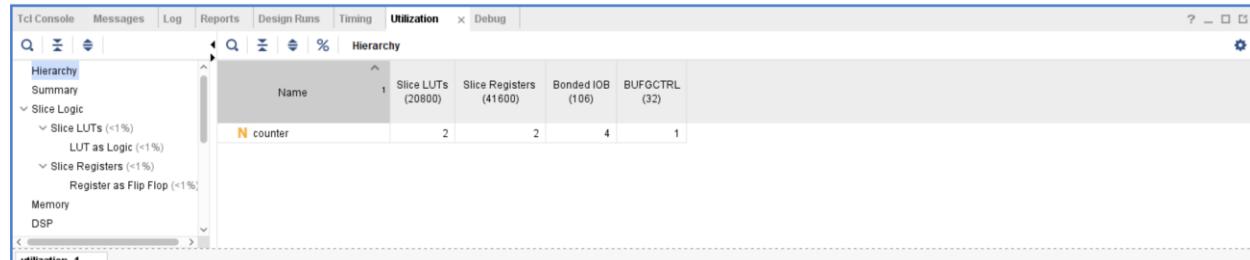
✓ Synthesis (1 warning, 23 infos, 11 status messages)

- > ⓘ Command: synth_design -top counter -part xc7a35tfg236-1L (10 more like this)
- ⓘ [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
- ⓘ [Synth 8-167] synthesizing module 'counter' (@v.1)
- > ⓘ [Synth 8-226] default block is never used (@v.2@) (1 more like this)
- > ⓘ [Synth 8-615] done synthesizing module 'counter' (@1) (@v.1)
- ⓘ [Device 21-403] Loading part xc7a35tfg236-1L
- > ⓘ [Project 1-236] Implementation specific constraints were found while reading constraint file [D:/other/Courses/Kareem_waseem_Digital_Design/Ass/Ass5/Q2/Synthesis/Constraints_basys3 - Copy.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [xilcounter_propimpl.xdc]. To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
- ⓘ [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'counter'
- > ⓘ [Synth 8-554] ROM "y" won't be mapped to Block RAM because address size (2) smaller than threshold (5) (1 more like this)
- ⓘ [Synth 8-335] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'counter'
- ⓘ [Project 1-571] Translating synthesized netlist
- > ⓘ [Netlist 29-17] Analyzing 2 Unisim elements for replacement
- ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- > ⓘ [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- > ⓘ [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
- ⓘ [Common 17-83] Releasing license: Synthesis
- ⓘ [Constraints 18-521] No constraint will be written out
- ⓘ [Common 17-138] The checkpoint D:/other/Courses/Kareem_waseem_Digital_Design/Ass/Ass5/Q2/Synthesis/project1/project1_runs/synth_1/counter.dcp has been generated.
- > ⓘ [runtdc-4] Executing : report_utilization -file counter_utilization_synth.rpt -pb counter_utilization_synth.pb
- ⓘ [Common 17-206] Exiting Vivado at Wed Aug 26 20:25:50 2025..

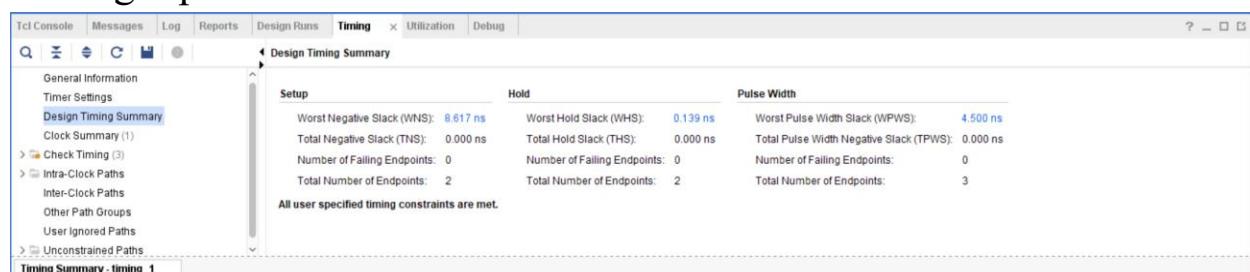
✓ Synthesized Design (5 infos, 2 status messages)

- > ⓘ General Messages (6 infos, 2 status messages)
 - ⓘ [Netlist 29-17] Analyzing 2 Unisim elements for replacement
 - ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - ⓘ [Project 1-479] Netlist was created with Vivado 2018.2
 - ⓘ [Project 1-570] Preparing netlist for logic optimization
 - > ⓘ Parsing XDC File [Constraints_basys3 - Copy.xdc] (1 more like this)
 - ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - ⓘ [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

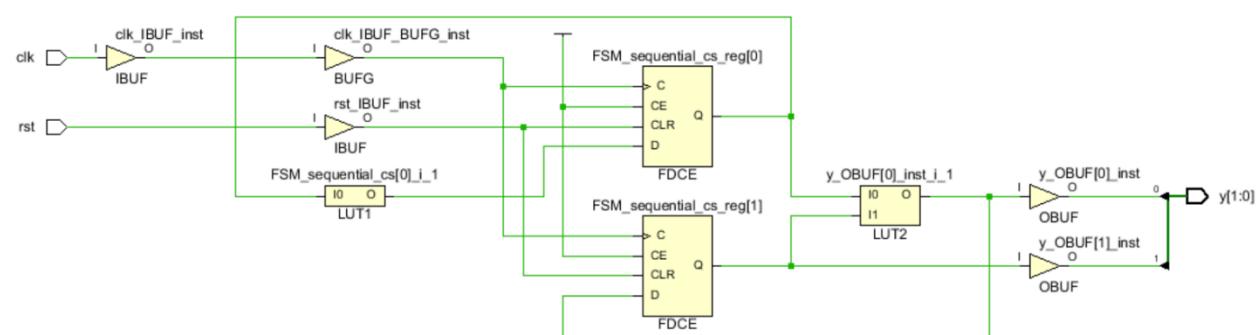
Utilization report



Timing report



Schematic

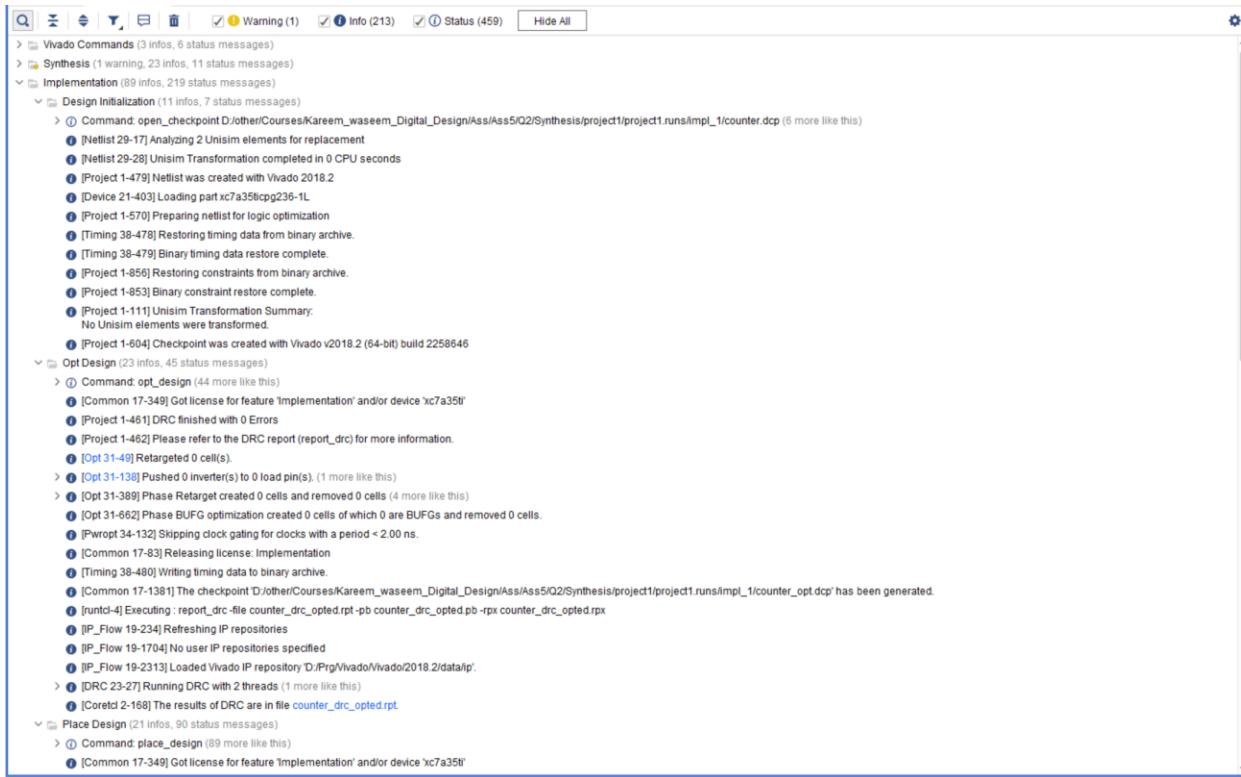


Netlist

```
18 module counter
19   (y,
20    rst,
21    clk);
22   output [1:0]y;
23   input rst;
24   input clk;
25
26   wire <const1>;
27   wire clk;
28   wire clk_IBUF;
29   wire clk_IBUF_BUFG;
30   (* RTL_KEEP = "yes" *) wire [0:0]cs;
31   wire [0:0]ns;
32   wire rst;
33   wire rst_IBUF;
34   wire [1:0]y;
35   (* RTL_KEEP = "yes" *) wire [1:0]y_OBUF;
36
37   LUT1 #(
38     .INIT(2'h1))
39     \FSM_sequential_cs[0].i_1
40     (.I0(cs),
41      |.O(ns));
42   (* FSM_ENCODED_STATES = "A:00,B:01,C:10,D:11" *)
43   (* KEEP = "yes" *)
44   FDCE #(
45     .INIT(1'b0))
46     \FSM_sequential_cs_reg[0]
47     (.C(clk_IBUF_BUFG),
48      .CE(<const1>),
49      .CLR(rst_IBUF),
50      .D(ns),
51      .O(cs));
52   (* FSM_ENCODED_STATES = "A:00,B:01,C:10,D:11" *)
53   (* KEEP = "yes" *)
54   FDCE #(
55     .INIT(1'b0))
56     \FSM_sequential_cs_reg[1]
57     (.C(clk_IBUF_BUFG),
58      .CE(<const1>),
59      .CLK(rst_IBUF),
60      .D(y_OBUF[0]),
61      .O(y_OBUF[1]));
62   VCC VCC
63     (.P(<const1>));
64   BUFG clk_IBUF_BUFG_inst
65     (.I(clk_IBUF),
66      .O(clk_IBUF_BUFG));
67   IBUF clk_IBUF_inst
68     (.I(clk),
69      .O(clk_IBUF));
70   IBUF rst_IBUF_inst
71     (.I(rst),
72      .O(rst_IBUF));
73   OBUF y_OBUF[0]_inst
74     (.I(y_OBUF[0]),
75      .O(y[0]));
76   LUT2 #(
77     .INIT(4'h6))
78     \y_OBUF[0]_inst_i_1
79     (.I0(cs),
80      .I1(y_OBUF[1]),
81      .O(y_OBUF[0]));
82   OBUF y_OBUF[1]_inst
83     (.I(y_OBUF[1]),
84      .O(y[1]));
85
86 endmodule
```

8. Implementation

Message Tab



The screenshot shows the 'Messages' tab in the Vivado IDE. The log is organized into sections: Vivado Commands, Synthesis, and Implementation. The Implementation section is expanded, showing sub-sections for Design Initialization, Opt Design, Place Design, and Timing. The log entries provide detailed information about the design process, including command history, analysis results, and license acquisition.

```
Vivado Commands (3 infos, 6 status messages)
Synthesis (1 warning, 23 infos, 11 status messages)
Implementation (89 infos, 219 status messages)
  Design Initialization (11 infos, 7 status messages)
    Command: open_checkpoint D:/other/Courses/Kareem_waseem_Digital_Design/Ass/Ass5/Q2/Synthesis/project1/project1.runs/impl_1/counter.dcp (6 more like this)
    [Netlist 29-17] Analyzing 2 Unisim elements for replacement
    [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    [Project 1-479] Netlist was created with Vivado 2018.2
    [Device 21-403] Loading part xc7a35icpg236-1L
    [Project 1-570] Preparing netlist for logic optimization
    [Timing 38-478] Restoring timing data from binary archive.
    [Timing 38-479] Binary timing data restore complete.
    [Project 1-856] Restoring constraints from binary archive.
    [Project 1-853] Binary constraint restore complete.
    [Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed.
    [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
  Opt Design (23 infos, 45 status messages)
    Command: opt_design (44 more like this)
    [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35i'
    [Project 1-461] DRC finished with 0 Errors
    [Project 1-462] Please refer to the DRC report (report_drc) for more information.
    [Opt 31-49] Retargeted 0 cells.
    [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s). (1 more like this)
    [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
    [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
    [Pwropt 34-132] Skipping clock gating for clocks with a period ~ 2.00 ns.
    [Common 17-83] Releasing license: Implementation
    [Timing 38-480] Writing timing data to binary archive.
    [Common 17-138] The checkpoint D:/other/Courses/Kareem_waseem_Digital_Design/Ass/Ass5/Q2/Synthesis/project1/project1.runs/impl_1/counter_opt.dcp has been generated.
    [runctd-4] Executing :report_drc_file counter_drc_opted.rpt-pb counter_drc_opted.pb -px counter_drc_opted.rpt
    [IP_Flow 19-234] Refreshing IP repositories
    [IP_Flow 19-1704] No user IP repositories specified
    [IP_Flow 19-2313] Loaded Vivado IP repository D:/Prj/Vivado/Vivado/2018.2/data/ip'.
    [DRC 23-27] Running DRC with 2 threads (1 more like this)
    [Corecl 2-168] The results of DRC are in file counter_drc_opted.rpt.
  Place Design (21 infos, 90 status messages)
    Command: place_design (89 more like this)
    [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35i'

  Place Design (21 infos, 90 status messages)
    Command: place_design (89 more like this)
    [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35i'
```

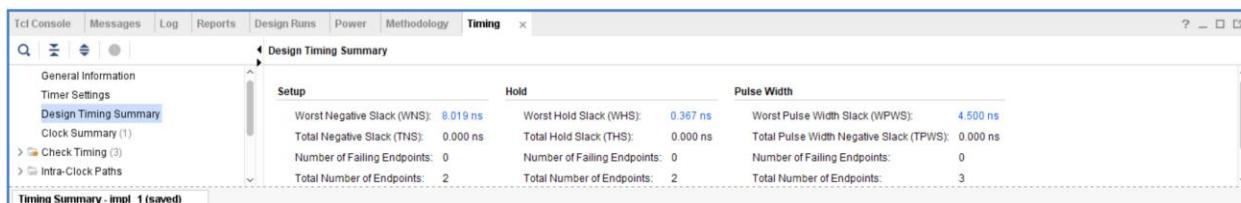
Utilization report



The screenshot shows the Utilization tab in the Vivado IDE. On the left, a hierarchy tree shows the design structure, with 'Slice Logic' expanded to show 'Slice LUTs' and 'Slice Registers'. The main area displays a utilization table for the 'counter' component. The table includes columns for Name, Slice LUTs (20800), Slice Registers (41600), Slice (8150), LUT as Logic (20800), LUT Flip Flop Pairs (20800), Bonded IOB (106), and BUFGCTRL (32).

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
counter	2	2	1	2	1	4	1

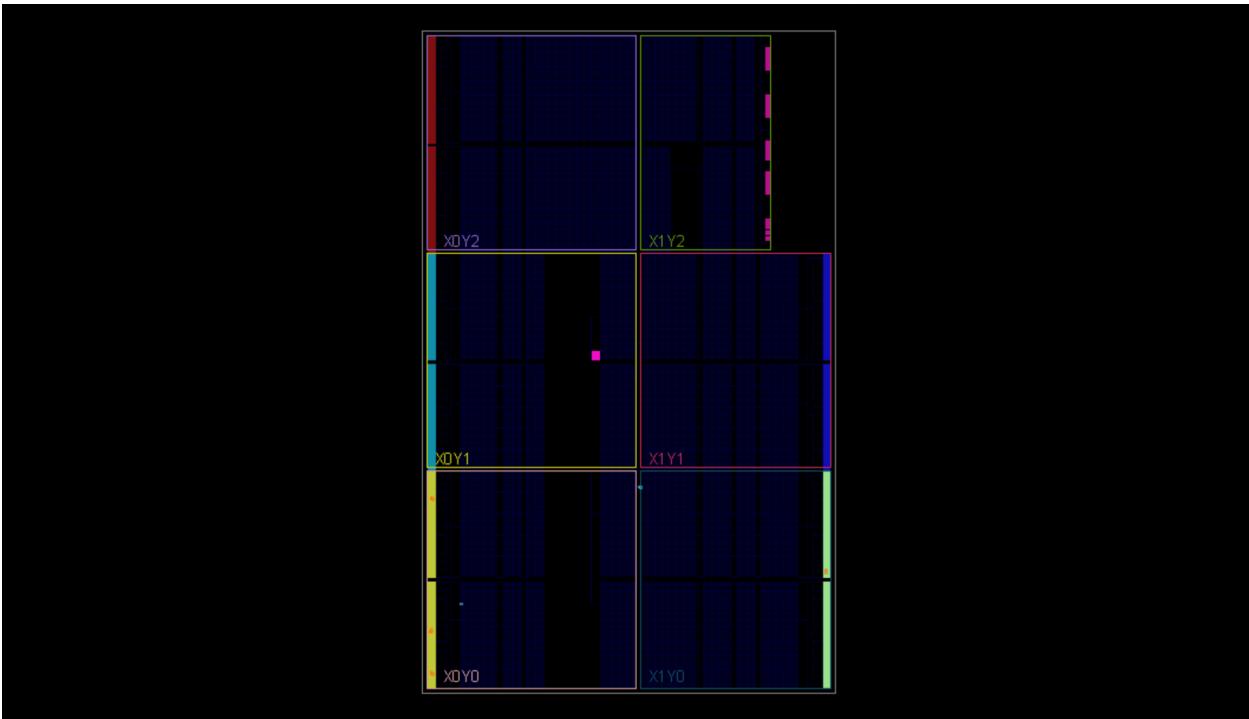
Timing report



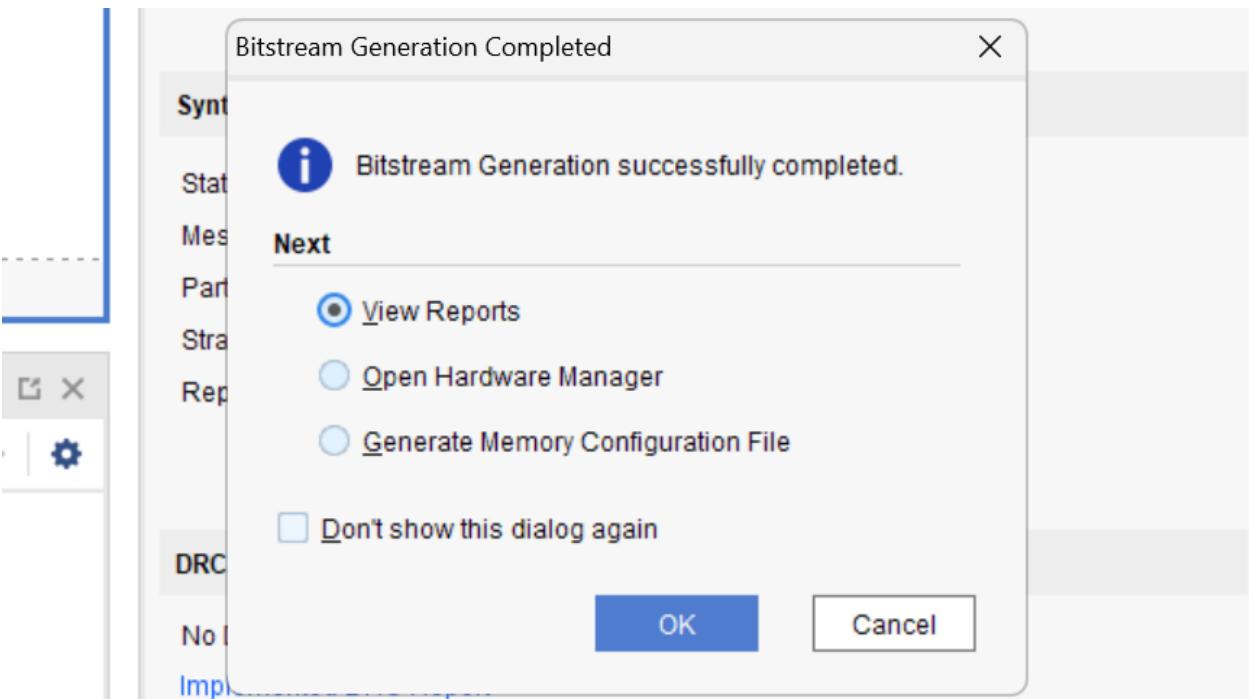
The screenshot shows the Timing tab in the Vivado IDE. The 'Design Timing Summary' section is selected. The table provides detailed timing information, including General Information, Timer Settings, and specific timing metrics like Worst Negative Slack (WNS), Total Negative Slack (TNS), and Pulse Width.

Design Timing Summary			
General Information		Setup	
Timer Settings		Worst Negative Slack (WNS):	8.019 ns
Design Timing Summary		Worst Hold Slack (WHS):	0.367 ns
Clock Summary (1)		Total Hold Slack (THS):	0.000 ns
> Check Timing (3)		Total Pulse Width Negative Slack (TPWNS):	0.000 ns
> Intra-Clock Paths		Number of Failing Endpoints:	0
Timing Summary - impl_1 (saved)		Number of Failing Endpoints:	0
		Total Number of Endpoints:	2
		Pulse Width	4.500 ns
		Total Number of Endpoints:	3

Device



9. Bitstream



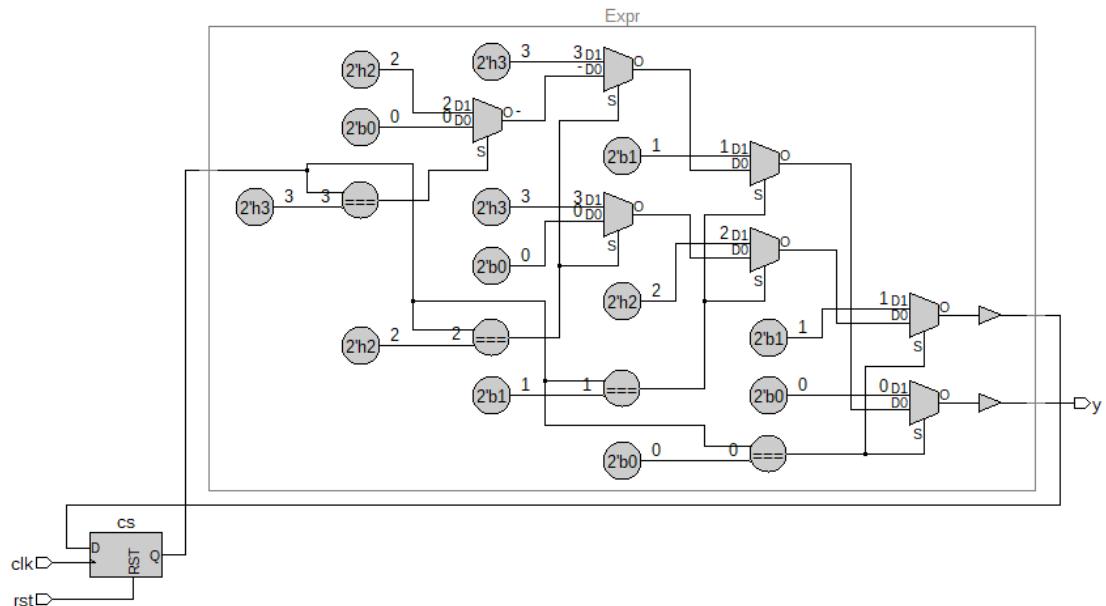
10. Linting

Lint snippet

The screenshot shows the Questa Lint interface. The top window displays a Verilog module named `counter` with parameters A=0, B=1, C=2, D=3. It includes an input `rst`, output `y`, and logic for state transitions between four states (A, B, C, D). The bottom window shows the Lint Checks table with two findings:

Severity	Status	Check	Alias	Message	Module	Category	State	Owner	STARC Reference
Info	Waived	async_reset_active...		Asynchronous reset is active high. Reset rst... counter	Clock	resolved unass...	2.3.6.2		
Info	Fixed	multi_ports_in_singl...		Multiple ports are declared in one line. Mod... counter	Rtl Design ...	resolved unass...	3.5.6.3		

Lint Schematic



3) Q3

1.RTL code

1. TOP_Module

```
● ● ●
1 module monitor (ERR, Din, clk, rst);
2   parameter START      = 0;
3   parameter D0_is_1    = 1;
4   parameter D0_not_1   = 2;
5   parameter D1_is_1    = 3;
6   parameter D1_not_1   = 4;
7
8   input Din, clk, rst;
9   output ERR;
10  reg [2:0] cs, ns;
11
12 //state memory
13 always @(posedge clk or posedge rst) begin
14   if(rst)
15     cs<=START;
16   else
17     cs<=ns;
18 end
19
20 //nextstate
21 always @(cs, Din) begin
22   case(cs)
23     START: begin
24       if (Din == 0)
25         ns=D0_not_1;
26       else
27         ns=D0_is_1;
28     end
29     D0_is_1:begin
30       if (Din == 0)
31         ns=D1_not_1;
32       else
33         ns=D1_is_1;
34     end
35     D0_not_1: ns=D1_not_1;
36     D1_is_1: ns=START;
37     D1_not_1: ns=START;
38     default: ns=START;
39   endcase
40 end
41
42 //output
43 assign ERR = (cs == D1_is_1)? ((Din == 1)? 1 : 0) : 0;
44
45 endmodule
```

2. Testbench code

```
● ● ●  
1 module monitor_tb ();  
2  
3     reg Din, clk, rst;  
4     wire ERR;  
5  
6     monitor DUT (ERR, Din, clk, rst);  
7  
8     initial begin  
9         clk = 0;  
10        forever begin  
11            #1 clk =~clk;  
12        end  
13    end  
14  
15    initial begin  
16        rst = 1;  
17        Din = 0;  
18        #5;  
19        rst = 0;  
20  
21        repeat(1000)begin  
22            Din = $random;  
23            @(negedge clk);  
24        end  
25  
26        $display("test done");  
27        $finish;  
28    end  
29 endmodule
```

3. Do file



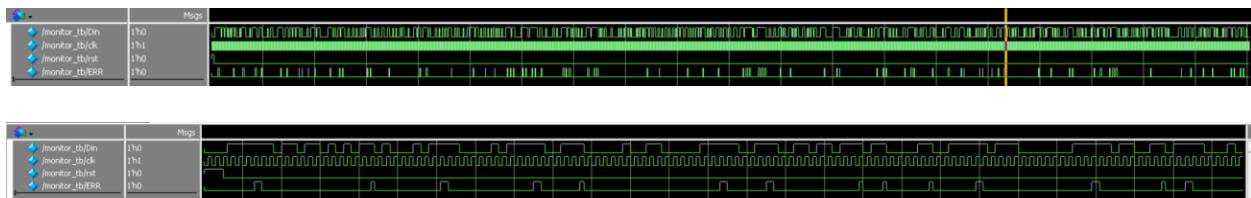
```
1 vlib work
2 vlog q3.v q3_tb.v
3 vsim -voptargs="+acc" work.monitor_tb
4 add wave *
5 run -all
6 #quit -sim
```

4. QuestaSim Snippets

Messages Snippet

```
# Top level modules:
#     monitor_tb
# End time: 07:03:22 on Aug 20,2025, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
# vsim -voptargs="+acc" work.monitor_tb
# Start time: 07:03:22 on Aug 20,2025
# ** Note: (vsim-3812) Design is being optimized...
# ** Note: (vopt-143) Recognized 1 FSM in module "monitor(fast)".
# Loading work.monitor_tb(fast)
# Loading work.monitor(fast)
# test done
# ** Note: $finish : q3_tb.v(27)
#     Time: 2004 ns  Iteration: 1  Instance: /monitor_tb
```

Waveform Snippet



5. Constraint File

```
## Clock signal
set_property -dict { PACKAGE_PIN W5    IO_STANDARD LVCMOS33 } [get_ports clk]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]

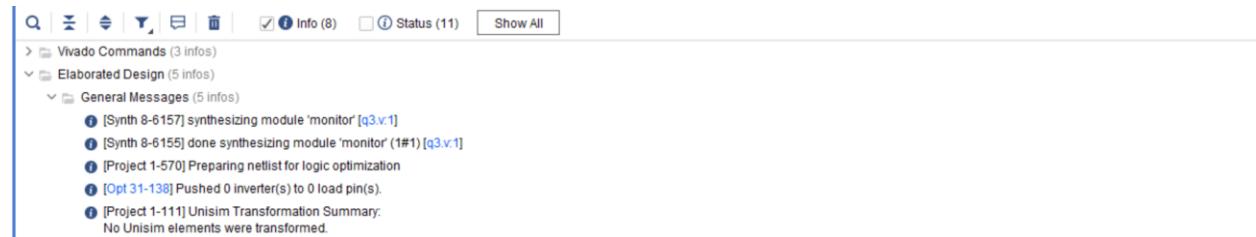
## Switches
set_property -dict { PACKAGE_PIN V17    IO_STANDARD LVCMOS33 } [get_ports {Din}]

## LEDs
set_property -dict { PACKAGE_PIN U16    IO_STANDARD LVCMOS33 } [get_ports {ERR}]

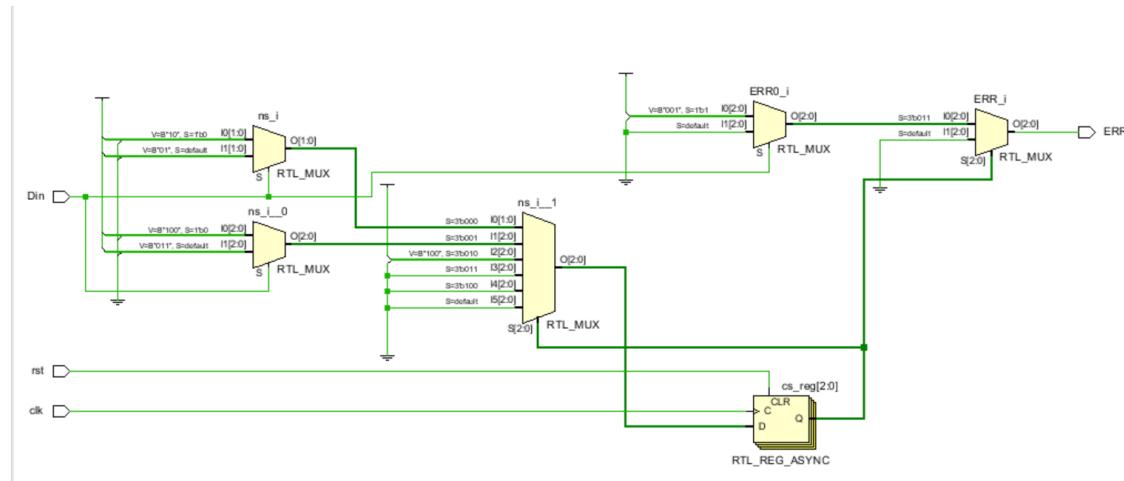
|
##Buttons
set_property -dict { PACKAGE_PIN U18    IO_STANDARD LVCMOS33 } [get_ports rst]
#set_property -dict { PACKAGE_PIN T18    IO_STANDARD LVCMOS33 } [get_ports btnU]
#set_property -dict { PACKAGE_PIN W19    IO_STANDARD LVCMOS33 } [get_ports btnL]
#set_property -dict { PACKAGE_PIN T17    IO_STANDARD LVCMOS33 } [get_ports btnR]
#set_property -dict { PACKAGE_PIN U17    IO_STANDARD LVCMOS33 } [get_ports btnD]
```

6. Elaboration

Message tab



Schematic

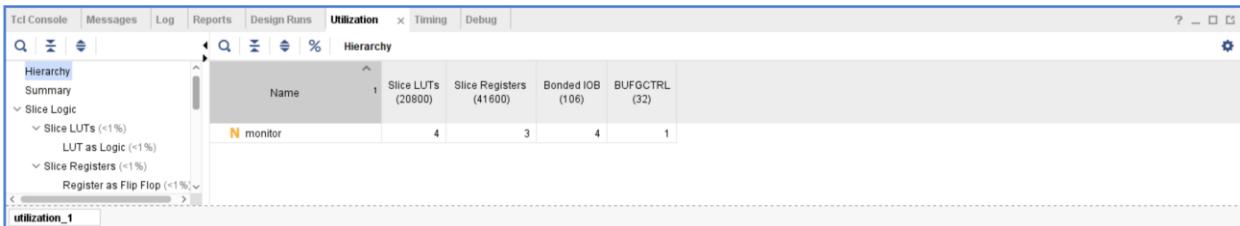


7. Synthesis

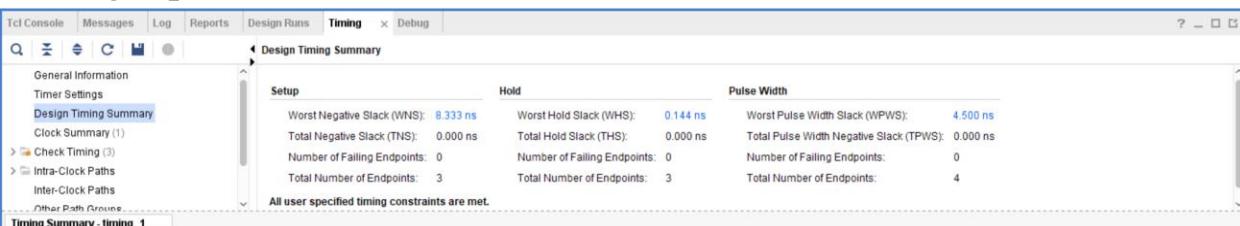
Message Tab



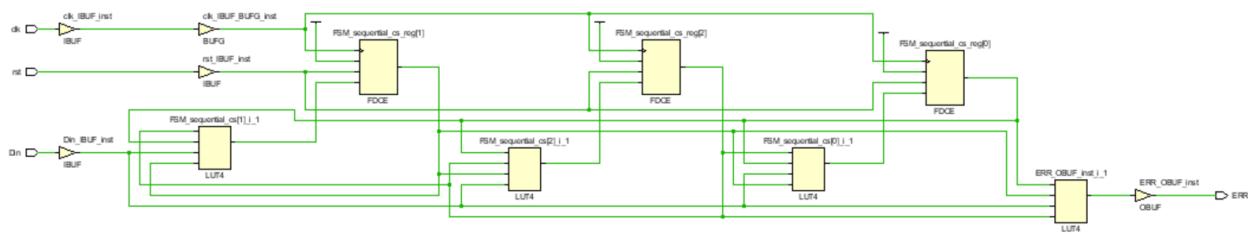
Utilization report



Timing report



Schematic



1. Netlist

```
18 module monitor
19   input Din;
20   input clk;
21   input rst;
22   output ERR;
23   input Din;
24   input clk;
25   input rst;
26
27   wire \<const1>;
28   wire Din;
29   wire Din_IBUF;
30   wire ERR;
31   wire ERR_OBUF;
32   wire clk;
33   wire clk_IBUF;
34   wire clk_IBUF_BUFG;
35   (* RTL_KEEP = "yes" *) wire [2:0]cs;
36   wire [2:0]ns;
37   wire rst;
38   wire rst_IBUF;
39
40   IBUF Din_IBUF_inst
41     (.I(Din),
42      .O(Din_IBUF));
44   OBUF ERR_OBUF_inst
45     (.I(ERR_OBUF),
46      .O(ERR));
47   LUT4 #(
48     .INIT(16'h1000))
49   ERR_OBUF_inst_i_1
50     (.I0(cs[0]),
51      .I1(cs[1]),
52      .I2(Din_IBUF),
53      .I3(cs[2]),
54      .O(ERR_OBUF));
55   LUT4 #(
56     .INIT(16'h0049))
57   \FSM_sequential_cs[0].i_1
58     (.I0(cs[2]),
59      .I1(cs[0]),
60      .I2(Din_IBUF),
61      .I3(cs[1]),
62      .O(ns[0]));
63   LUT4 #(
64     .INIT(16'h0154))
65   \FSM_sequential_cs[1].i_1
66     (.I0(cs[2]),
67      .I1(cs[0]),
68      .I2(Din_IBUF),
69      .I3(cs[1]),
70      .O(ns[1]));
71   LUT4 #(
72     .INIT(16'h1000))
73   \FSM_sequential_cs[2].i_1
74     (.I0(cs[0]),
75      .I1(cs[2]),
76      .I2(cs[1]),
77      .I3(Din_IBUF),
78      .O(ns[2]));
79   (* FSM_ENCODED_STATES = "START:000,D0_is_1:010,D0_not_1:001,D1_is_1:100,D1_not_1:011" *)
80   (* KEEP = "yes" *)
81   FDCE #(
82     .INIT(1'b0))
83   \FSM_sequential_cs_reg[0]
84     (.C(clk_IBUF_BUFG),
85      .CE(\<const1>),
86      .CLR(rst_IBUF),
87      .D(ns[0]),
88      .Q(cs[0]));
89   (* FSM_ENCODED_STATES = "START:000,D0_is_1:010,D0_not_1:001,D1_is_1:100,D1_not_1:011" *)
90
91   (* KEEP = "yes" *)
92   FDCE #(
93     .INIT(1'b0))
94   \FSM_sequential_cs_reg[1]
95     (.C(clk_IBUF_BUFG),
96      .CE(\<const1>),
97      .CLR(rst_IBUF),
98      .D(ns[1]),
99      .Q(cs[1]));
100  (* FSM_ENCODED_STATES = "START:000,D0_is_1:010,D0_not_1:001,D1_is_1:100,D1_not_1:011" *)
101  (* KEEP = "yes" *)
102  FDCE #(
103    .INIT(1'b0))
104  \FSM_sequential_cs_reg[2]
105    (.C(clk_IBUF_BUFG),
106      .CE(\<const1>),
107      .CLR(rst_IBUF),
108      .D(ns[2]),
109      .Q(cs[2]));
110  VCC VCC
111    (.P(\<const1>));
112  BUFG clk_IBUF_BUFG_inst
113    (.I(clk_IBUF),
114      .O(clk_IBUF_BUFG));
115  IBUF clk_IBUF_inst
116    (.I(clk),
117      .O(clk_IBUF));
118  IBUF rst_IBUF_inst
119    (.I(rst),
120      .O(rst_IBUF));
121
122 endmodule
```

8. Implementation

Message Tab

Vivado Commands (3 infos)
Synthesis (1 warning, 21 infos)
Implementation (89 infos)
Design Initialization (11 infos)
Opt Design (23 infos)
Place Design (21 infos)
IP Flow (19-234)

[Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35l'
[Project 1-461] DRC finished with 0 Errors
[Project 1-462] Please refer to the DRC report (report_drc) for more information.
[Opt 31-49] Retargeted 0 cell(s).
[Opt 31-138] Pushed 0 inverter(s) to load pin(s). (1 more like this)
[Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
[Opt 31-662] Phase BUFQ optimization created 0 cells of which 0 are BUFQs and removed 0 cells.
[Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
[Common 17-83] Releasing license: Implementation
[Timing 38-480] Writing timing data to binary archive.
[Common 17-1381] The checkpoint D:/other/Courses/Kareem_waseem_Digital_Design/Ass/Ass5/Q3/Synthesis/project_1/project_1_runs/impl_1/monitor_opt.dcp has been generated.
[runtd-4] Executing : report_drc -file monitor_drc_opted.rpt -pb monitor_drc_opted.pb -rpx monitor_drc_opted.rpx
[IP_Flow 19-234] Refreshing IP repositories
[IP_Flow 19-1704] No user IP repositories specified
[IP_Flow 19-2313] Loaded Vivado IP repository 'D:/Prg/Vivado/Vivado/2018.2/data/ip'.
[DRC 23-27] Running DRC with 2 threads (1 more like this)
[Coretd 2-168] The results of DRC are in file monitor_drc_opted.rpt.
[Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35l'
[DRC 23-27] Running DRC with 2 threads (1 more like this)
[Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
[Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)

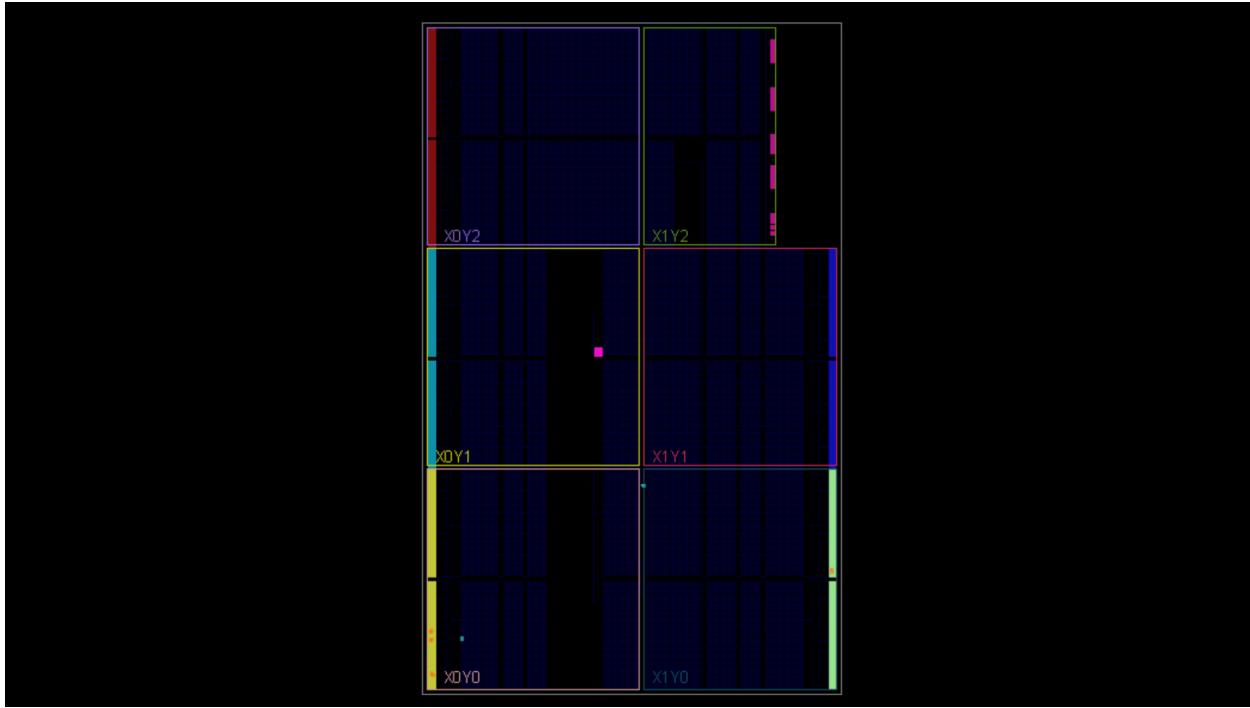
Utilization report

Name	1	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
N monitor	4	3	1	4	3	4	1	

Timing report

Setup			Hold			Pulse Width		
Worst Negative Slack (WNS):	8.513 ns		Worst Hold Slack (WHS):	0.279 ns		Worst Pulse Width Slack (WPWS):	4.500 ns	
Total Negative Slack (TNS):	0.000 ns		Total Hold Slack (THS):	0.000 ns		Total Pulse Width Negative Slack (TPWS):	0.000 ns	
Number of Failing Endpoints:	0		Number of Failing Endpoints:	0		Number of Failing Endpoints:	0	
Total Number of Endpoints:	3		Total Number of Endpoints:	3		Total Number of Endpoints:	4	

Device



Comment

One hot encoding:

Design Timing Summary

Setup			Hold			Pulse Width		
Worst Negative Slack (WNS):	8.357 ns		Worst Hold Slack (WHS):	0.139 ns		Worst Pulse Width Slack (WPWS):	4.500 ns	
Total Negative Slack (TNS):	0.000 ns		Total Hold Slack (THS):	0.000 ns		Total Pulse Width Negative Slack (TPWNS):	0.000 ns	
Number of Failing Endpoints:	0		Number of Failing Endpoints:	0		Number of Failing Endpoints:	0	
Total Number of Endpoints:	5		Total Number of Endpoints:	5		Total Number of Endpoints:	6	

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Bonded IOB (106)	BUFGCTRL (32)
N monitor	6	5	4	1

Gray encoding:

Same as the binary

It appears that best encoding in highest frequency for the design will be one hot encoding, but for minimum area could be gray or binary encoding.

10. Bitstream

9. Linting

Lint snippet

Questa Lint 2021.1 (L_Digital_Design/Ass5/Q3/Lint/Lint.db)

File Edit View Lint Checks Window Help

Design D:\other\Courses\Kareem_waseem_Digital_Design\Ass\Ass5\Q3\Lint\q3.v [monitor]

Search: Type S... 1 module monitor (ERR, Din, clk, rst);
2 parameter START = 0;
3 parameter D0_is_1 = 1;
4 parameter D0_not_1 = 2;
5 parameter D1_is_1 = 3;
6 parameter D1_not_1 = 4;
7
8 input Din, clk, rst;
9 output ERR;
10 reg [2:0] cs, ns;
11
12 //state memory
13 always @(posedge clk or posedge rst) begin
14 if(rst)
15 cs<=START;
16 else
17 cs<=ns;
18 end
19
20 //nextstate
21 always @(cs, Din) begin
22 case(cs)
23 START: begin
24 if (Din == 0)
25 ns=D0_not_1;
26 else
27 ns=D0_is_1;
28 end
29 D0_is_1:begin
30 if (Din == 0)
31 ns=D1_not_1;
32 end
33 end
34
35
36 Flow Na... D... 34

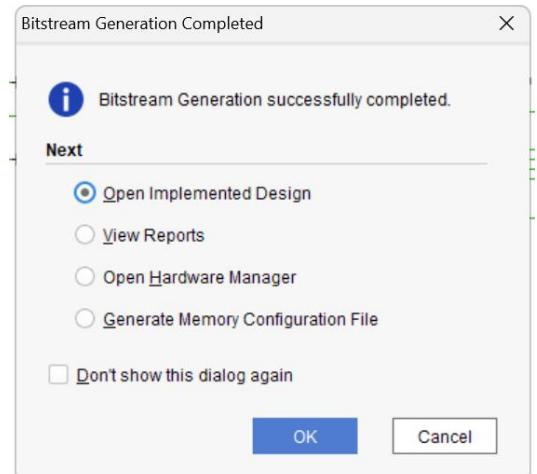
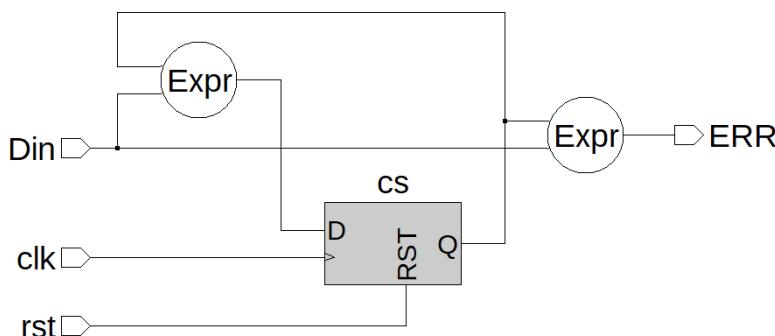
Flow Navigator Design Lint Checks

Filter: Type here (Waived Fixed Pending Unexpected Bug Verified Total : 0 Selected : 0)

Severity	Status	Check	Alias	Message	Module	Category	State	Owner	STARC Reference
Info	Info	async_reset_active...		Asynchronous reset is active high. Reset rst... monitor	Clock	resolved unass...	2.3.6.2		
Info	Info	multi_ports_in_singl...		Multiple ports are declared in one line. Mod... monitor	Rtl Design	... resolved unass...	3.5.6.3		

Transcript Message Viewer Lint Checks Design Metrics Design Information Status History Lint Dashboard ...3.v [monitor]

Lint Schematic



4) Q4

1.RTL code

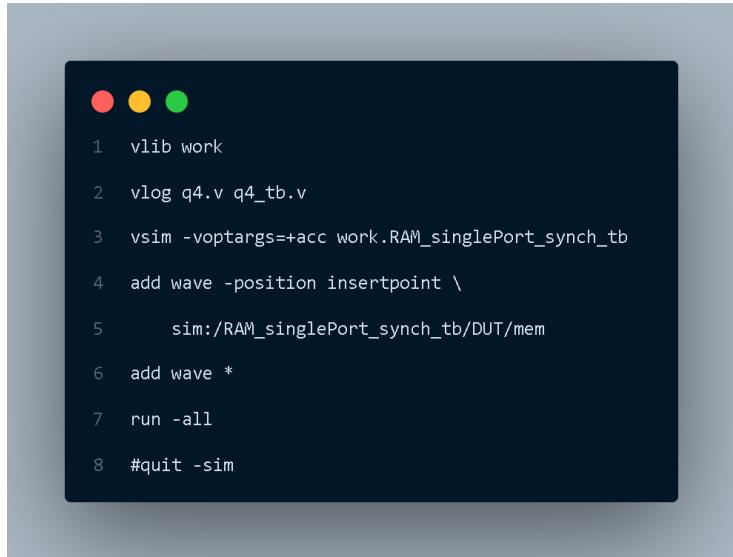
1. TOP_Module

```
● ● ●
1 module RAM_singlePort_synch (dout, parity_out, din, addr, clk, rst, wr_en, rd_en, blk_select, addr_en, dout_en);
2   parameter MEM_WIDTH = 16;
3   parameter MEM_DEPTH = 1024;
4   parameter ADDR_SIZE = 10;
5   parameter ADDR_PIPELINE = "FALSE";
6   parameter DOUT_PIPELINE = "TRUE";
7   parameter PARITY_ENABLE = 1;
8
9   input clk, rst, wr_en, rd_en, blk_select, addr_en, dout_en;
10
11  input [MEM_WIDTH-1:0] din;
12
13  input [ADDR_SIZE-1:0] addr;
14  reg [ADDR_SIZE-1:0] addr_pipe;
15  wire [ADDR_SIZE-1:0] addr_mux;
16
17  output [MEM_WIDTH-1:0] dout;
18  reg [MEM_WIDTH-1:0] dout_RAM;
19  reg [MEM_WIDTH-1:0] dout_pipe;
20
21  output parity_out;
22
23  reg [MEM_WIDTH-1:0] mem [MEM_DEPTH-1:0];
24
25  assign parity_out = (PARITY_ENABLE == 1)? (^dout) : 0;
26  assign addr_mux = (ADDR_PIPELINE == "TRUE")? addr_pipe : addr;
27  assign dout = (DOUT_PIPELINE == "TRUE")? dout_pipe : dout_RAM;
28
29  always @ (posedge clk) begin
30    if(rst)begin
31      addr_pipe <= 0;
32      dout_pipe <= 0;
33      dout_RAM <= 0;
34    end
35    else begin
36      if (addr_en) begin
37        addr_pipe <= addr;
38      end
39      if (dout_en) begin
40        dout_pipe <= dout_RAM;
41      end
42      if(blk_select)begin
43        if (wr_en) begin
44          mem[addr_mux] <= din;
45        end
46        if (rd_en) begin
47          dout_RAM <= mem[addr_mux];
48        end
49      end
50    end
51  end
52
53 endmodule
```

2. Testbench code

```
 1 module RAM_singlePort_synch_tb ();
 2     parameter MEM_WIDTH = 16;
 3     parameter MEM_DEPTH = 1024;
 4     parameter ADDR_SIZE = 10;
 5     parameter ADDR_PIPELINE = "FALSE";
 6     parameter DOUT_PIPELINE = "TRUE";
 7     parameter PARITY_ENABLE = 1;
 8
 9     reg clk, rst, wr_en, rd_en, blk_select, addr_en, dout_en;
10     reg [MEM_WIDTH-1:0] din;
11     reg [ADDR_SIZE-1:0] addr;
12
13     wire [MEM_WIDTH-1:0] dout;
14     wire parity_out;
15
16     RAM_singlePort_synch DUT (dout, parity_out, din, addr, clk, rst, wr_en, rd_en, blk_select, addr_en, dout_en);
17
18     initial begin
19         clk = 0;
20         forever begin
21             #1 clk = ~clk;
22         end
23     end
24
25     initial begin
26         $readmemh("mem.dat", DUT.mem);
27         rst = 1;
28         addr=0; addr_en=0; din=0; rd_en=0; blk_select=0; dout_en=0;
29         #5;
30         rst = 0;
31
32         wr_en = 1;
33         rd_en = 0;
34         repeat(5000)begin
35             blk_select = $random;
36             addr_en = $random;
37             dout_en = $random;
38
39             din = $random;
40             addr = $random;
41             @(negedge clk);
42         end
43
44         wr_en = 0;
45         rd_en = 1;
46         repeat(5000)begin
47             blk_select = $random;
48             addr_en = $random;
49             dout_en = $random;
50
51             addr = $random;
52             @(negedge clk);
53         end
54
55         $display("test done");
56         $finish;
57     end
58 endmodule
```

3. Do file



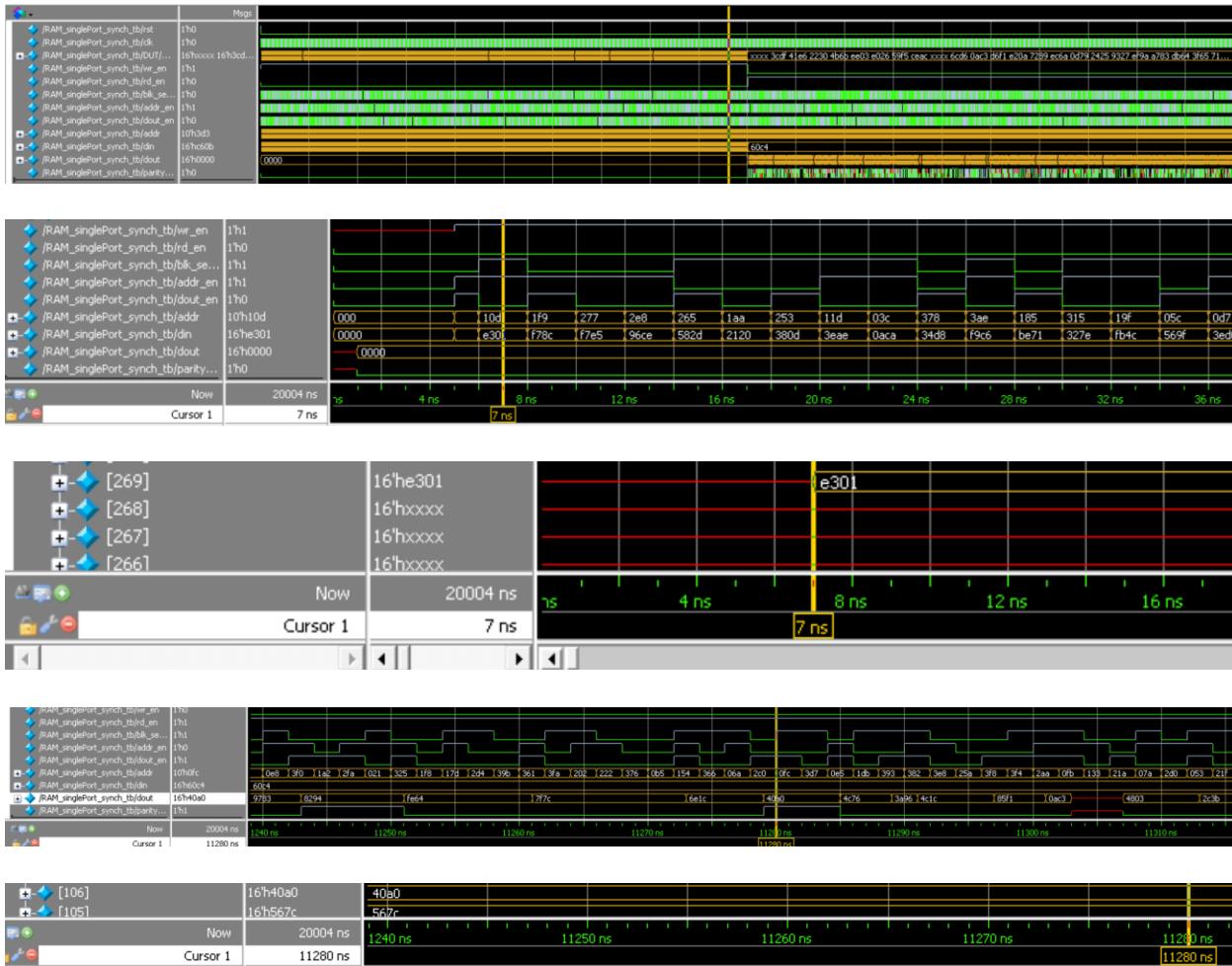
```
1 vlib work
2 vlog q4.v q4_tb.v
3 vsim -voptargs=+acc work.RAM_singlePort_synch_tb
4 add wave -position insertpoint \
5      sim:/RAM_singlePort_synch_tb/DUT/mem
6 add wave *
7 run -all
8 #quit -sim
```

4. QuestaSim Snippets

Messages Snippet

```
# Top level modules:
#          RAM_singlePort_synch_tb
# End time: 08:44:31 on Aug 20,2025, Elapsed time: 0:00:01
# Errors: 0, Warnings: 0
# vsim -voptargs="+acc" work.RAM_singlePort_synch_tb
# Start time: 08:44:31 on Aug 20,2025
# ** Note: (vsim-8009) Loading existing optimized design _opt
# Loading work.RAM_singlePort_synch_tb(fast)
# Loading work.RAM_singlePort_synch(fast)
# ** Warning: (vsim-7) Failed to open readmem file "mem.dat" in read mode.
# No such file or directory. (errno = ENOENT)    : q4_tb.v(26)
#   Time: 0 ns Iteration: 0 Instance: /RAM_singlePort_synch_tb
# test done
# ** Note: $finish    : q4_tb.v(56)
#   Time: 20004 ns Iteration: 1 Instance: /RAM_singlePort_synch_tb
```

Waveform Snippet



5. Constraint File

```
## Clock signal
set_property -dict { PACKAGE_PIN W5    IOSTANDARD LVCMOS33 } [get_ports clk]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
```

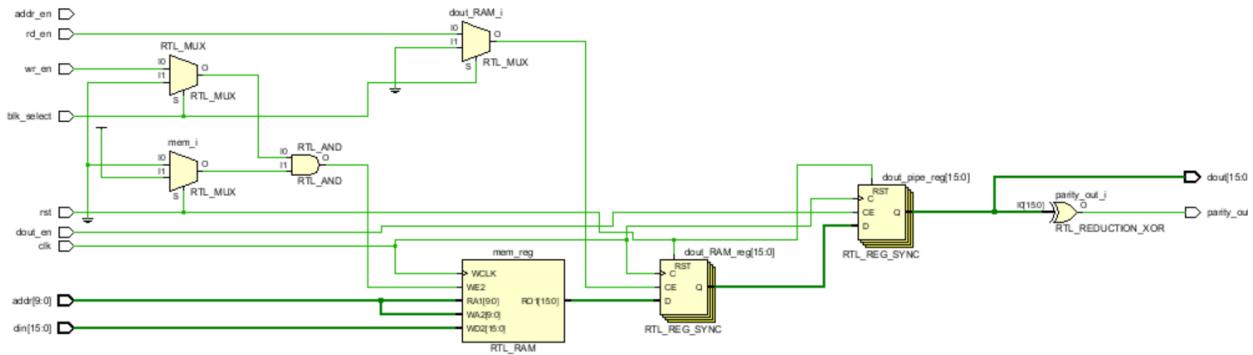
6. Elaboration

Message tab

✓ Elaborated Design (2 warnings, 5 infos)
✓ General Messages (2 warnings, 5 infos)

- ⓘ [Synth 8-6157] synthesizing module 'RAM_singlePort_synch' [q4.v:1]
- ⓘ [Synth 8-6014] Unused sequential element addr_pipe_reg was removed. [q4.v:31]
- ⓘ [Synth 8-6155] done synthesizing module 'RAM_singlePort_synch' (1#1) [q4.v:1]
- ⓘ [Synth 8-3331] design RAM_singlePort_synch has unconnected port addr_en
- ⓘ [Project 1-570] Preparing netlist for logic optimization
- ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- ⓘ [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Schematic



7. Synthesis

Message Tab

✓ **Synthesis** (4 warnings, 17 infos)

- ➊ [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
- ➋ [Synth 8-6157] synthesizing module 'RAM_singlePort_synch' [q4.v1]
- ➌ [Synth 8-6014] Unused sequential element 'addr_pipe_reg' was removed. [q4.v31]
- ➍ [Synth 8-6155] done synthesizing module 'RAM_singlePort_synch' (1#1) [q4.v1]
- ➎ [Device 21-403] Loading part xc7a35tccg236-1L
- ➏ [Project 1-236] Implementation specific constraints were found while reading constraint file [D:/other/Courses/Kareem_waseem_Digital_Design/Ass5/Q4/Synthesis/Constraints_basys3 - Copy.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file 'XilfRAM_singlePort_synch_propimpl.xdc'. Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
- > ➐ [Synth 8-3331] design RAM_singlePort_synch has unconnected port 'addr_en' (1 more like this)
- ➑ [Project 1-571] Translating synthesized netlist
- ➒ [Netlist 29-17] Analyzing 33 Unisim elements for replacement
- ➓ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- > ➔ [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- ➕ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- > ➖ [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
- ➗ [Common 17-83] Releasing license: Synthesis
- ➘ [Constraints 18-5210] No constraint will be written out.
- ➙ [Common 17-1381] The checkpoint D:/other/Courses/Kareem_waseem_Digital_Design/Ass5/Q4/Synthesis/project_1/project_1.rns/synth_1/RAM_singlePort_synch.dcp has been generated.
- ➚ [runtdm-4] Executing : report_utilization -file RAM_singlePort_synch_utilization_synth.rpt -pb RAM_singlePort_synch_utilization_synth.pb
- ➛ [Common 17-206] Exiting Vivado at Wed Aug 20 11:12:56 2025...

✓ **Synthesized Design** (9 infos)

- ➊ [Netlist 29-17] Analyzing 33 Unisim elements for replacement
- ➋ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- ➌ [Project 1-479] Netlist was created with Vivado 2018.2
- ➍ [Project 1-570] Preparing netlist for logic optimization
- ➎ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- ➏ [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
- ➐ [Timing 38-35] Done setting XDC timing constraints.
- ➑ [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.
- ➒ [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

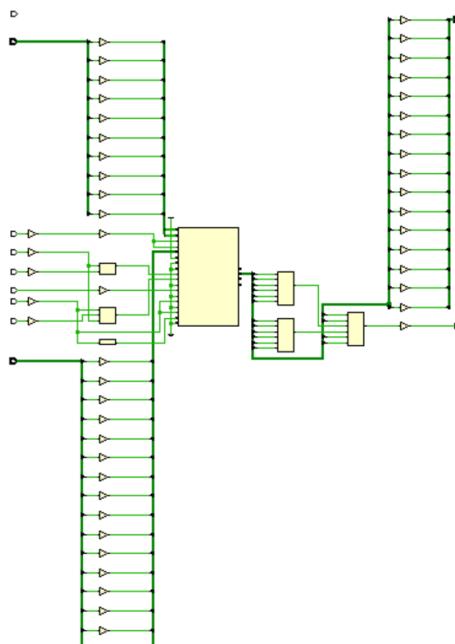
Utilization report

Utilization					
	Name	Slice LUTs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N	RAM_singlePort_synch	6	0.5	49	1

Timing report

Design Timing Summary					
General Information		Setup		Hold	
Timer Settings		Worst Negative Slack (WNS):	inf	Worst Hold Slack (WHS):	inf
Design Timing Summary		Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns
Clock Summary (1)		Number of Falling Endpoints:	0	Number of Falling Endpoints:	0
> Check Timing (48)		Total Number of Endpoints:	60	Total Number of Endpoints:	60
> Intra-Clock Paths		All user specified timing constraints are met.			
Inter-Clock Paths					
Other Path Groups					

Schematic



8. Netlist

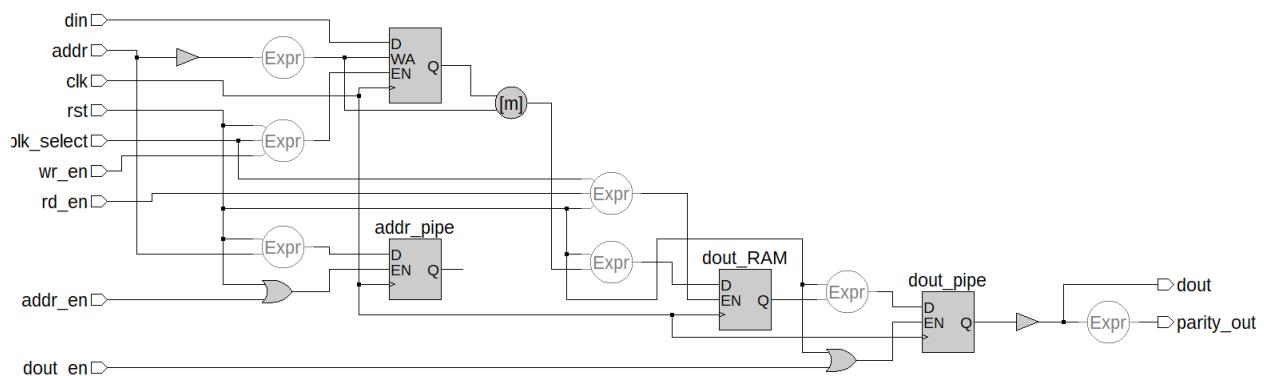
```
18 module RAM_singlePort_synch
19   (dout,
20   parity_out,
21   din,
22   addr,
23   clk,
24   rst,
25   wr_en,
26   rd_en,
27   blk_select,
28   addr_en,
29   dout_en);
30   output [15:0]dout;
31   output parity_out;
32   input [15:0]din;
33   input [9:0]addr;
34   input clk;
35   input rst;
36   input wr_en;
37   input rd_en;
38   input blk_select;
39   input addr_en;
40   input dout_en;
41
42   wire \<const0> ;
43   wire \<const1> ;
44   wire [9:0]addr;
45   wire [9:0]addr_IBUF;
46   wire blk_select;
47   wire blk_select_IBUF;
48   wire clk;
49   wire clk_IBUF;
50   wire clk_IBUF_BUFG;
51   wire [15:0]din;
52   wire [15:0]din_IBUF;
53   wire [15:0]dout;
54   wire [15:0]dout_OBUF;
55   wire dout_en;
```

```
18 module RAM_singlePort_synch
357   parity_out_OBUF_inst_i_1
358     (.I0(dout_OBUF[3]),
359     .I1(dout_OBUF[2]),
360     .I2(parity_out_OBUF_inst_i_2_n_0),
361     .I3(parity_out_OBUF_inst_i_3_n_0),
362     .I4(dout_OBUF[0]),
363     .I5(dout_OBUF[1]),
364     .O(parity_out_OBUF));
365   LUT6 #(
366     .INIT(64'h6996966996696996)
367   parity_out_OBUF_inst_i_2
368     (.I0(dout_OBUF[11]),
369     .I1(dout_OBUF[10]),
370     .I2(dout_OBUF[14]),
371     .I3(dout_OBUF[15]),
372     .I4(dout_OBUF[12]),
373     .I5(dout_OBUF[13]),
374     .O(parity_out_OBUF_inst_i_2_n_0));
375   LUT6 #(
376     .INIT(64'h6996966996696996)
377   parity_out_OBUF_inst_i_3
378     (.I0(dout_OBUF[4]),
379     .I1(dout_OBUF[5]),
380     .I2(dout_OBUF[8]),
381     .I3(dout_OBUF[9]),
382     .I4(dout_OBUF[7]),
383     .I5(dout_OBUF[6]),
384     .O(parity_out_OBUF_inst_i_3_n_0));
385   IBUF rd_en_IBUF_inst
386     (.I(rd_en),
387     .O(rd_en_IBUF));
388   IBUF rst_IBUF_inst
389     (.I(rst),
390     .O(rst_IBUF));
391   IBUF wr_en_IBUF_inst
392     (.I(wr_en),
393     .O(wr_en_IBUF));
394 endmodule
```

9. Linting

Lint snippet

Lint Schematic



5) Q5

1.RTL code

1. TOP_Module

```
● ● ●
1 module FIFO_memory (dout_b, full, empty, din_a, clk_a, clk_b, rst, wen_a, ren_b);
2   parameter FIFO_WIDTH = 16;
3   parameter FIFO_DEPTH = 512;
4
5   input clk_a, clk_b, rst, wen_a, ren_b;
6   input [FIFO_WIDTH-1:0] din_a;
7
8   output reg [FIFO_WIDTH-1:0] dout_b;
9   output full, empty;
10
11  reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0];
12  reg [$cLog2(FIFO_DEPTH):0] Wptr, Rptr;
13
14  assign full = (Wptr[$cLog2(FIFO_DEPTH)] != Rptr[$cLog2(FIFO_DEPTH)] && (Wptr[$cLog2(FIFO_DEPTH)-1:0] == Rptr[$cLog2(FIFO_DEPTH)-1:0]))? 1: 0;
15
16  assign empty = (Wptr == Rptr)? 1 : 0;
17
18  always @(posedge clk_a) begin
19    if (rst) begin
20      Wptr <= 0;
21    end
22    else begin
23      if(wen_a && !full)begin
24        mem[Wptr[$cLog2(FIFO_DEPTH)-1:0]] <= din_a;
25        Wptr <= Wptr + 1;
26      end
27    end
28  end
29
30  always @(posedge clk_b) begin
31    if (rst) begin
32      Rptr <= 0;
33    end
34    else begin
35      if (ren_b && !empty) begin
36        dout_b <= mem[Rptr[$cLog2(FIFO_DEPTH)-1:0]];
37        Rptr <= Rptr + 1;
38      end
39    end
40  end
41
42
43 endmodule
```

2. Testbench code

```
● ● ●
1 module FIFO_memory_tb ();
2   parameter FIFO_WIDTH = 16;
3   parameter FIFO_DEPTH = 512;
4
5   reg clk_a, clk_b, rst, wen_a, ren_b;
6   reg [FIFO_WIDTH-1:0] din_a;
7
8   wire [FIFO_WIDTH-1:0] dout_b;
9   wire full, empty;
10
11  FIFO_memory DUT (dout_b, full, empty, din_a, clk_a, clk_b, rst, wen_a, ren_b);
12
13  initial begin
14    clk_a = 0;
15    clk_b = 0;
16    forever begin
17      #1;
18      clk_a = ~clk_a;
19      clk_b = ~clk_b;
20    end
21  end
22
23  initial begin
24    rst = 1;
25    #5;
26    rst = 0;
27
28    ren_b = 0;
29    wen_a = 1;
30    repeat(100)begin
31      din_a = $random;
32      @(posedge clk_a);
33    end
34
35    wen_a = 0;
36    repeat(100)begin
37      ren_b = $random;
38    end
39
40    ren_b = 1;
41    wen_a = 1;
42    repeat(100)begin
43      din_a = $random;
44      @(posedge clk_a);
45    end
46
47    $display("test done");
48    $finish;
49  end
50
51 endmodule
```

3. Do file

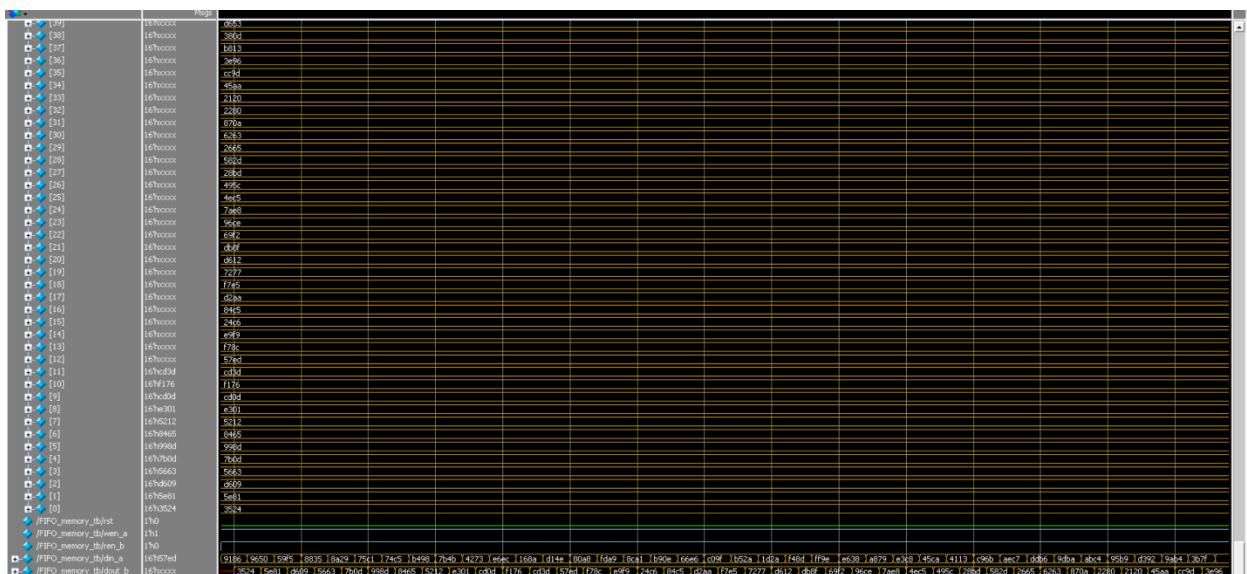
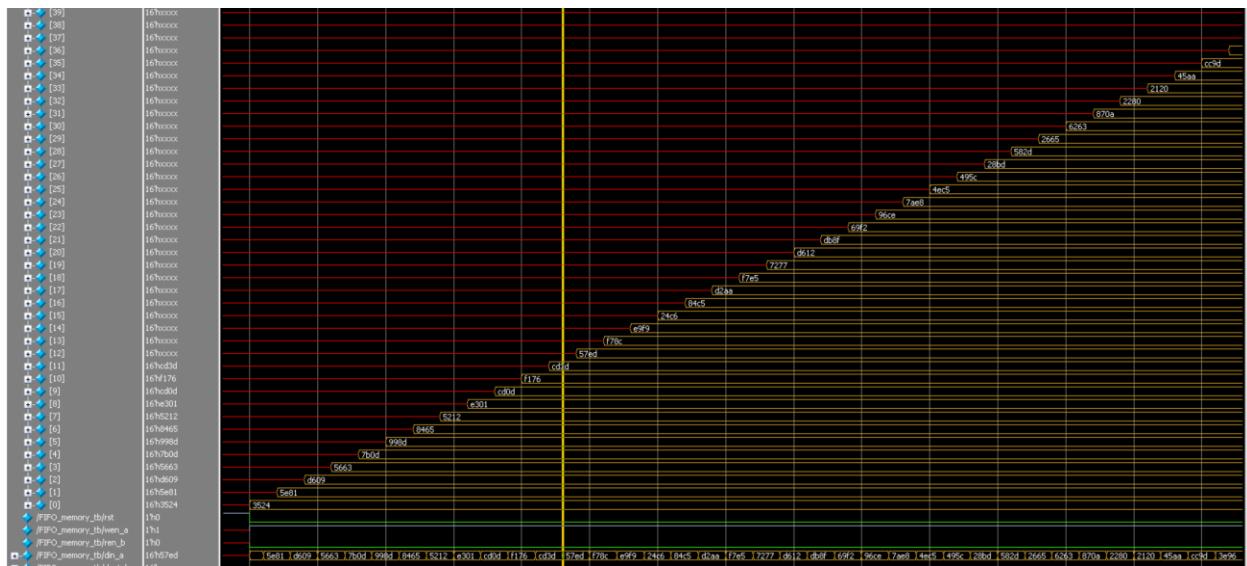
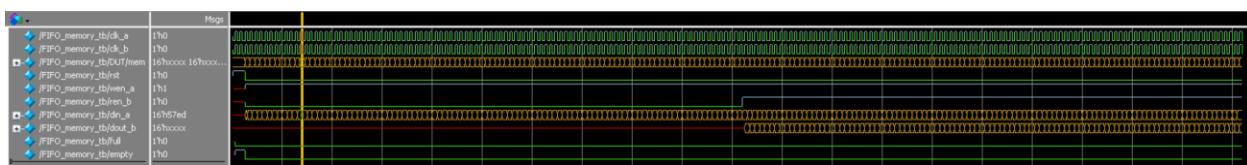
```
● ● ●
1 vlib work
2 vlog q5.v q5_tb.v
3 vsim -voptargs=+acc work.FIFO_memory_tb
4 add wave -position insertpoint \
5     sim:/FIFO_memory_tb/DUT/mem
6 add wave *
7 run -all
8 #quit -sim
```

4. QuestaSim Snippets

Messages Snippet

```
# Top level modules:
#   FIFO_memory_tb
# End time: 09:55:10 on Aug 20, 2025, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
# usim -voptargs+acc" work.FIFO_memory_tb
# Start time: 09:55:10 on Aug 20, 2025
## ** Note: (usim-2013) Design is being optimized due to module recompilation...
# Loading work.FIFO_memory_tb(fast)
# Loading work.FIFO_memory(fast)
# test done
## ** Note: $finish : q5_tb.v(48)
# Time: 404 ns Iteration: 1 Instance: /FIFO_memory_tb
```

Waveform Snippet



5. Constraint File

```
5
6  ## Clock signal
7  set_property -dict { PACKAGE_PIN W5      IO_STANDARD LVCMSOS33 } [get_ports clk_a]
8  create_clock -add -name sys_clk_a_pin -period 10.00 -waveform {0 5} [get_ports clk_a]
9  create_clock -add -name sys_clk_b_pin -period 10.00 -waveform {0 5} [get_ports clk_b]
10
11 .
12  ## Switches
```

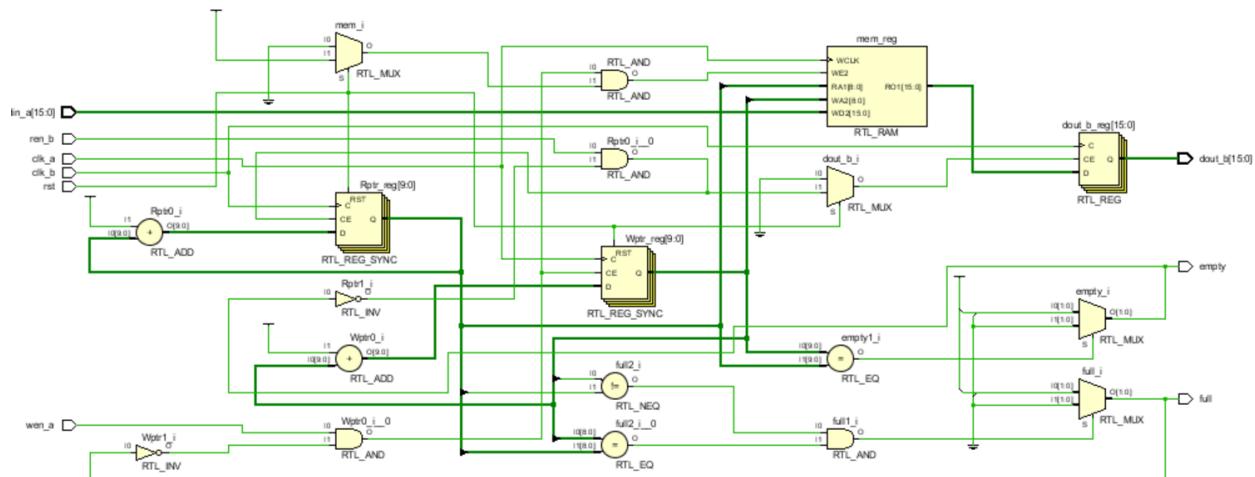
6. Elaboration

Message tab

✓ Elaborated Design (5 infos)

- [Synth 8-6157] synthesizing module 'FIFO_memory' [q5.v:1]
- [Synth 8-6155] done synthesizing module 'FIFO_memory' (1#1) [q5.v:1]
- [Project 1-570] Preparing netlist for logic optimization
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Schematic



7. Synthesis

Message Tab

Tcl Console Messages Log Reports Design Runs Utilization Timing Debug

Warning (2) Info (40) Status (20) Show All

Vivado Commands (3 infos)

Synthesis (2 warnings, 28 infos)

- [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
- [Synth 8-6157] synthesizing module FIFO_memory [q5.v:1]
- [Synth 8-6155] done synthesizing module FIFO_memory [#1] [q5.v:1]
- [Device 21-403] Loading part xc7a35lcp236-1L
- [Project 1-236] Implementation specific constraints were found while reading constraint file [D:/other/Courses/Kareem_waseem_Digital_Design/Ass/Ass5/Q5/Synthesis/Constraints_basys3 - Copy.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [XilFIFO_memory_propimpl.xdc]. Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
- [Synth 8-6014] Unused sequential element Rplc_reg_rep was removed. [q5.v:14]
- [Synth 8-3886] merging instance Rplc_reg_rep[0] (FDRE) to Rplc_reg[0] (8 more like this)
- [Synth 8-4480] The timing for the instance _2mem_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing. (1 more like this)
- [Project 1-571] Translating synthesized netlist
- [Netlist 29-17] Analyzing 24 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed. (1 more like this)
- [Common 17-83] Releasing license: Synthesis
- [Constraints 18-5210] No constraint will be written out.
- [Common 17-1381] The checkpoint D:/other/Courses/Kareem_waseem_Digital_Design/Ass/Ass5/Q5/Synthesis/project_1/runs/synth_1/FIFO_memory.dcp has been generated.
- [runtd-4] Executing : report_utilization -file FIFO_memory_utilization_synth.rpt -pb FIFO_memory_utilization_synth.pb
- [Common 17-206] Exiting Vivado at Wed Aug 20 11:31:08 2025..

Synthesized Design (9 infos)

General Messages (9 infos)

- [Netlist 29-17] Analyzing 24 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-479] Netlist was created with Vivado 2018.2
- [Project 1-570] Preparing netlist for logic optimization
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed.
- [Timing 38-35] Done setting XDC timing constraints.
- [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.
- [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs.

Utilization report

Tcl Console Messages Log Reports Design Runs Utilization Timing Debug

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
FIFO_memory	26	20	0.5	39	2

Summary

Slice Logic

Slice LUTs (<1%)

LUT as Logic (<1%)

Timing report

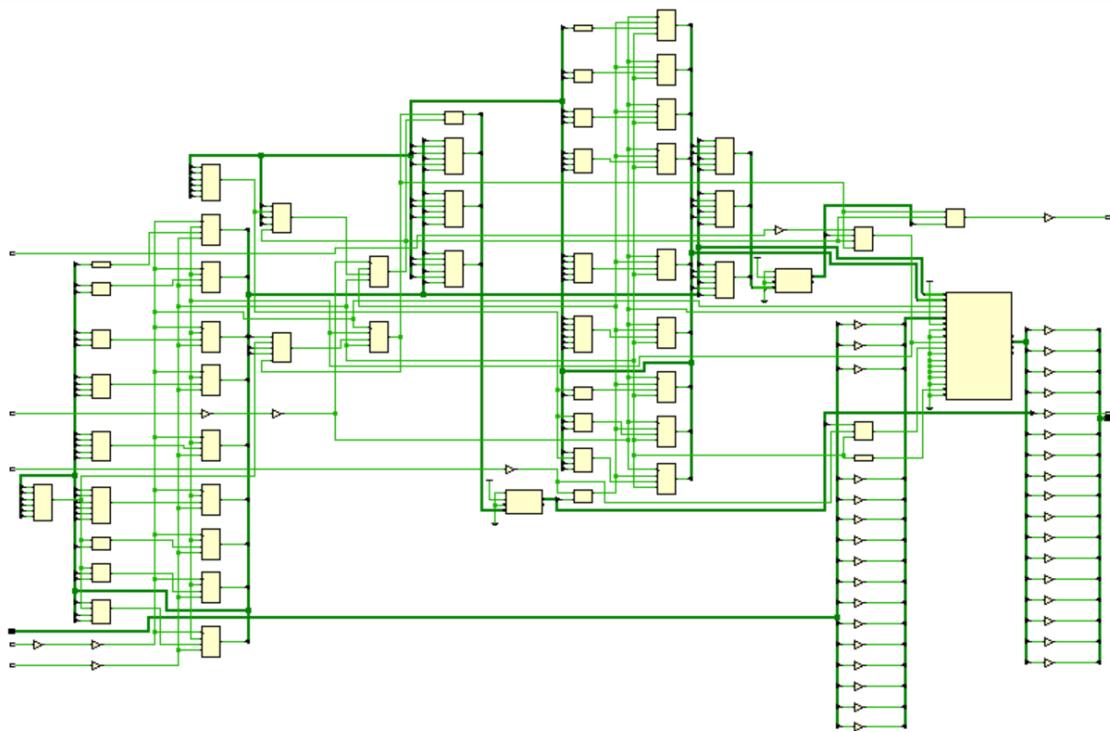
Tcl Console Messages Log Reports Design Runs Utilization Timing Debug

Design Timing Summary

General Information			
Timer Settings	Setup	Hold	Pulse Width
Design Timing Summary	Worst Negative Slack (WNS): 4.502 ns	Worst Hold Slack (WHS): 0.146 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Clock Summary (2)	Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Check Timing (37)	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Intra-Clock Paths	Total Number of Endpoints: 60	Total Number of Endpoints: 60	Total Number of Endpoints: 24
Inter-Clock Paths			
Other Path Groups			

All user specified timing constraints are met.

Schematic



8. Netlist

```
module FIFO_memory
(dout_b,
 full,
 empty,
 din_a,
 clk_a,
 clk_b,
 rst,
 wen_a,
 ren_b);
output [15:0]dout_b;
output full;
output empty;
input [15:0]din_a;
input clk_a;
input clk_b;
input rst;
input wen_a;
input ren_b;

wire \<const0>;
wire \<const1>;
wire Rptr0;
wire Rptr[0].i_1.l_n_0 ;
wire Rptr[1].i_1.l_n_0 ;
wire Rptr[2].i_1.l_n_0 ;
wire Rptr[3].i_1.l_n_0 ;
wire Rptr[4].i_1.l_n_0 ;
wire Rptr[5].i_1.l_n_0 ;
wire Rptr[6].i_1.l_n_0 ;
wire Rptr[7].i_1.l_n_0 ;
wire Rptr[8].i_1.l_n_0 ;
wire Rptr[9].i_1.3_n_0 ;
wire [8:0]Rptr_reg_rep_0;
wire Wptr0;
wire Wptr[9].i_2.n_0 ;
wire Wptr_reg_n_0_0[0] ;
wire Wptr_reg_n_0_1[1] ;
wire Wptr_reg_n_0_2[2] ;
wire Wptr_reg_n_0_3[3] ;
wire Wptr_reg_n_0_4[4] ;
wire Wptr_reg_n_0_5[5] ;
wire Wptr_reg_n_0_6[6] ;
wire Wptr_reg_n_0_7[7] ;
wire Wptr_reg_n_0_8[8] ;
wire CLK_a;
wire CLK_a_IBUF;
wire CLK_a_IBUF_BUFG;
wire CLK_b;
```

9. Linting

Lint snippet

Questa Lint 2021.1 (~_Digital_Design/Ass/Ass5/QS/Lint/lint.db)

```

module FIFO_memory (dout_b, full, empty, din_a, clk_a, clk_b, rst, wen_a, ren_b);
    parameter FIFO_WIDTH = 16;
    parameter FIFO_DEPTH = 512;
    reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0];
    reg [16:0] Wptr, Rptr;
    assign full = (Wptr[$clog2(FIFO_DEPTH)] != Rptr[$clog2(FIFO_DEPTH)]) && (Wptr[$clog2(FIFO_DEPTH)-1:0] == Rptr[$clog2(FIFO_DEPTH)-1:0]);
    assign empty = (Wptr == Rptr) ? 1 : 0;
    always @(posedge clk_a) begin
        if (rst) begin
            Wptr <= 0;
        end
        else begin
            if(wen_a && !full)begin
                mem[Wptr[$clog2(FIFO_DEPTH)-1:0]] <= din_a;
                Wptr <= Wptr + 1;
            end
        end
    end
    always @(posedge clk_b) begin
        if (rst) begin
            Rptr <= 0;
        end
    end
endmodule

```

Lint Summary

Name	Count
Resolved(verified, fixable)	2
Info	2

Lint Checks

Severity	Status	Check	Alias	Message	Module	Category	State	Owner	STARC Reference
Info	Waived	line_char_large		Line has more characters than the specified limit.	none	Rtl Design ...	resolved unass...	3.14.5	
Info	Fixed	multi_ports_in_singl...		Multiple ports are declared in one line. Mod...	FIFO_me...	Rtl Design ...	resolved unass...	3.5.6.3	

Lint Schematic

