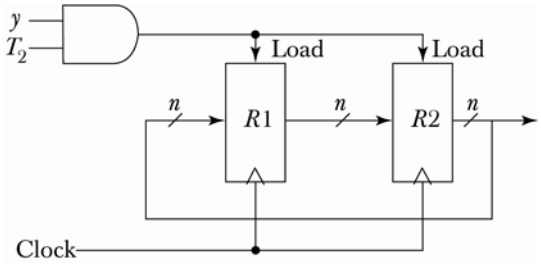
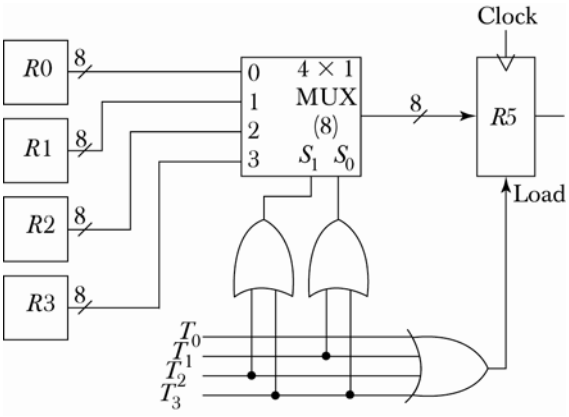
CHAPTER 4

4.1



4.2



$T_0T_1T_2T_3$	S_1 S_0 R_3 load
0 0 0 0	X X 0
1 0 0 0	0 0 1
0 1 0 0	0 1 1
0 0 1 0	1 0 1
0 0 0 1	1 1 1

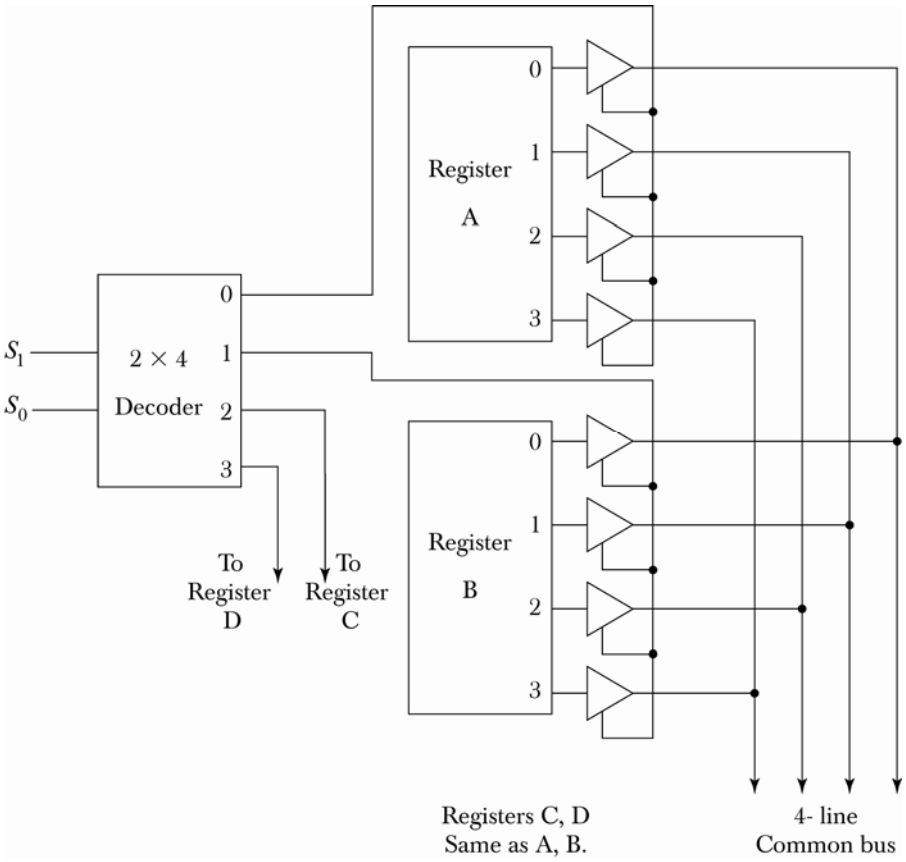
$S_1 = T_2 + T_3$
$S_0 = T_1 + T_3$
load = $T_0 + T_1 + T_2 + T_3$

4.3
P: R1 ← R2
P'Q: R1 ← R3

4.4
Connect the 4-line common bus to the four inputs of each register.
Provide a “load” control input in each register.
Provide a clock input for each register.

To transfer from register C to register A:
Apply $S_1S_0 = 10$ (to select C for the bus.)
Enable the load input of A
Apply a clock pulse.

4.5



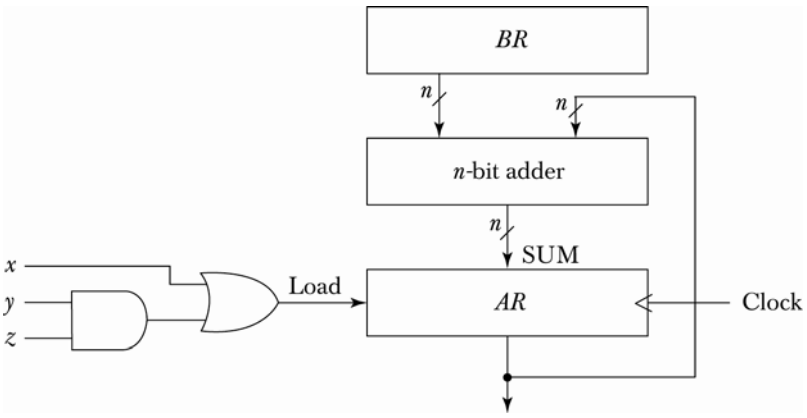
4.6

(a) 4 selection lines to select one of 16 registers.
(b) 16 × 1 multiplexers.
(c) 32 multiplexers, one for each bit of the registers.

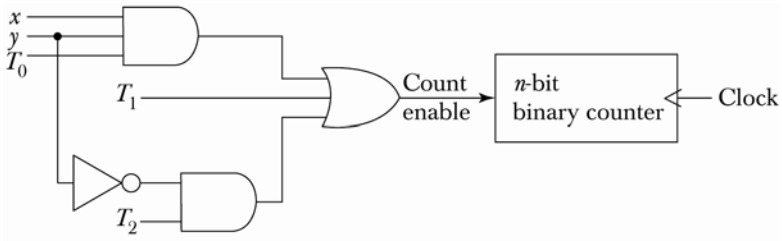
4.7

(a) Read memory word specified by the address in AR into register R2.
(b) Write content of register R3 into the memory word specified by the address in AR.
(c) Read memory word specified by the address in R5 and transfer content to R5 (destroys previous value)

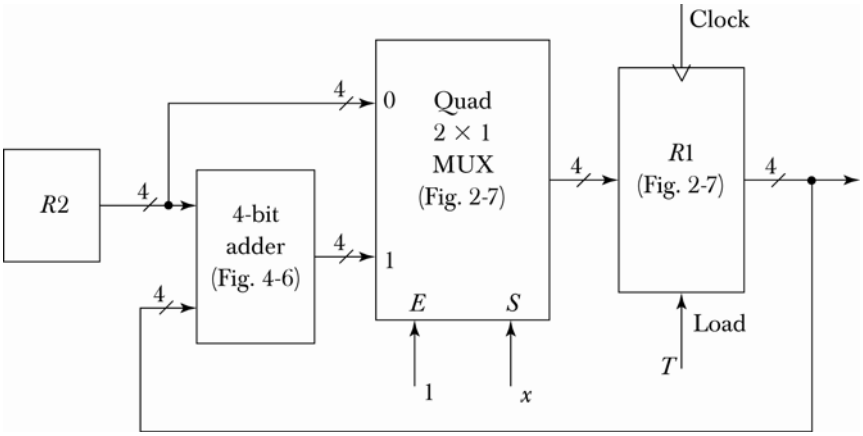
4.8



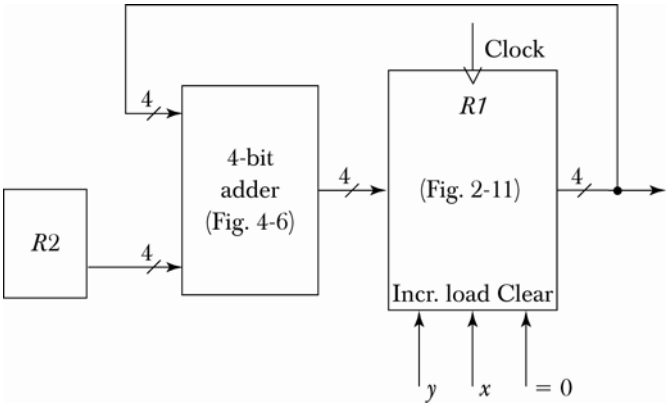
4.9



4.10



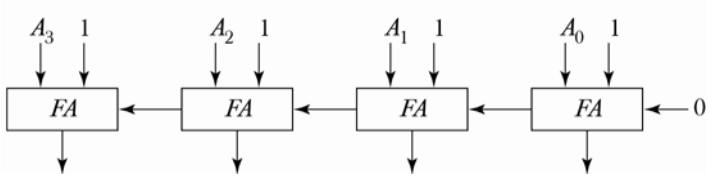
4.11



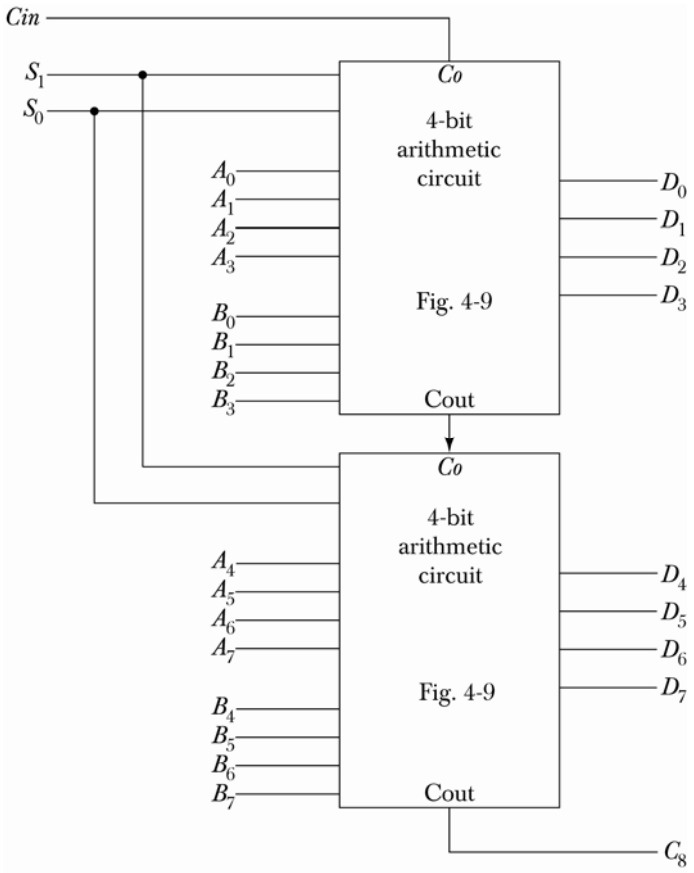
4.12

M	A	B	Sum	Cu	
0	0111	+ 0110	1101	0	7 + 6 = 13
0	1000	+ 1001	0001	1	8 + 9 = 16 + 1
1	1100	– 1000	0100	1	12 – 8 = 4
1	0101	– 1010	1011	0	5 – 10 = – 5(in 2's comp.)
1	0000	– 0001	1111	0	0 –1 = –1 (in 2's comp.)

4.13 A – 1 = A + 2's complement of 1 = A + 1111

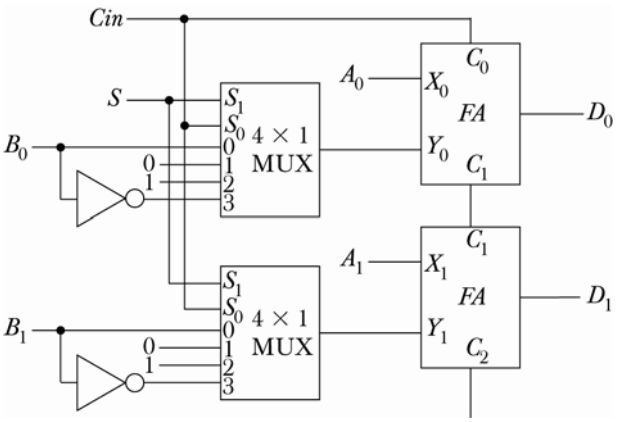


4.14

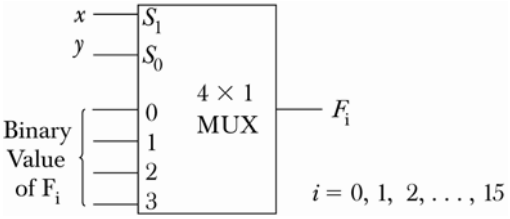


4.15

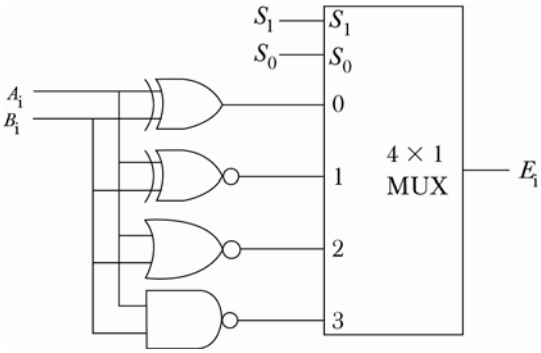
S	Cin	X	Y	
0	0	A	B	(A + B)
0	1	A	0	(A + 1)
1	0	A	1	(A –1)
1	1	A	$\overline{B}$	(A – B)



4.16



4.17



4.18

(a) A = 11011001 ⊕
B = 10110100
A ← A⊕B 01101101

A = 11011001
B = 11111101 (OR)
11111101 A ← AVB

4.19

(a) AR = 11110010
BR = 11111111(+)
AR = 11110001 BR = 11111111 CR = 10111001 DR= 1110 1010

(b) CR = 10111001 BR = 1111 1111
DR = 11101010(AND) +1
CR = 10101000 BR = 0000 0000 AR = 1111 0001 DR = 11101010

(c) AR = 11110001 (–1)
CR = 10101000
AR = 01001001; BR = 00000000; CR = 10101000; DR = 11101010

4.20

R = 10011100
Arithmetic shift right: 11001110
Arithmetic shift left: 00111000 overflow because a negative number changed to positive.

4.21

R = 11011101
Logical shift left: 10111010
Circular shift right: 01011101
Logical shift right: 00101110
Circular shift left: 01011100

4.22

S = 1 Shift left

A_0 A_1 A_2 A_3 I_L

1 0 0 1 0

H = 0 0 1 0 shift left

4.23

(a) Cannot complement and increment the same register at the same time.

(b) Cannot transfer two different values (R_2 and R_3) to the same register (R_1) at the same time.

(c) Cannot transfer a new value into a register (PC) and increment the original value by one at the same time.