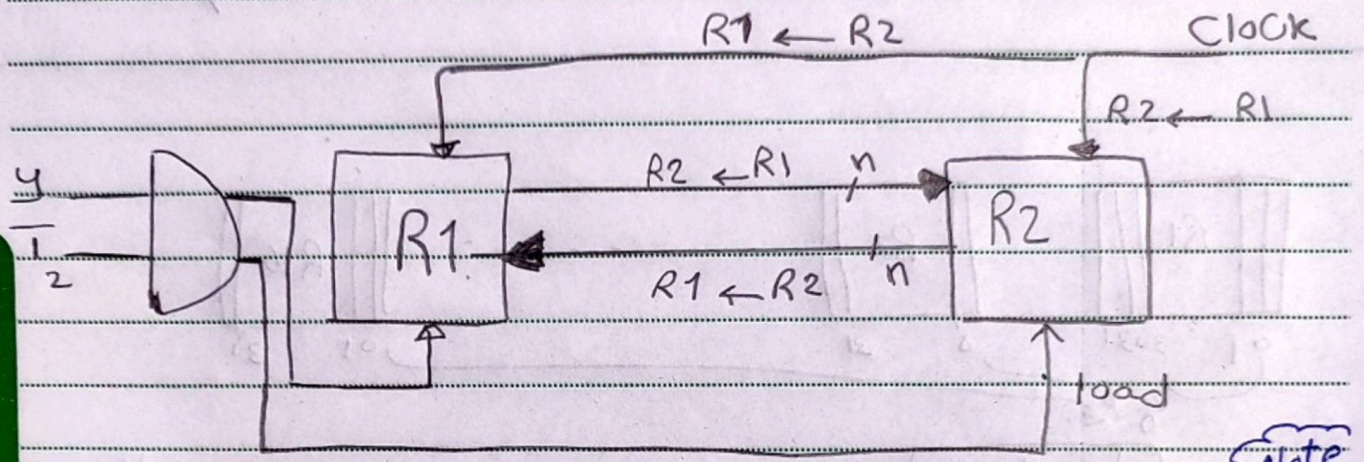
Date: Page:

Computer Architecture

$y, \bar{T}_2$ $R2 \leftarrow R1$, $R1 \leftarrow R2$

and

R mean register



Note

data الـ Register بيستقبل الـ load الـ بيجي لـ

clock الـ بيروح لـ

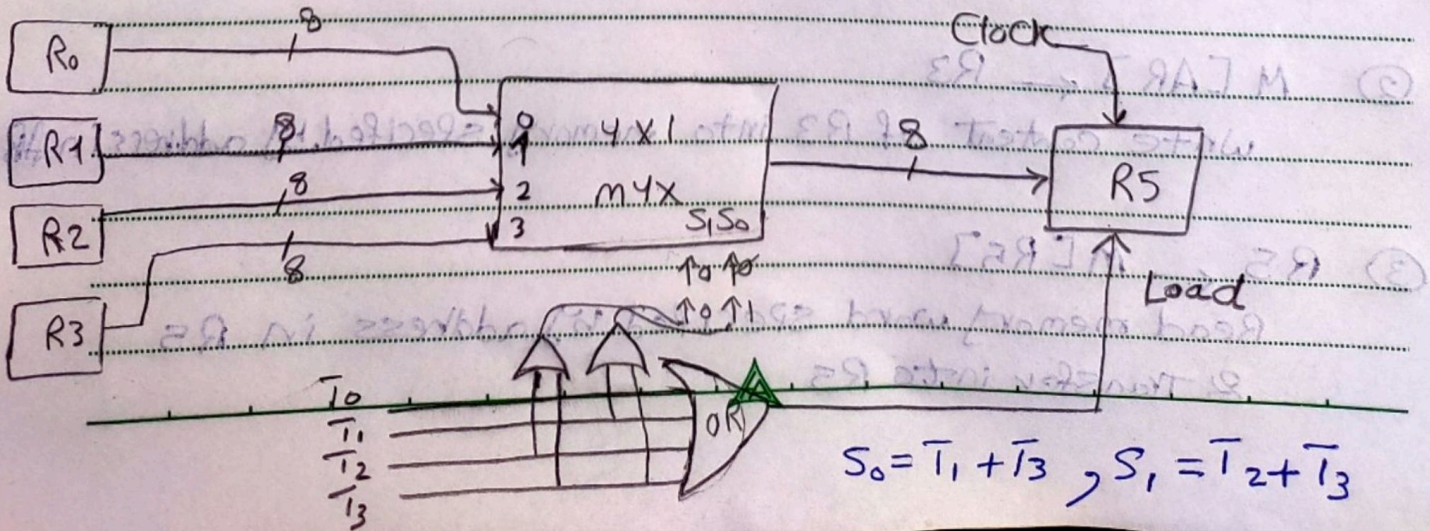
$y \oplus T$ → OR

example: $y=2$ T_0 : $R5 \leftarrow R0$ T_1 : $R5 \leftarrow R1$

T_2 : $R5 \leftarrow R2$ T_3 : $R5 \leftarrow R3$

→ every Register has 8-bits.

only one register make copy (=1) and others should be zero.



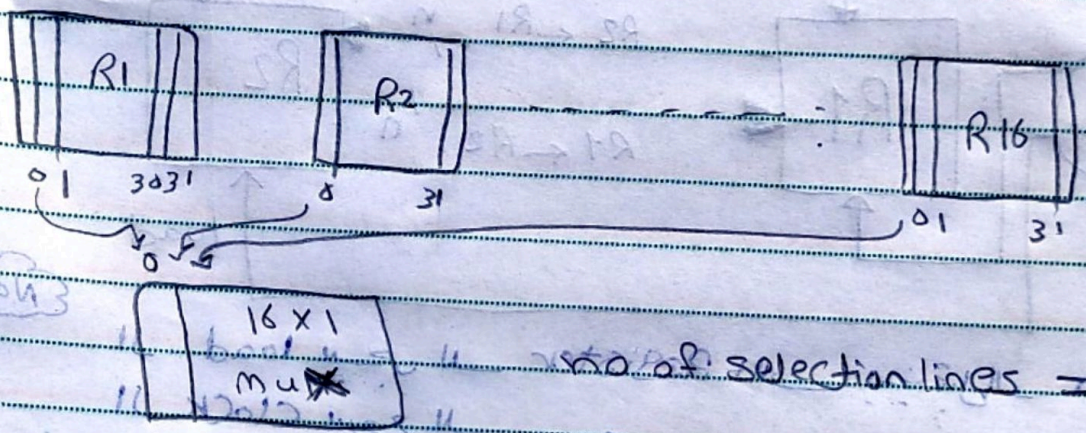
Date: Page:

Question:- if (P=1) Then R1 ← R2
else if (Q=1) Then R1 ← R3

Sol:-

P : R1 ← R2

P'Q : R1 ← R3 P' → 0



no of selection lines = 2^4

note:-

no of bits ⇒ mux bits = mux

no of register ⇒ mux size R_5 = mux size

4.7 write what are mean??

① R2 ← M[AR]

Read memory word specified by address in AR register & transfer into R2

② M[AR] ← R3

write content of R3 into memory specified by address in AR

③ R5 ← M[R5]

Read memory word specified by address in R5 & Transfer into R5