In general for any bus Transfer system:-

K register of n bits can be multiplexed to produce an n-line common bus, where:

- n muxs are needed (= bit numbers)
- The size of each MUX is $K \times 1$ (= number of register) $\times 1$ — no of inputs register
- W selection lines are needed where, $2^w \geq k$ → $\boxed{\log_2 \text{muxs}}$

* selection line = $\log_2$ inputs

example: for register R0 to R63 in a 16-bit bus system; what is the mux size we use? and how many select bits are needed?

Size = 64×1 = 64

no of muxs = 16

no of selection line ⇒ 2^{4} ⇒ $\boxed{4}$

Memory Transfer:-

- The read operation is the transfer of information from a memory word to the outside environment: $DR \leftarrow M[AR]$ (Data register; address register)
- The write operation: is the transfer of new information to be stored into a memory word $M[AR] \leftarrow R1$

What is memory word? address of data in memory

- Computer Microoperations
- Arithmetic microoperations
- Arithmetic addition and Subtraction

Microoperation:- The operations on the data in registers

Computer Microoperations 3 types:

1- Arithmetic 2- logic 3- Shift

Arithmetic microoperations

Symbolic designation	Description
$R3 \leftarrow R1 + R2$	Contents of R1 Plus R2 Transferred to R3
$R3 \leftarrow R1 - R2$	~ ~ R1 Minus R2 ~ ~ R3
$R2 \leftarrow \overline{R2}$	1's Complement The contents of R2
$R2 \leftarrow \overline{R2} + 1$	2's ~ ~ ~ (negate) لو جمع 1 على R2 ده ضيف المتمم الثاني
$R3 \leftarrow R1 + \overline{R2} + 1$	R1 Plus The 2's Complement of R2 (Subtract)
$R1 \leftarrow R1 + 1$	Increment R1 by one
$R1 \leftarrow R1 - 1$	Decrement ~ ~

Arithmetic addition: $R3 \leftarrow R1 + R2$

Arithmetic subtraction: كثاني

* $R3 \leftarrow R1 + (R2' + 1)$, 2's Complement $\equiv R1 - R2$
* R1 - R2 إضافة محتويات الـ 2's Complement الـ بيجعل آخر كأنها تساوي -
- على الطرح عبر عنها بجمع المتمم الثاني للمطروح

steps
- $R2'$ is The Complement of R2
- Adding 1 to The 1's Complement of R2 gives The 2's Comp of R2
- Adding R1 to the 2's Comple of R2 is equivalent to subtracting R2 from R1

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example "التشكير"

$R1 = 1000$
$R2 = 1101$ +

$\underbrace{1}_{2}0101 = R1 + R2$

[R1 - R2]??

① find $R2' = 0010$ → 1'S Complement
② add 1 to $R2'$ 2'S Complement

= 0010
1 +

$R2'+1 = 0011$ → 2'S Complement

③ add R1 to $R_2'+1$

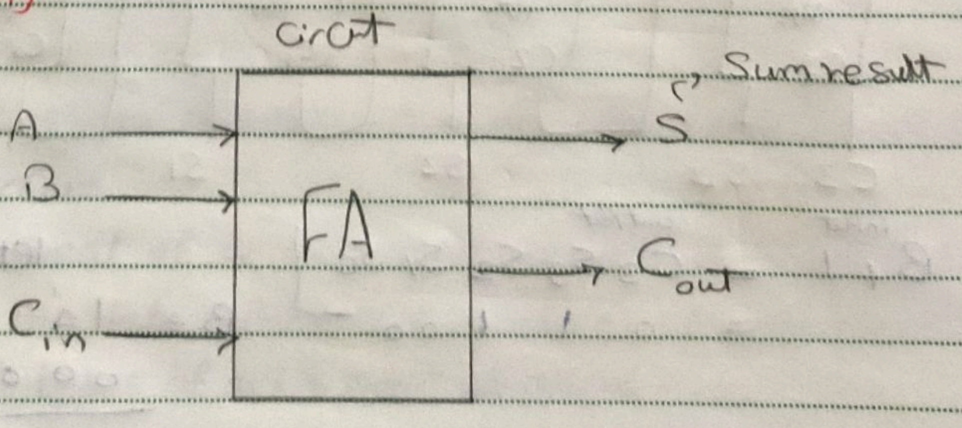
R_1 1000
$R2'+1$ 0011 +

$1011 = R1 - R2$

Arithmetic hardware implementation

① 4-bit binary adder ② 4-bit binary adder Subtractor
③ 4-bit binary incrementer

for remindering



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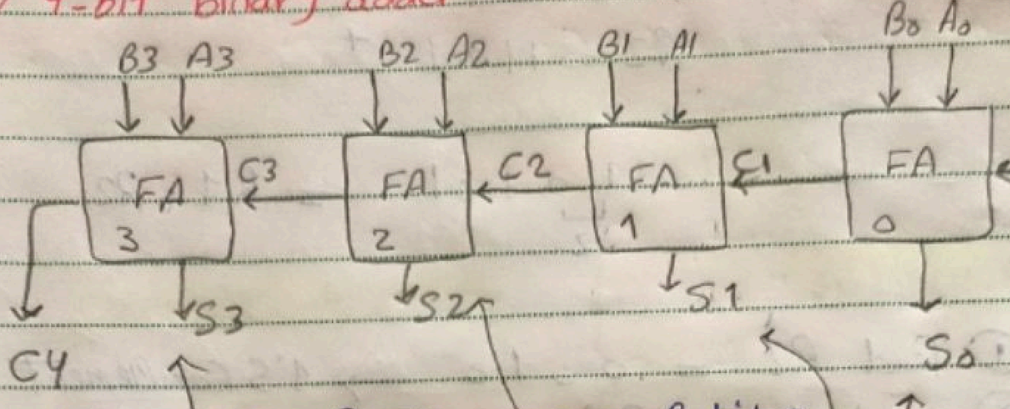
① 4-bit binary adder



$C_0 = C_{in}$ Should be grounded

توصل بالأرض

Note → no of FA = no of bits

let اوزان

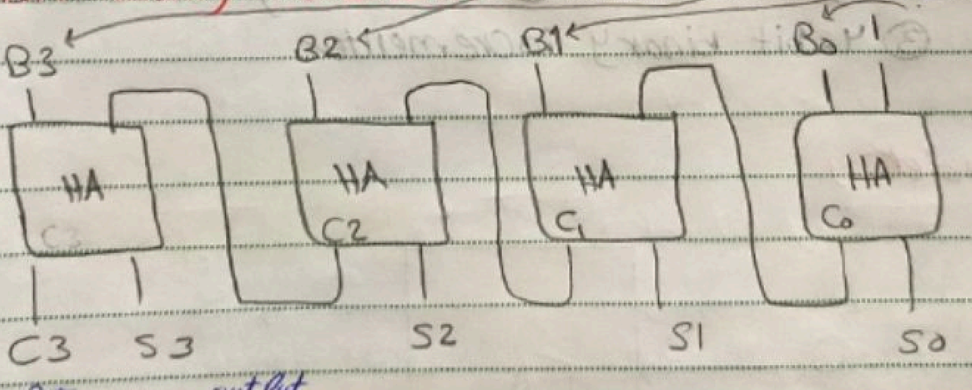
$$\left[\begin{array}{l} A = A_3 A_2 A_1 A_0 = 1\ 0\ 1\ 0 \\ B = B_3 B_2 B_1 B_0 = 0\ 0\ 1\ 0 \end{array}\right.$$

* Cout of FA1 ⟶ Cin of FA2

$$Sum = A + B = \begin{array}{r} 1010 \\ +\ 0010 \\ \hline 01100 \end{array}$$

$C_4 \quad S_3 \quad S_2 \quad S_1 \quad S_0$

② 4 bit binary incrementor $B = B_3 B_2 B_1 B_0$



$\underset{input}{B+1} = \underset{output}{C_3 S_3 S_2 S_1 S_0}$
$= 0\ 1\ 1\ 0\ 0$

let

$$B = \begin{array}{r} 1011 \\ +\ 0001 \\ \hline 01100 \end{array}$$

binary
2 → 10

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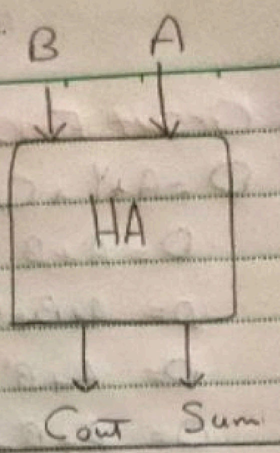
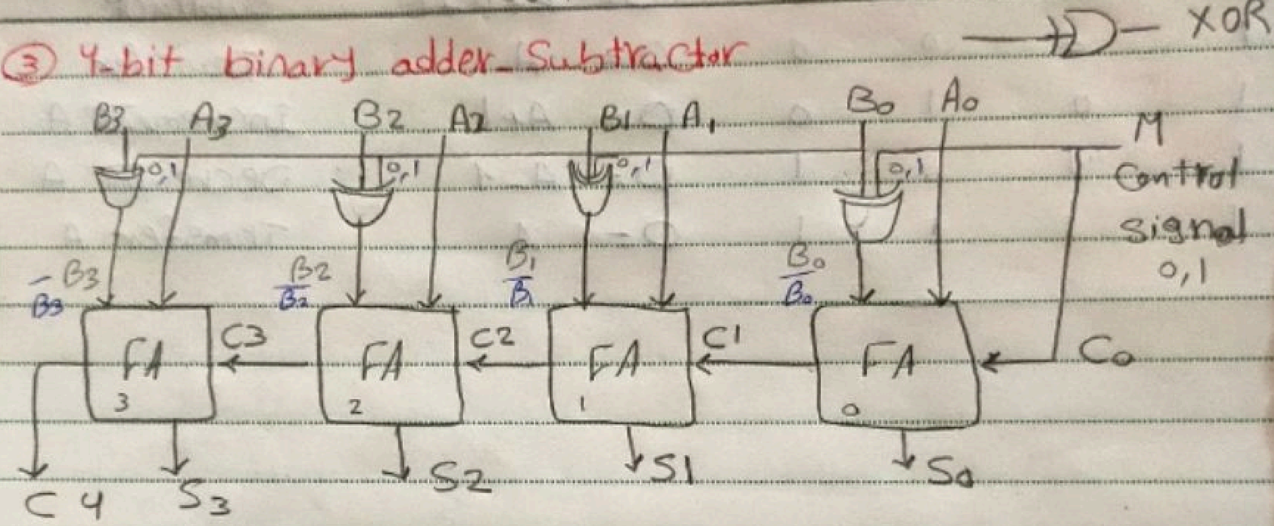
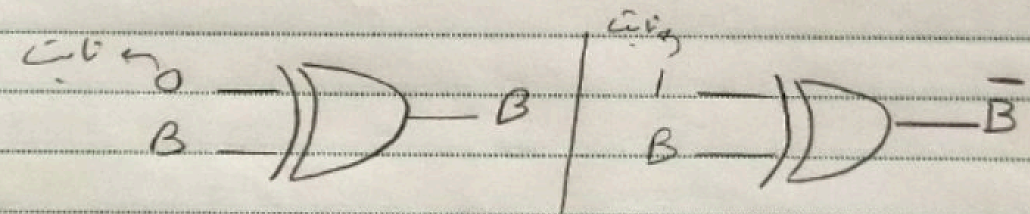


remind

③ 4-bit binary adder-Subtractor



advantages of XOR gate



لو

$M = 0 \xrightarrow{Sum} A + B$, $M = 1$ $A_0 + \bar{B}_0 + 1 = A_0 - B_0$

Arithmetic Circuit

- The arithmetic micro operations can be implemented in one composite arithmetic circuit.
- The basic component of an arithmetic circuit is the parallel adder
- By controlling the data inputs to the adder, it is ~~the~~ possible to obtain different types of arithmetic operations.
- The output of binary adder is calculated from arithmetic sum

$$D = A + Y + C_{in}$$

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Arithmetic Circuit Function

S_1	S_0	C_{in}	Y	$D = A + Y + C_{in}$	Microoperation
0	0	0	B	$D = A + B$	Add
0	0	1	B	$D = A + B + 1$	Add with Carry
0	1	0	B'	$D = A + B'$	Subtract with borrow
0	1	1	B'	$D = A + B' + 1$	Subtract
1	0	0	0	$D = A$	Transfer
1	0	1	0	$D = A + 1$	Increment A
1	1	0	1	$D = A - 1$	Decrement A
1	1	1	1	$D = A$	Transfer A