

# Assignment 5.1

## Linear Feedback Shift Register

### Introduction: -

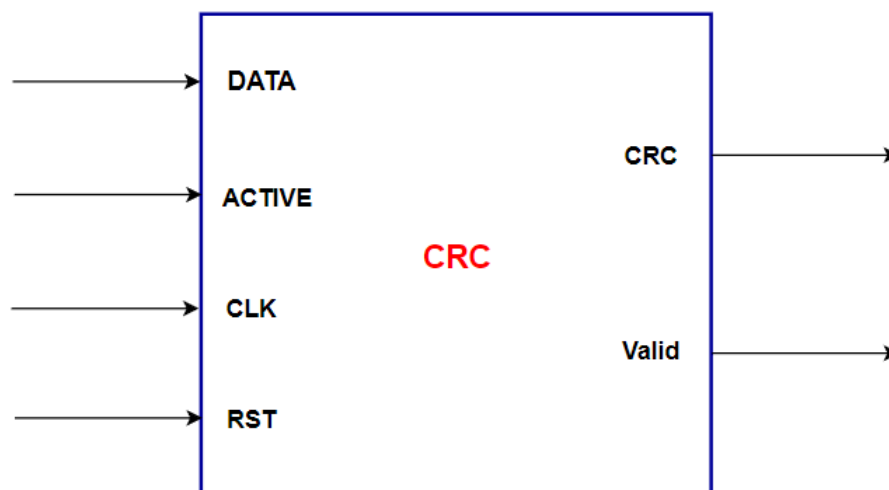
#### What is LFSR?

- The **LFSR** is a **shift register** that has some of its outputs together in **exclusive-OR** or **exclusive-NOR** configurations to form a feedback path.
- The initial content of the shift register is referred to as **seed**. (Note: any value can be a seed except all 0's to avoid lookup state)

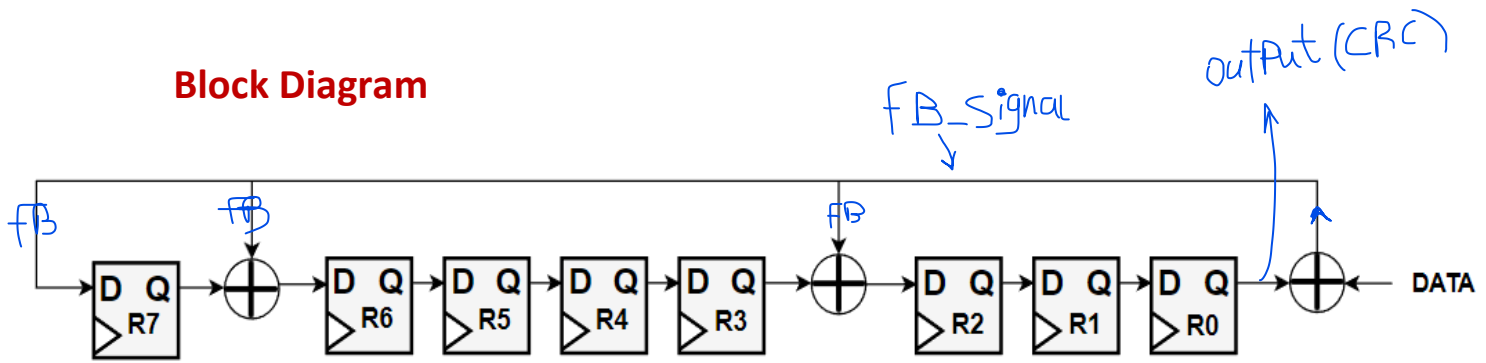
#### LFSR Applications

- 1) Pattern Generators
- 2) Encryption
- 3) Compression
- 4) CRC
- 5) Pseudo-Random Bit Sequences (PRBS)

### Block Interface



## Block Diagram



## Specification

1. All registers are cleared using asynchronous active low reset
2. All outputs are registered
3. DATA serial bit length vary from 1 byte to 4 bytes
4. ACTIVE input signal is high signal during data transmission, low otherwise.
5. CRC 8 bits are shifted serially through CRC output port
6. Valid signal is high during CRC bits transmission, otherwise low.

## Operation:

1. **Initialize** the shift registers (R7 – R0) to zeros
2. **Shift** the data bits into the LFSR in the order of **LSB first**.
3. After the last data bit is shifted into the LFSR, the registers contain the CRC bits
4. Shift out the CRC bits in the (R7 – R0) in order, R0 contains the LSB

## Requirements: -

- 1- Design a LFSR with the above specifications using Verilog language.
- 2- Write a testbench to validate your design using
  - Clock frequency: 10 MHz