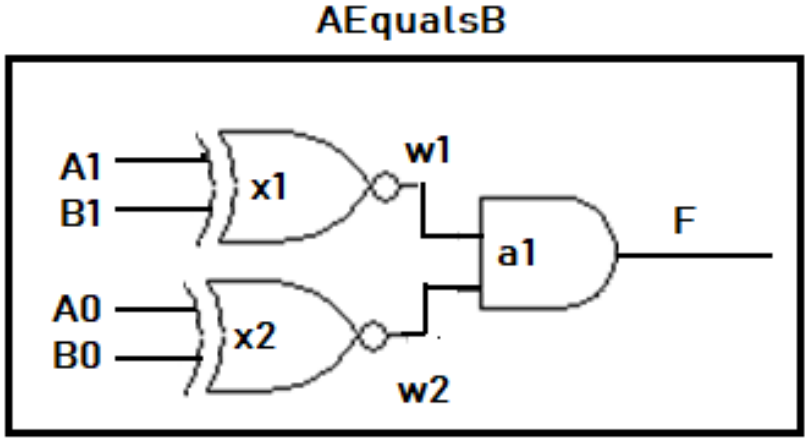
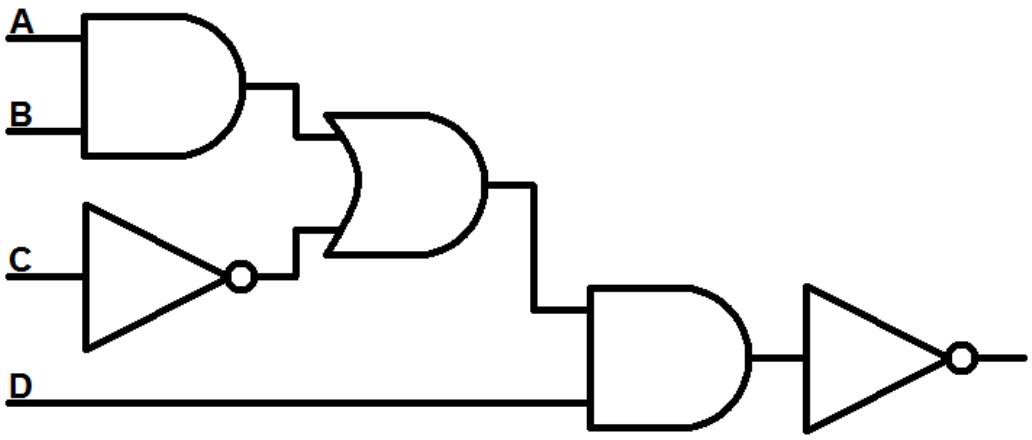
Problem 1: Draw the logic circuit described by the Verilog code below.

```
module AEqualsB (A1, A0, B1, B0, F);
        input A1, A0, B1, B0;
        output F;
        wire w1, w2;
        and a1 (F, w1, w2);
        xnor x1 (w1, A1, B1);
        xnor x2 (w2, A0, B0);
endmodule
```

Solution:



Problem 2: Write a Verilog explicit structural description of the following logic.



Solution:

```
module Quiz1_q2 (A, B, C, D, F);
        input A, B, C, D;
        output F;
        wire t1, t2, t3, t4;
        and a1 (t1, A, B);
        not n1 (t2, C);
        or o1 (t3, t1, t2);
        and a2 (t4, t3, D);
        not n2 (F, t4);
endmodule
```