Name: SHAH RAZA

REG NO: 18PWCSE1658

SECTION: B

SUBJECT: DSD

Exam: MID TERM

PROBLEM 1:

Solution:

```
module counter(clock, reset, out);
        input clock, reset;
        output [2:0] out;
        wire Qn0, Qn1, Qn2;
        wire w1, w2;

        not (w1, out[0], out[2]);
        and (w2, out[1], Qn2);
        DFF dff0(out[2], clock, reset, out[0], Qn0);
        DFF dff1(w1, clock, reset, out[1], Qn1);
        DFF dff2(w2, clock, reset, out[2], Qn2);
endmodule
```

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PROBLEM 2:

Solution:

```
module Mux8to1 (sel, I0, I1, I2, I3, I4,
                I5, I6, I7, OUT);
  input [2:0] sel;
  input I0, I1, I2, I3, I4, I5, I6, I7;
  output OUT;
  reg OUT;

  always @(*)
    case (sel)
      3'b000: OUT = I0;
      3'b001: OUT = I1;
      3'b010: OUT = I2;
      3'b011: OUT = I3;
      3'b100: OUT = I4;
      3'b101: OUT = I5;
      3'b110: OUT = I6;
      3'b111: OUT = I7;
    endcase
endmodule
```

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PROBLEM 3:

Solution:

```
module Design(clk, reset, D0, D1, D2, D3,
              D4, D5, D6, D7, OUT);
input clk, reset, D0, D1, D2, D3, D4,
      D5, D6, D7;
output OUT;
wire [2:0] Cout;

Counter ct(clk, reset, Cout);
Mux8to1 mux(Cout, D0, D1, D2, D3
            D4, D5, D6, D7, OUT);
endmodule
```