Problem 1: Draw the logic circuit described by the Verilog code below.

```
module AEqualsB (A1, A0, B1, B0, F);
        input A1, A0, B1, B0;
        output F;
        wire w1, w2;
        and a1 (F, w1, w2);
        xnor x1 (w1, A1, B1);
        xnor x2 (w2, A0, B0);
endmodule
```

Problem 2: Write a Verilog explicit structural description of the following logic.