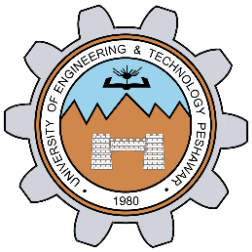
DIGITAL SYSTEM DESIGN LAB

LAB #04



Spring 2021

CSE308L DSD LAB

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"On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work."

Student Signature: _____

Submitted to:

Engr. Madiha Sher

Monday, May 10, 2021

Department of Computer Systems Engineering

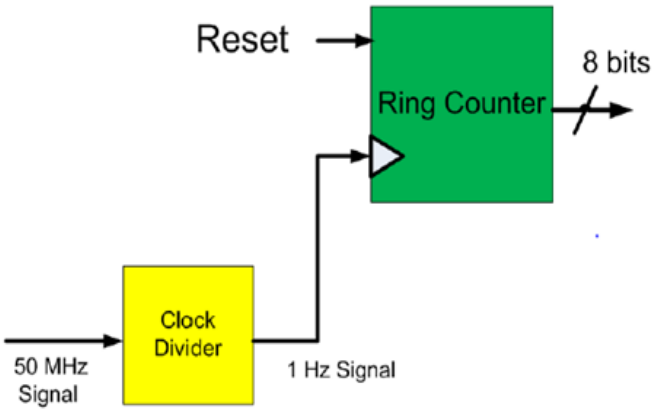
University of Engineering and Technology, Peshawar

Objectives:

This lab will enable students to:

- Code using Behavioral level modeling
- Implement an 8 Bit Ring Counter

Task # 01: Implementation of 8 bit Ring Counter.



Pictorial View of the Operation of a Ring Counter

count [7:0]								
	0	0	0	0	0	0	0	1
	0	0	0	0	0	0	1	0
	0	0	0	0	0	1	0	0
	0	0	0	0	1	0	0	0
t	0	0	0	1	0	0	0	0
	0	0	1	0	0	0	0	0
	0	1	0	0	0	0	0	0
	1	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1

Code:

Ring Counter:

```
module Counter_8bit(clock,reset,Output);
	input clock,reset;
	output [7:0] Output;

	reg [7:0] C;

	always @(posedge clock or reset)
		if(reset)
			C = 8'b00000001;
		else
		begin
			C <= C << 1;
			C[0] <= C[7];
		end
		assign Output = C;
endmodule
```

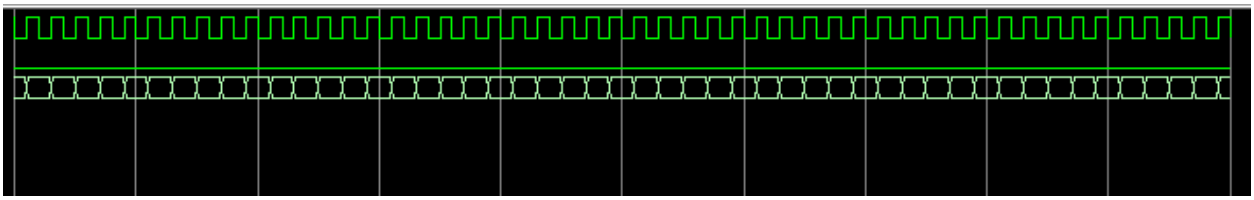
Test Bench:

```
module testCounter;
        reg clk, rst;
        wire [7:0] Out;

        Counter_8bit c1(clk,rst,Out);
        always
                #1 clk = ~clk;
        initial
        begin
                $display("Rst  Out");
                clk = 0; rst = 1;
                $monitor("%b  %b",rst,Out);
                #1 rst =1;
                #1 rst =0;
                #28 $stop;
        end

endmodule
```

Output:

```
# Rst  Out
# 1  00000001
# 0  00000010
# 0  00000100
# 0  00001000
# 0  00010000
# 0  00100000
# 0  01000000
# 0  10000000
# 0  00000001
# 0  00000010
# 0  00000100
# 0  00001000
# 0  00010000
# 0  00100000
# 0  01000000
# 0  10000000
```

Waveform:



Dataflow: