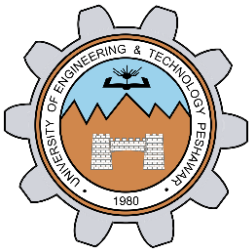
DIGITAL SYSTEM DESIGN LAB

LAB #08



Spring 2021

CSE308L DSD LAB

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"On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work."

Student Signature: _____

Submitted to:

Engr. Madiha Sher

Saturday, July 3, 2021

Department of Computer Systems Engineering

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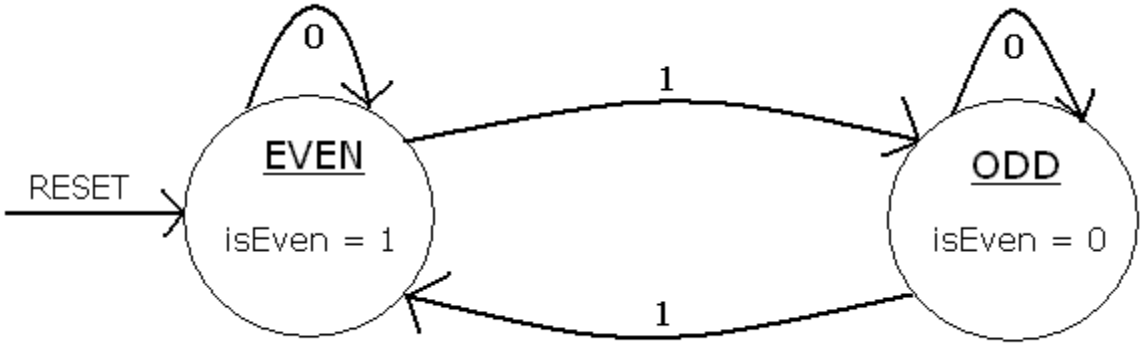
Task # 01:

Implement an even/odd checker using FSM.

This FSM asserts its output whenever it has seen an even number of 1's. Otherwise the output is low.

Problem Analysis:

State Diagram:



Code:

Parity Checker:

```
module ParityChecker(in,clk,rst,z);
	input in,clk,rst;
	output z;
	reg z;

	parameter EVEN = 1, ODD = 0;

	reg PS,NS;

	always @(posedge clk or rst)
		if(rst)
			PS = EVEN;
		else
			PS = NS;

	always @(PS or in)
	begin
		case(PS)
```

```
                EVEN:
                begin
                NS = in?ODD:EVEN;
                z = in?0:1;
                end
                ODD:
                begin
                NS = in?EVEN:ODD;
                z = in?1:0;

                end
        endcase
    end

endmodule
```

TestBench:

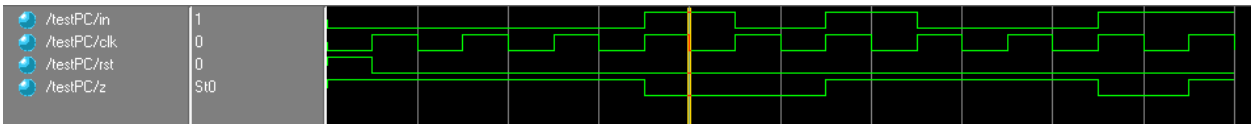
```
module testPC;
    reg in,clk,rst;
    wire z;

    ParityChecker pc(in,clk,rst,z);

    always
        #5 clk = ~clk;

    initial
    begin
        $display ("rst    in     out");
        $monitor ("%b     %b     %b",rst,in,z);
        rst =1;
        clk = 0;
        in = 0;
        #5
        rst = 0;
        #10
        in = 0;
        #10
        in = 0;
        #10
        in = 1;
        #10
        in = 0;
        #10
        in = 1;
        #10
        in = 0;
```

```
            #10
            in = 0;
            #10
            in =1;
        end
endmodule
```

Output:

```
# rst   in    out
# 1     0     1
# 0     0     1
# 0     1     0
# 0     0     0
# 0     1     1
# 0     0     1
# 0     1     0
# 0     1     1
```

Waveform:



Dataflow: