Computer Organization and Architecture

MIPS Architecture

Lecture: 04

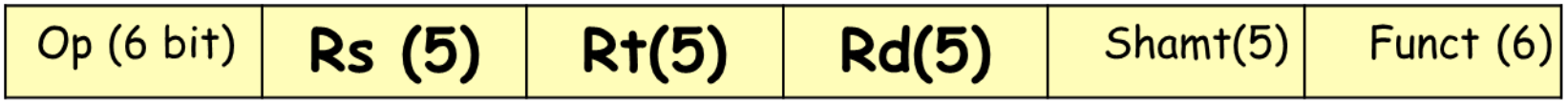
Fall, 2020

R type instruction

Main processor instructions that do not require a target address, immediate value, or branch displacement use an R-type coding format.

This format has fields for specifying of up to three registers and a shift amount.

For instructions that do not use all of these fields, the unused fields are coded with all 0 bits.



opcode 0.

rs: 1st register operand (register source) (5 bits)

rt: 2nd register operand (5 bits)

rd: register destination (5 bits)

shamt: shift amount (0 when N/A) (5 bits)

funct: function code (identifies the specific R-format instruction) (6 bits)

Instruction		Function
add	rd, rs, rt	100000
addu	rd, rs, rt	100001
and	rd, rs, rt	100100
break		001101
div	rs, rt	011010
divu	rs, rt	011011
jalr	rd, rs	001001
jr	rs	001000
mfhi	rd	010000
mflo	rd	010010
mthi	rs	010001
mtlo	rs	010011
mult	rs, rt	011000
multu	rs, rt	011001
nor	rd, rs, rt	100111
or	rd, rs, rt	100101
sll	rd, rt, sa	000000
sllv	rd, rt, rs	000100
slt	rd, rs, rt	101010
sltu	rd, rs, rt	101011
sra	rd, rt, sa	000011
srav	rd, rt, rs	000111
srl	rd, rt, sa	000010
srlv	rd, rt, rs	000110
sub	rd, rs, rt	100010
subu	rd, rs, rt	100011
syscall		001100

R- I and J type Instructions

Type	**31--26**	**25---21**	**20---16**	**15---11**	**10---06**	**05--00**
R-Type	opcode	$rs	$rt	$rd	shamt	funct
I-Type	opcode	$rs	$rt	imm		
J-Type	opcode	address				

I Type Instruction

- Have a constant value immediately present in the instruction.
- Also have:
    - rs: register containing base address (5 bits)
    - rt: register destination/source (5 bits)
    - immediate: value or offset (16 bits)

Name	Format	Layout						Example
		6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	
		op	rs	rt	immediate			
beq	I	4	1	2	25 (offset)			beq $1, $2, 100
bne	I	5	1	2	25 (offset)			bne $1, $2, 100
addi	I	8	2	1	100			addi $1, $2, 100
addiu	I	9	2	1	100			addiu $1, $2, 100
andi	I	12	2	1	100			andi $1, $2, 100
ori	I	13	2	1	100			ori $1, $2, 100
slti	I	10	2	1	100			slti $1, $2, 100
sltiu	I	11	2	1	100			sltiu $1, $2, 100
lui	I	15	0	1	100			lui $1, 100
lw	I	35	2	1	100 (offset)			lw $1, 100($2)
sw	I	43	2	1	100 (offset)			sw $1, 100($2)

I Type Instruction

- I-type instructions have a 16-bit imm field that codes one of the following types of information.
- An immediate operand
- A memory operand displacement
- For the bgez, bgtz, blez, and bltz instructions, the rt field is used as an extension of the opcode field.

Instruction		Opcode	Notes
addi	rt, rs, imm	001000	
addiu	rt, rs, imm	001001	
andi	rt, rs, imm	001100	
beq	rs, rt, label	000100	
bgez	rs, label	000001	rt = 00001
bgtz	rs, label	000111	rt = 00000
blez	rs, label	000110	rt = 00000
bltz	rs, label	000001	rt = 00000
bne	rs, rt, label	000101	

J-format Instructions

•Have an address (part of one, actually) in the instruction.

Name	Format	Layout						Example
		6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	
		op	address					
j	J	2	2500					j 10000
jal	J	3	2500					jal 10000