DIGITAL SYSTEM DESIGN LAB

LAB #03



Spring 2021 CSE308L DSD LAB

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Class Section: **B**

"On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work."

Student Signature:

Submitted to:

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Wednesday, May 5, 2021

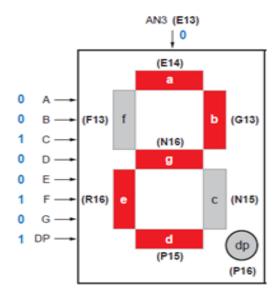
Department of Computer Systems Engineering
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Objectives:

This lab will enable students to:

- Learn top down and bottom up design methodologies
- Use seven segment display available on the S3board
- Data flow level modeling

Task # 01: BCD to Seven Segment Decoder.



Problem Analysis:

Truth Table:

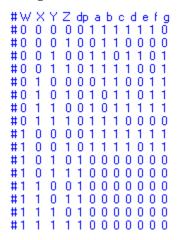
II uu I											
\mathbf{W}	X	Y	Z	dp	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	0	1	1	0	0	0	0
0	0	1	0	0	1	1	0	1	1	0	1
0	0	1	1	0	1	1	1	1	0	0	1
0	1	0	0	0	0	1	1	0	0	1	1
0	1	0	1	0	1	0	1	1	0	1	1
0	1	1	0	0	1	0	1	1	1	1	1
0	1	1	1	0	1	1	1	0	0	0	0
1	0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	0	1	1
1	0	1	0	1	0	0	0	0	0	0	0
1	0	1	1	1	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0	0
1	1	0	1	1	0	0	0	0	0	0	0
1	1	1	0	1	0	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

```
Code:
Module:
module BCDto7S(dp,Segment,BCD);
                       input [3:0] BCD;
                       output [6:0] Segment;
                       output dp;
                       assign {dp,Segment} = (BCD==4'b0000)?8'b01111110:
                                                                                 (BCD==4'b0001)?8'b00110000:
                                                                                 (BCD==4'b0010)?8'b01101101:
                                                                                 (BCD==4'b0011)?8'b01111001:
                                                                                 (BCD==4'b0100)?8'b00110011:
                                                                                 (BCD==4'b0101)?8'b01011011:
                                                                                 (BCD==4'b0110)?8'b01011111:
                                                                                 (BCD==4'b0111)?8'b01110000:
                                                                                 (BCD==4'b1000)?8'b01111111:
                                                                                 (BCD==4'b1001)?8'b01111011:8'b10000000;
endmodule
Test Bench:
module testBCDto7S;
                       reg [3:0] BCD;
                       wire [6:0] Segment;
                       wire dp;
                      BCDto7S m1(dp,Segment,BCD);
                       initial
                       begin
                                              $display("W X Y Z dp a b c d e f g");
                                              $monitor("%b %b %b %b %b %b %b %b %b %b %b,
BCD[3],BCD[2],BCD[1],BCD[0],dp,Segment[6],Segment[5],Segment[4],Segment[3],Segment[2],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Segment[6],Se
nt[1],Segment[0]);
                                             BCD = 4'b0000;
                                             #5
                                             BCD = 4'b0001;
                                             BCD = 4'b0010;
                                             #5
                                             BCD = 4'b0011;
                                             BCD = 4'b0100;
                                             BCD = 4'b0101;
                                             BCD = 4'b0110;
```

```
#5
BCD = 4'b0111;
#5
BCD = 4'b1000;
#5
BCD = 4'b1001;
#5
BCD = 4'b1010;
BCD = 4'b1011;
#5
BCD = 4'b1100;
BCD = 4'b1101;
#5
BCD = 4'b1110;
#5
BCD = 4'b1111;
```

end endmodule

Output:



Waveform:

At 10ns:

⊞- /testBCDto7S/BCD	0010	(0000 (0001	0010 (0011	(0100 (0101	0110 (0111	(1000 (1001	1010 (1011	(1100 (1101	1110 (1111	
⊕- /testBCDto7S/Segm	1101101) (X X	X X	X X	20000000			
/testBCDto7S/dp	0									
]			

At 25ns:

⊕- /testBCDto7S/BC		(0000)(000	(0010	(0011	(0100	0101	0110	0111	1000	(1001	1010 (1011	1100 (1101	1110 (1111	
⊞-🥙 /testBCDto7S/Se	m 1011011	(2000)		()						(0000000			
🥠 /testBCDto7S/dp	0													

At 40ns:

⊕ /testBCDto7S/BCD :	1000	(0000)	0001	0010	0011	0100	(0101	0110	0111	1000	1001	(1010 (1011	1100 (1101	1110 (1111	
⊕-/testBCDto7S/Segm	1111111	(χ			,0000000			
/testBCDto7S/dp	0														
								l							

At 50ns:

⊕– ⊘ /testBCD		1010	(0000	(0001	0010	0011	0100	0101	0110	(0111	1000	(1001	1010 (1011	1100 (1101	1110 (1111	
⊕- /testBCD	to7S/Segm	0000000								X			0000000			
/testBCD	to7S/dp	1														
					l		l		l							

At 65ns:



Dataflow:

