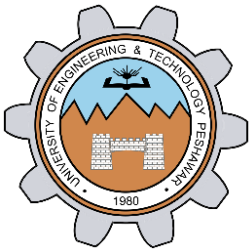
DIGITAL SYSTEM DESIGN LAB

LAB #06



Spring 2021

CSE308L DSD LAB

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Class Section: **B**

"On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work."

Student Signature: _____

Submitted to:

Engr. Madiha Sher

Monday, June 14, 2021

Department of Computer Systems Engineering

University of Engineering and Technology, Peshawar

Objectives:

This lab will enable students to:

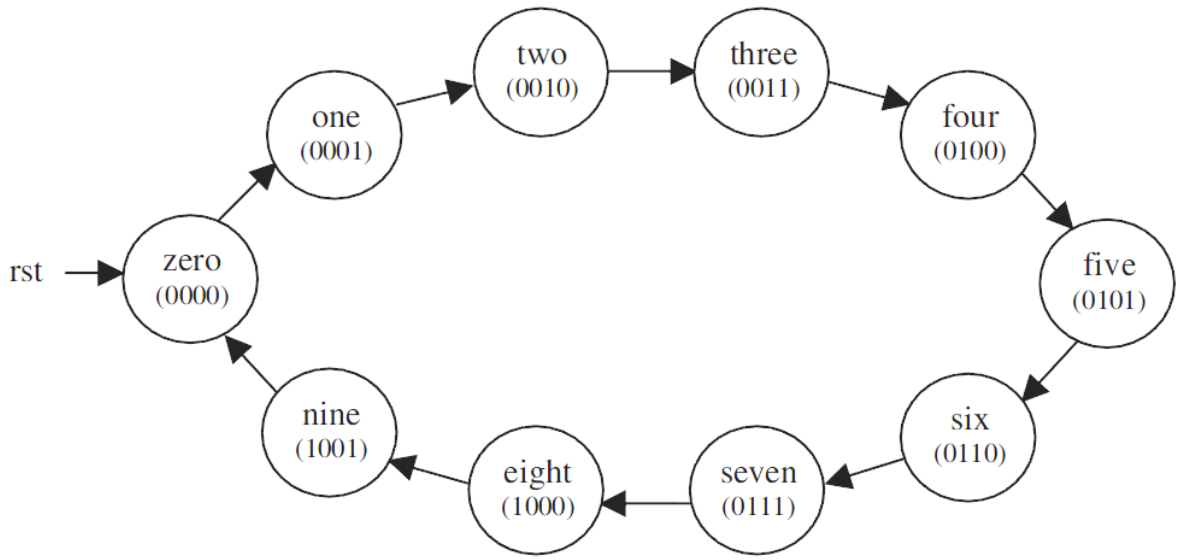
- Code using Behavioral level modeling
- Implement FSM of BCD Counter

Task # 01:

Develop a verilog model for the FSM of BCD Counter (0 – 9), which rolls over when it reaches 9 to 0.

Problem Analysis:

State Diagram:



Code:

BCD Counter:

```
module BCD_Counter(reset,clk,out);
        input reset,clk;
        output [3:0] out;
        reg [3:0] out;

        reg [3:0] state, next_state;

        always @(posedge clk)
                state = next_state;

        always @(state or reset)
        begin
```

```
		if(reset)
			next_state = 4'b0000;
		else
			next_state <= (state<9)?(state+1):4'b0000;
		out = next_state;
	end

endmodule
```

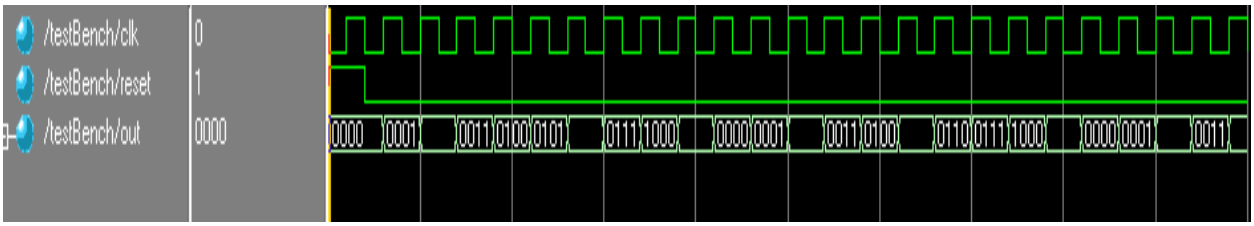
TestBench:

```
module testBench;
	reg clk, reset;
	wire [3:0] out;

	BCD_Counter c1(reset,clk,out);

	always
		#2 clk = ~clk;

	initial
	begin
		clk =0;
		reset = 1;
		$display("reset    out");
		$monitor("%b      %b",reset,out);
		#4
		reset = 0;
		#200 $stop;
	end
endmodule
```

Output:

```
# reset    out
# 1      0000
# 0      0000
# 0      0001
# 0      0010
# 0      0011
# 0      0100
# 0      0101
# 0      0110
# 0      0111
# 0      1000
# 0      1001
# 0      0000
# 0      0001
# 0      0010
# 0      0011
# 0      0100
# 0      0101
# 0      0110
# 0      0111
# 0      1000
# 0      1001
# 0      0000
# 0      0001
# 0      0010
# 0      0011
# 0      0100
```

Waveform:



Dataflow: