

#) DE :

#) Syllabus:

- DE Basics
- Boolean Algebra laws & logic gates
- Boolean exp. (SOP/POS) minimiz.
- Combinational circuit
- Sequential circuit
- Number system & Number rep'

#) DE Basics:

problem \rightarrow Truth table \rightarrow Boolean Exp.

implement using logic gates \leftarrow minimize B.E (K-map)

Note :-

$$a \oplus b = a' \odot b = (a' \odot b)' = (a' \oplus b)'$$

$$a \odot b = a' \oplus b = (a \oplus b)' = a' \odot b'$$

Note:-

$$A \oplus P \oplus A \oplus P = \frac{A \oplus A}{\cancel{A}} \oplus \frac{P \oplus P}{\cancel{P}} = \underline{\underline{0}} \oplus \underline{\underline{0}} = 0$$

o) Boolean exp. :-

1) SOP (considers 1) (used more often)

2) POS (" 0)

x	y	z	o/p
0	0	0	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

1) SOP : Example = $x'y + y'z' + xyz$

Product term which have all literals = minterm

As in above Ex: o/p(x,y,z) = $(\bar{x}\bar{y}z) + (x\bar{y}z) +$

$(xy\bar{z}) + (xyz)$

$= m_1 + m_4 + m_6 + m_7$

$= \Sigma_m(1,4,6,7)$

Canonical form = Every product term have all literals

Ex: $a\bar{b} + a\bar{c} + abc$

$a\bar{b}(c+\bar{c}) + a\bar{c}(b+\bar{b}) + ab\bar{c}$

$a\bar{b}\bar{c} + a\bar{b}c + abc = \Sigma_m(4,5,7)$

2) POS: Example = $(\bar{a}+b)(\bar{b}+\bar{c})(a+c)$

Sum terms which have all literals = maxterm

As in above Ex: o/p(x,y,z) = $(x+y+z) \cdot (\bar{x}+\bar{y}+z)$

$(x+\bar{y}+z) \cdot (\bar{x}+y+\bar{z}) = m_0 \cdot m_2 \cdot m_3 \cdot m_5$

$= \Pi_m(0,2,3,5)$

Canonical form = Every sum term have all literals

Ex: $a \cdot (\bar{b}+c) \cdot (\bar{a}+b+\bar{c})$

$= (a+b\bar{b}+c\bar{c}) \cdot (a\bar{a}+b+c) \cdot (\bar{a}+b+\bar{c})$

$= (a+\bar{b}+\bar{c})(a+\bar{b}+c)(a+b+\bar{c})$

$(a+\bar{b}+c) \cdot (\bar{a}+b+c)$

$(\bar{a}+b+\bar{c})$

$= (011)(010)(001)(000) \cdot (110) \cdot (101)$

$= m_3 \cdot m_2 \cdot m_1 \cdot m_0 \cdot m_6 \cdot m_5$

o) Gates:

NOT) $y = x'$ \Rightarrow

OR) $y = a+b$ \Rightarrow Idempotent, comm., AM.

AND) $y = a \cdot b$ \Rightarrow Idempotent, comm., AM.

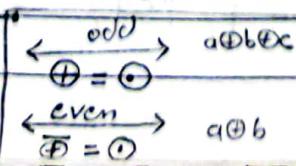
NOR) $y = (a+b)'$ \Rightarrow comm.

NAND) $y = (a \cdot b)'$ \Rightarrow comm.

EX-OR) $y = A \oplus B$ \Rightarrow odd I \Rightarrow I
 $= \bar{a}b + a\bar{b}$ comm. & AM.

EX-NOR) $y = A \odot B$ \Rightarrow even I \Rightarrow I
 $= \bar{a}\bar{b} + ab$ comm. & AM.

Note: If no. of i/p's are odd, then \oplus follows \oplus



• No. of fxⁿ possible

Variables Combi's Fxⁿ

$$n \rightarrow 2^n \rightarrow (2)^{2^n}$$

$$z \rightarrow y^z \rightarrow (x)^{y^z}$$

• 2ⁿ minterms possible

• Duality: 0 → 1 & 1 → 0 & OR → AND AND → OR

but nature of variable remain same

Ex: $a \cdot b$ dual is $a + b$

$a + 0$ dual is $a \cdot 1 = a$

1) Neutral fxⁿ: no. of minterm = no. of maxterm

2) Self dual: if fxⁿ & its dual are same

$$\text{Ex: } f = a \cdot b + b \cdot c + c \cdot a$$

$$f(\text{dual}) = (a+b) \cdot (b+c) \cdot (c+a)$$

Vertical
Self dual

$$= \dots$$

$$= a \cdot b + b \cdot c + c \cdot a$$

From 'n' variables $(2)^{2^{n-1}}$ self dual fxⁿ are possible

• To check self-dual:

1. check if no. of minterms = no. of maxterms

$$\begin{array}{l} 0 \leftrightarrow 7 \\ 1 \leftrightarrow 6 \\ 2 \leftrightarrow 5 \\ 3 \leftrightarrow 4 \end{array} \quad \begin{array}{l} 0 \leftrightarrow 11 \\ 1 \leftrightarrow 10 \\ 2 \leftrightarrow 9 \\ 3 \leftrightarrow 8 \end{array}$$

Pairs of mutually exclusive terms = $2^n / 2$

$$\text{Ex: } f(a, b, c) = \sum_m (0, 1, 2, 4) \checkmark$$

$$f(a, b, c) = \sum_m (0, 1, 6, 7) \times$$

3) Orthogonal: if complement & dual of fxⁿ are same

To check orthogonal:-

1. minterms = maxterms

$$\begin{array}{l} 0 \leftrightarrow 7 \\ 1 \leftrightarrow 6 \\ 2 \leftrightarrow 5 \\ 3 \leftrightarrow 4 \end{array}$$

4) Functionally complete: if a fxⁿ can implement

Not with either AND OR

(Support of 0, 1, complement not allowed)

Partially functionally complete:

(Support of 0, 1 allowed, complement not allowed)

Note: SOP can be implemented using AND-OR ($\overline{\text{NAND}} - \text{NOR}$)

POS can be implemented using OR-AND ($\text{NOR} - \text{NAND}$)

*> BE Simplification:

1) Using K-map 2) using Boolean laws

cd	$\bar{c}\bar{d}$	$\bar{c}d$	$c\bar{d}$	cd	ab	$\bar{a}\bar{b}$	$\bar{a}b$	$a\bar{b}$	ab
ab	00	01	11	10	00	01	11	10	10
00	0	1	3	2	00	0	4	12	8
01	4	5	7	6	01	1	5	13	9
11	12	13	15	14	11	3	7	15	11
10	8	9	11	10	10	2	6	14	0

ad	$\bar{a}\bar{d}$	$\bar{a}d$	$a\bar{d}$	ad	bc	$\bar{b}\bar{c}$	$\bar{b}c$	$c\bar{b}$	bc
bc	00	01	11	10	00	01	11	10	10
00	0	1	9	8	00	0	4	5	1
01	2	3	11	10	01	3	12	13	9
11	6	7	15	14	11	10	14	15	11
10	4	5	13	12	10	2	6	7	3

ab	$\bar{a}\bar{b}$	$\bar{a}b$	$a\bar{b}$	ab	bc	$\bar{b}\bar{c}$	$\bar{b}c$	$c\bar{b}$	bc
c	0	1	2	6	0	1	3	2	2
0	0	2	6	7	0	1	3	2	2
1	1	3	7	5	1	5	7	6	6

a	0	4	1	5	a	0	1	2	b	0	2
1	5	2	6	7	1	2	3	4	1	3	5
3	7				2	6			2		
2	6				0				0		
0					ab	cd	cd	ab	bc	bc	ab

a/bc → always from a
b/cd → always from b

K-map for POS					
$a+b$	$a+b$	$a+b$	$a+b$	$a+b$	
$a+b$	0+0	0+1	1+1	1+0	
0+0	0	+	12	8	$\frac{1+1}{0+2}$
0+1	1	5	13	9	$\frac{1+1}{0+2}$
1+1	3	7	15	11	i.e., $a=0$ $\bar{a}=1$
1+0	2	0	14	10	

Example				
4x4				
0+0	0+1	1+1	1+0	
0	1	0	8	
1	X	0	9	$(\bar{w} + \bar{z})$
3	7	X	11	
2	X	0	10	$(\bar{x} + z)$
				$\Rightarrow (\bar{w} + \bar{z})(\bar{x} + z)$
				!ITerms

$1 \rightarrow 6$

$2 \rightarrow 5$

$3 \rightarrow 4$

Pairs of mutually exclusive terms = $2^n/2$

$$\text{Ex: } f(a, b, c) = \sum_m (0, 1, 2, 4) \quad \checkmark$$

$$f(a, b, c) = \sum_m (0, 1, 6, 7) \quad \times$$

3) Orthogonal: If complement & dual of $f(x)$ sum

To check orthogonal:-

1. minterms = maxterms

$$\begin{array}{l} 0 - 7 \\ 1 - 6 \\ 2 - 5 \\ 3 - 4 \end{array}$$

4) Functionally complete: If a $f(x)$ can implement all functions with either AND OR (Support of 0, 1, complement not allowed)

Partially functionally complete:

(Support of 0, 1 allowed, complement not allowed)

Note: SOP can be implemented using AND-OR (NAND-NOR)

POS can be implemented using OR-AND (NOR-NOR)

Note:)

Abdorption Law

$$a + ab = a$$

$$a \cdot (a+b) = a$$

Compensation

$$ab + \bar{a}c + bc = ab + \bar{a}c$$

$$(a+b)(\bar{a}+c)(b+c) = (a+b)(\bar{a}+c)$$

$$a + \bar{a}b = a + b$$

$$a \cdot (\bar{a} + b) = a \cdot b$$

Note:)

Not + OR = NOR
(Not + And = NAnd)

universal gates

Example: $f(abcd) = \sum_m \{4, 5, 6, 7, 8, 9, 10, 11, 13, 14\}$

ab	00	01	11	10	EPI
00	0	1	12	8	$\bar{a}b + a\bar{b} + b\bar{c}\bar{d} + (\bar{b}c\bar{d})$
01	1	1	13	9	$a\bar{c}d$
11	3	1	15	11	$EPI = 2$
10	2	1	14	10	$NEPI = 4$, PI = 6

Different expressions = 4.

Literals in = 10

Note:)



Note: To check if f is functionally complete

$$\text{Ex: } f(x, y, z) = \bar{x}yz + x\bar{y} + \bar{y}z$$

✓ ① Not preserve 0 $\Rightarrow \bar{0}00 + 0\bar{0} + \bar{0}\bar{0} = 1$

✓ ② Not preserve 1 $\Rightarrow \bar{1}11 + 1\bar{1} + \bar{1}\bar{1} = 0$

✓ ③ Not self dual. $\bar{x}yz + x\bar{y} + \bar{y}z$

$$\begin{array}{l} 0 - 7 \\ 1 - 6 \\ 2 - 5 \\ 3 - 4 \end{array}$$

$$\begin{array}{l} 3 \\ 4, 5 \\ 0, 1 \end{array}$$

NOT, AND, OR, NOR

Note: Total neutral fxns possible
 $= 2^n C_{2^{n-1}}$ bcz. half of 2^n minterms are 1

Note: #neutral $\equiv 2^n C_{\frac{2^n}{2}}$

#Self Dual $\equiv 2^{\frac{2^n}{2}} \equiv$ Orthogonal

Note:)

	NOT	AND	OR	NAND	NOR	Play	with	ExNOR
NAND	1	2	3	4	5	Play	with	mouse
NOR	1	2	3	4	5	sport	ball	

Combinational Circuits:-

*) Adders:-

*) Summary:-

1) Half adder

$$\text{Sum} = A \oplus B$$

$$\text{Carry} = A \cdot B$$

• Using NAND = 5 gates

• Using NOR = 5 gates

2) Full adder

$$\text{Sum} = A \oplus B \oplus C$$

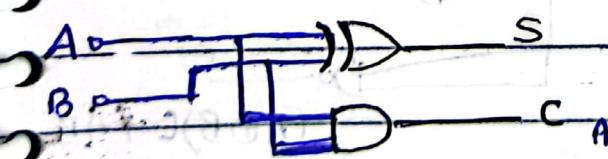
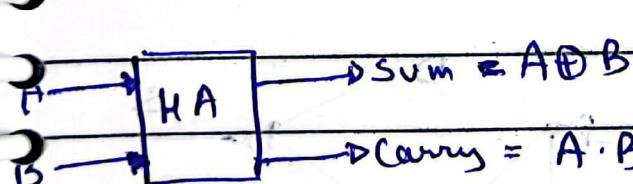
$$\text{Carry} = AB + BC + CA$$

• Using NAND = 9 gates

• Using NOR = 9 gates

• Using HA + OR = 2 HA & 1 OR

*) Half adder: - (Add. n. of two 1-bit numbers)

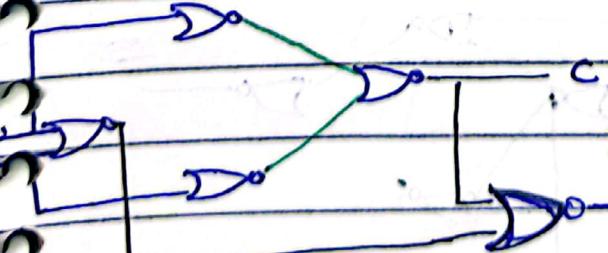
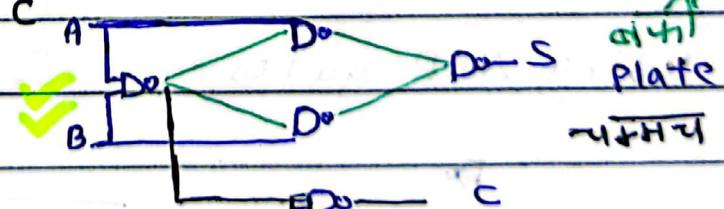


A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Using NAND

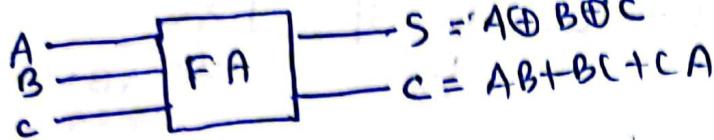


using NOR



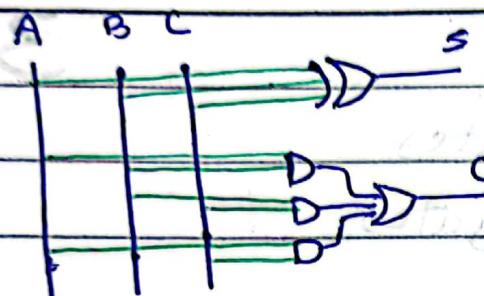
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Ammi

* Full adder: (Addition of three 1-bit numbers)

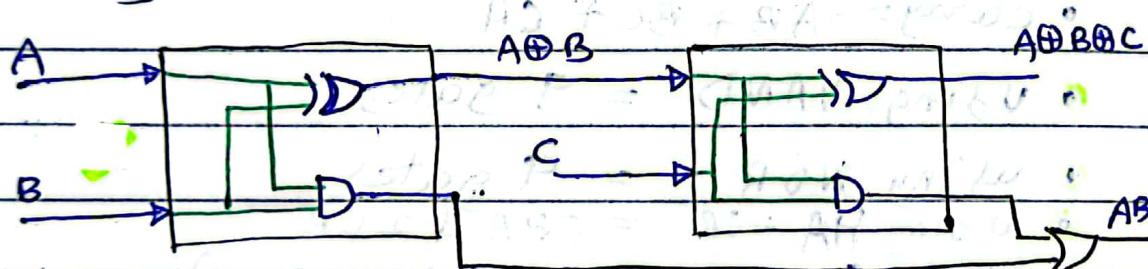


$$ABC \mid S \cdot C$$

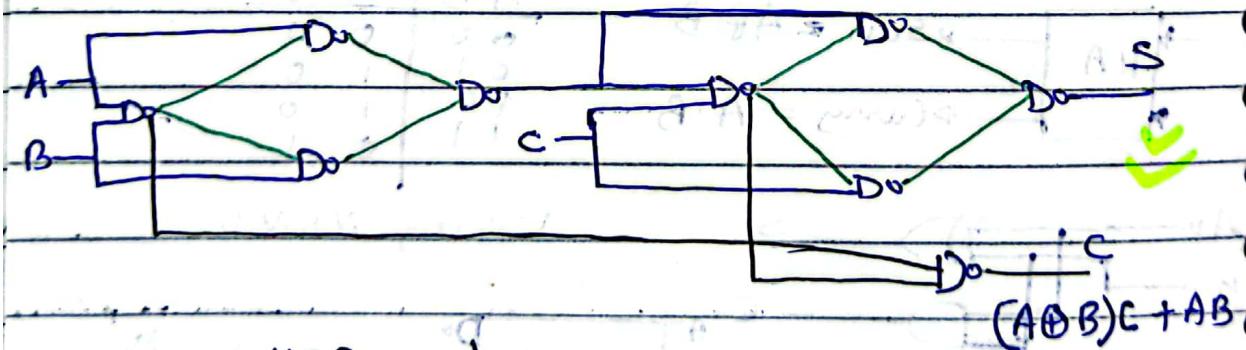
0 0 0	0 0
0 0 1	1 0
0 1 0	1 0
0 1 1	0 1
1 0 0	1 0
1 0 1	0 1
1 1 0	0 1
1 1 1	1 0



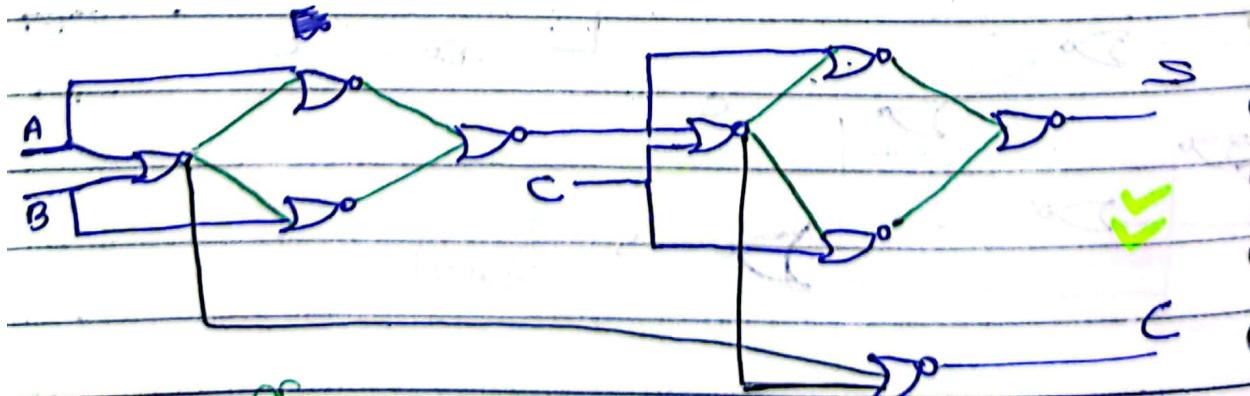
using HA's :-



using NAND gates:-



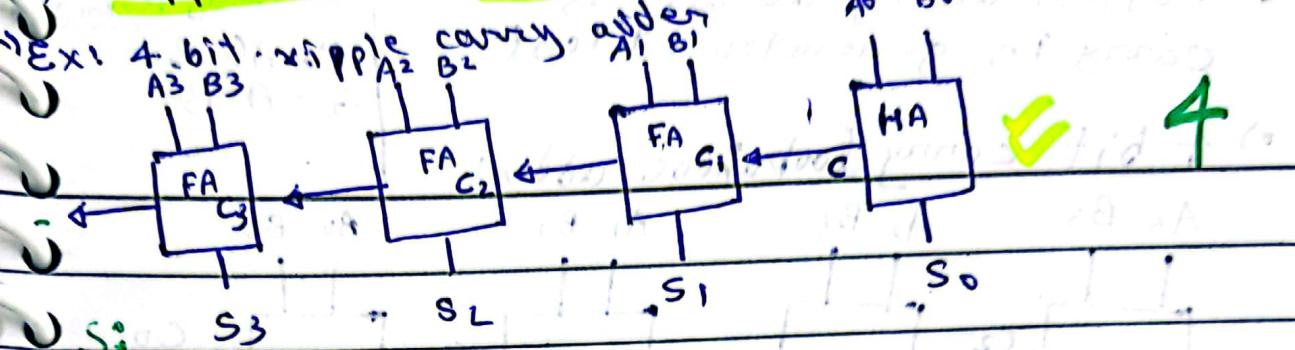
Using NOR gates



2 at 4nf
2 plate
1 - 1 & H-1

Ripple adder (Parallel adder) (Ripple carry adder)

"Ex: 4-bit ripple carry adder



To implement 4-bit parallel adder:-

$$\Rightarrow 3 \text{ FA} + 1 \text{ HA}$$

$$\Rightarrow 3 [2 \text{ HA} + 1 \text{ OR}] + 1 \text{ HA}$$

$$\Rightarrow 7 \text{ HA} + 3 \text{ OR} \quad (\text{Using only HA's})$$

$$\Rightarrow 7 [\text{XOR} + \text{AND}] + 3 \text{ OR}$$

$$\Rightarrow 7 \text{ XOR} + 7 \text{ AND} + 3 \text{ OR} \quad (\text{using only basic gates})$$

$$\Rightarrow 4 \text{ FA} \quad (\text{using only FA's})$$

To implement n-bit parallel adder:-

$$\Rightarrow n \text{ FA's}$$

$$\Rightarrow n-1 \text{ FA's} + 1 \text{ HA}$$

$$\Rightarrow (2n-1) \text{ HA's} + (n-1) \text{ OR}$$

$$\Rightarrow (2n-1) [\text{XOR} + \text{AND}] + (n-1) \text{ OR}$$

Delay :- for n-bit parallel adder

$$\text{Delay} = (n-1) \times \underbrace{t_{pd}}_{\text{of carry}} + \max \left[\underbrace{t_{pd}}_{\text{of sum}}, \underbrace{t_{pd}}_{\text{of carry}} \right]$$

[$t_{pd} = t_{pd, FA} + t_{pd, HA}$]

[$t_{pd, FA} = t_{pd, HA} = t_{pd, sum} = t_{pd, carry}$]

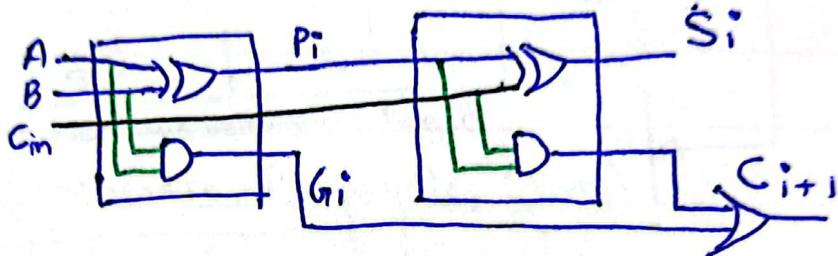
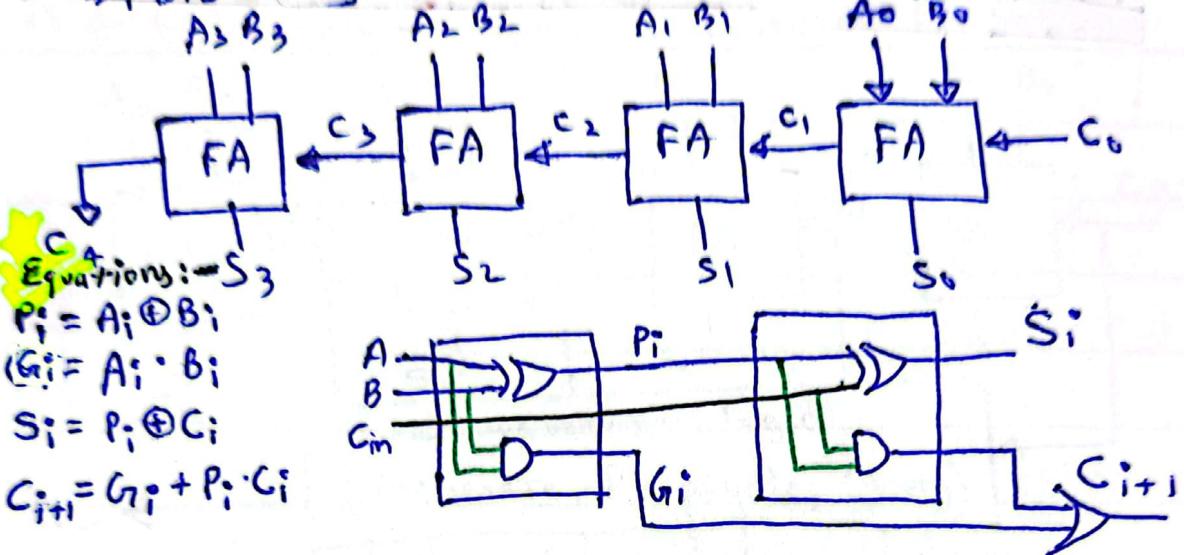
[$t_{pd, sum} = t_{pd, carry} = t_{pd, FA} + t_{pd, HA}$]

*> Carry lookahead adder:

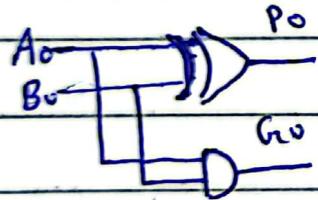
- > Fastest among all adders
- > carry is generated bit last
- > 4-bit carry lookahead adder :-

$$P = A \oplus B$$

$$G_i = A \cdot B$$



Level-1



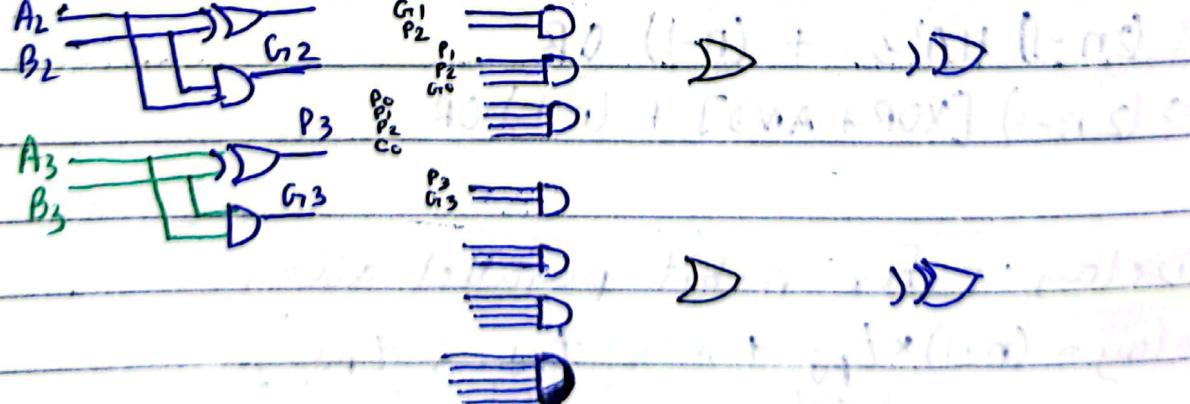
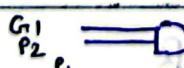
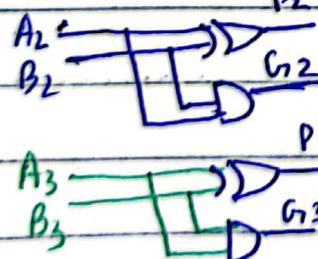
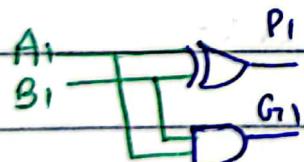
Level-2



Level-3



Level-4



4 [AND XOR] $[1+2+3+4]$ AND 4 [OR] 4 [XOR]

•> for n-bit carry lookahead adder:-

n [AND XOR] + $[1+2+\dots+n]$ AND + n [OR] + n [XOR] ✓

1) Delay :-

Level 1

$t_{pd} \text{ MAX(AND,XOR)}$

Level 2

$t_{pd} \text{ (AND)}$

Level 3

$t_{pd} \text{ (OR)}$

Level 4

$t_{pd} \text{ (XOR)}$

$$\text{UFO \& SVM, } D_{\text{sum}} = L_{v1} + L_{v2} + L_{v3} + L_{v4} \quad \checkmark 5$$

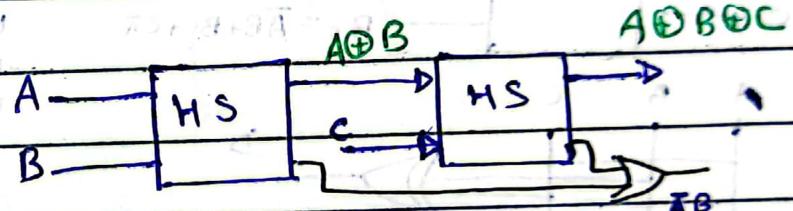
$$\text{UFO \& carry, } D_{\text{carry}} = L_{v1} + L_{v2} + L_{v3} \quad \checkmark$$

For entire addition = $\max [D_{\text{sum}}, D_{\text{carry}}]$

$$= D_{\text{sum}} \quad \checkmark$$

2) Subtractor:

Summary:



1) Half Subtractor

- $D_{\text{diff}} = A \oplus B$

- $B_{\text{borrow}} = \bar{A}B$

- Using NAND = 5 gates

- Using NOR = 5 gates

2) Full Subtractor

- $D_{\text{diff}} = A \oplus B \oplus C$

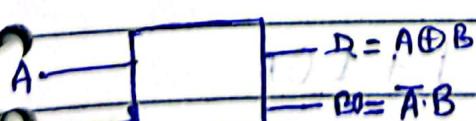
- $B_{\text{borrow}} = \bar{A}B + \bar{B}C + \bar{C}\bar{A}$

- Using NAND = 9 gates

- Using NOR = 9 gates

- Using HS =

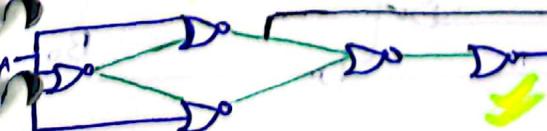
Half Subtractor:-



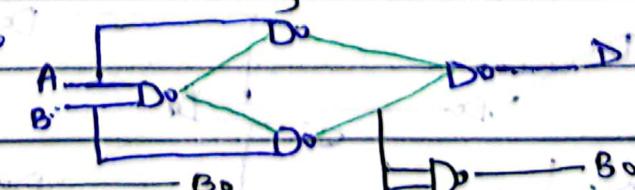
A	B	D	B_{O}
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0



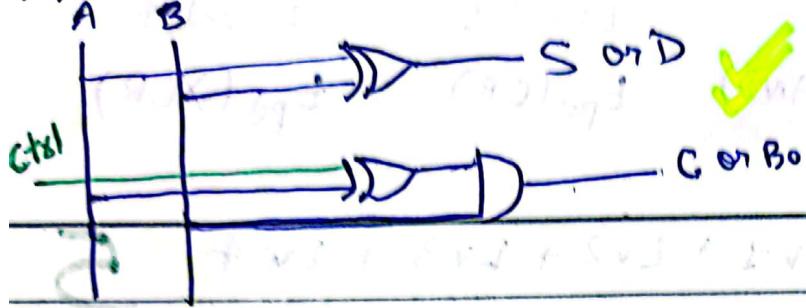
Using NOR



Using NAND



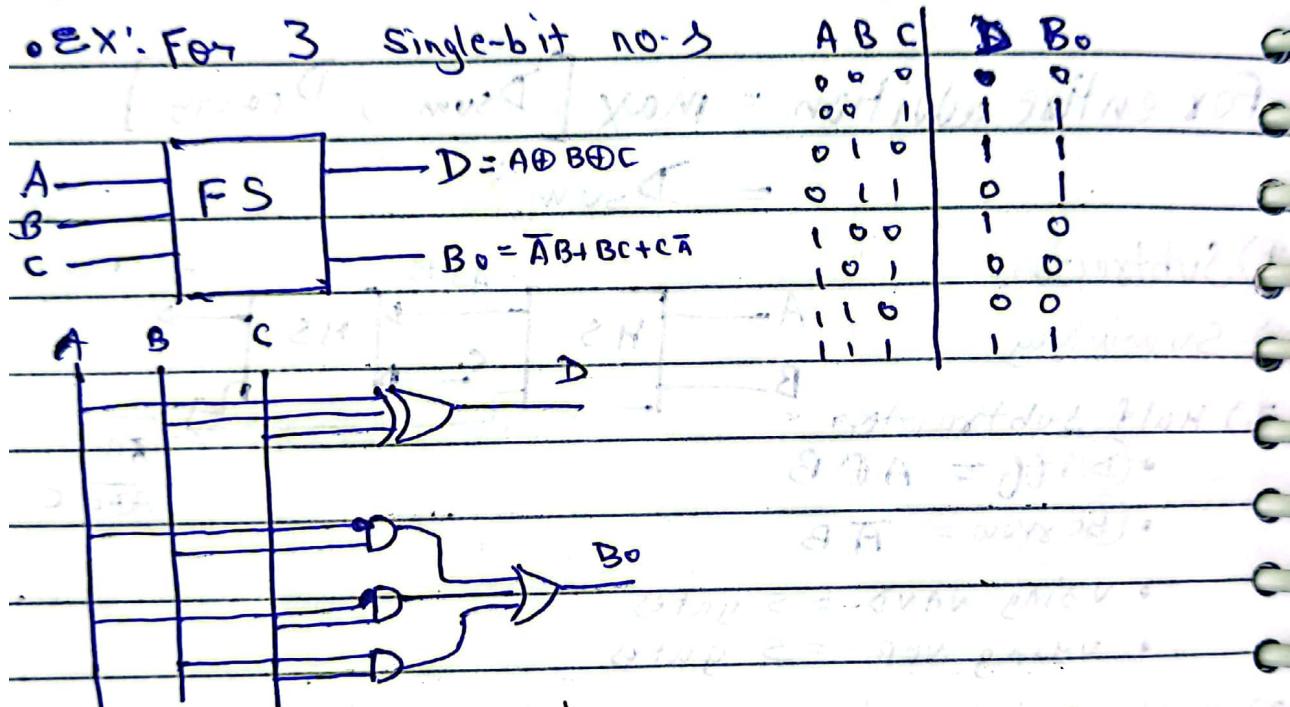
*> Half adder/Subtractor:-



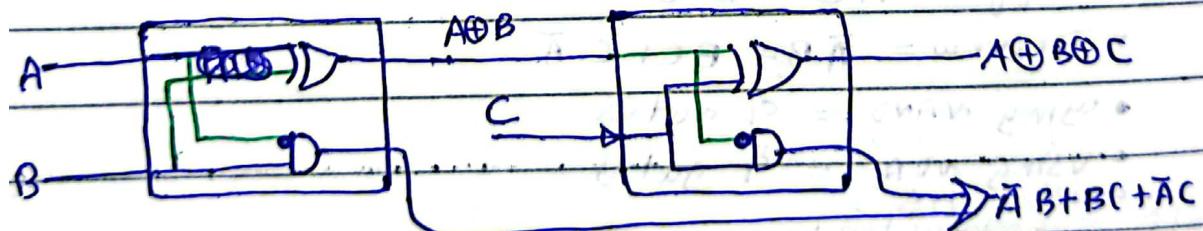
$$\text{ctrl} = 0 \Rightarrow \text{HA} \\ \text{ctrl} = 1 \Rightarrow \text{HS}$$

*> Full Subtractor:

Ex: For 3 single-bit no's



Using half subtractors

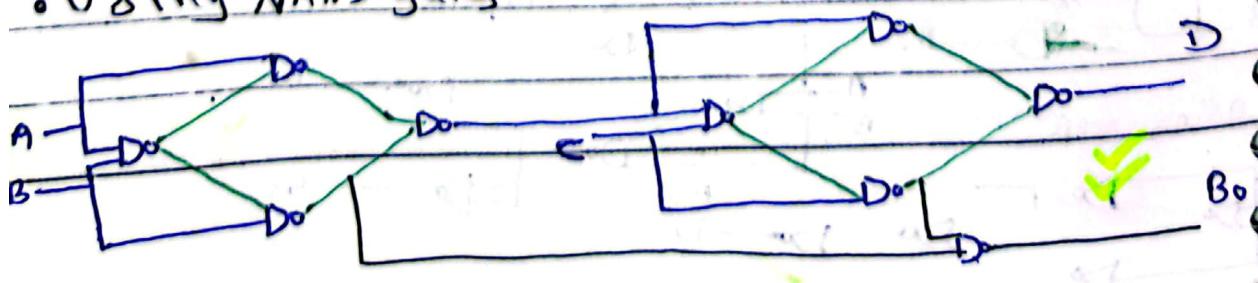


$\star \text{FS} = 2 \text{HS} + 1 \text{OR}$

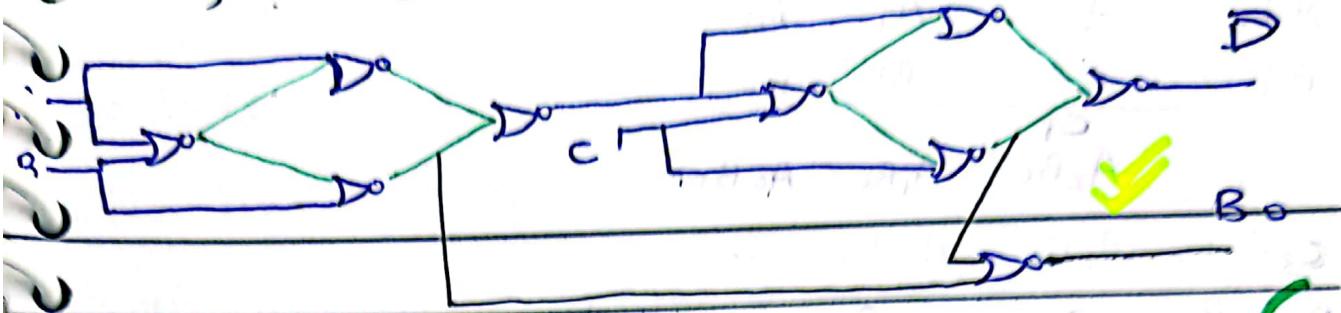
$$= 2 [\text{XOR} + \text{AND} + \text{NOT}] + 1 \text{OR}$$

$$= 2 \text{XOR} + 2 \text{AND} + 2 \text{NOT} + 1 \text{OR}$$

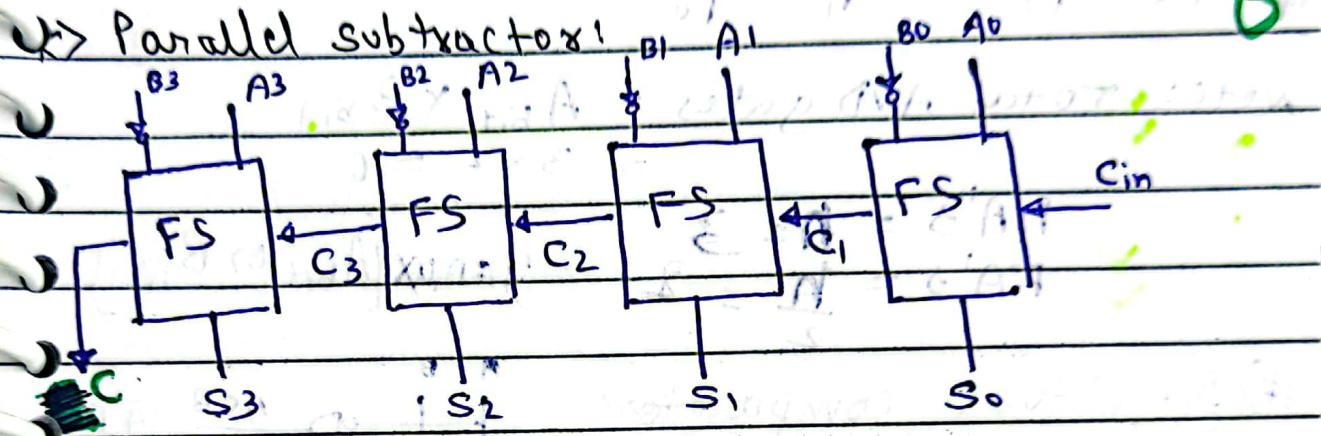
Using NAND gates



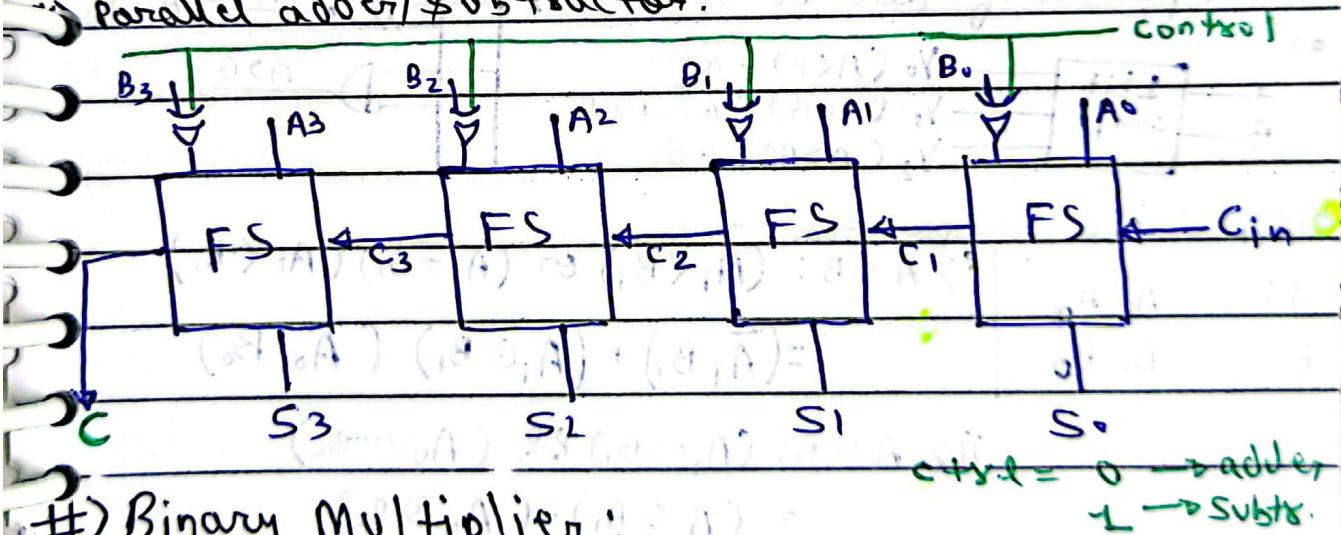
Using NOR gate



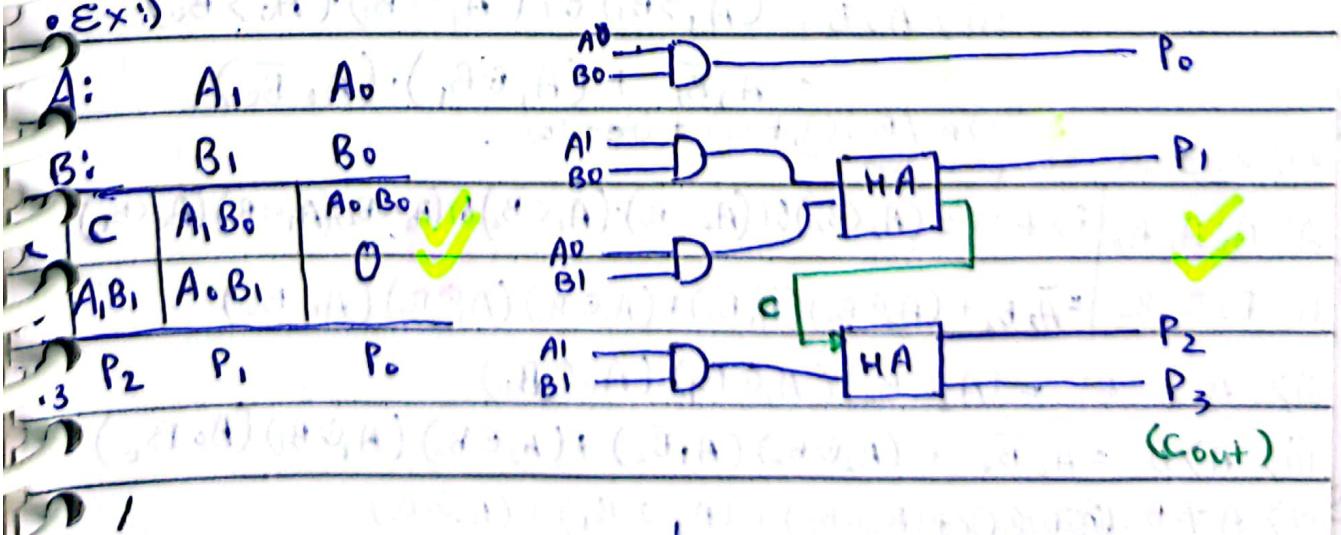
→ Parallel subtractor



Parallel adder/subtractor:



→ Binary Multiplier:



• EX:

A:	A_2	A_1	A_0
B:		B_1	B_0
	C_1		
	$A_2 B_0$	$A_1 B_0$	$A_0 B_0$
C_2	$A_2 B_1$	$A_1 B_1$	$A_0 B_1$
	0		
P_4	P_3	P_2	P_1
			P_0

Note: Total AND gates = $A_{bit} \times B_{bit}$.
 $= 3 \times 2 = 6$

?

$H A' \delta = A = 3$

$F.A' \delta = \frac{A}{2} = 2$

$n = \max\{A_{bit}, B_{bit}\}$

#) Magnitude Comparator:

a) Comparison of two no.s

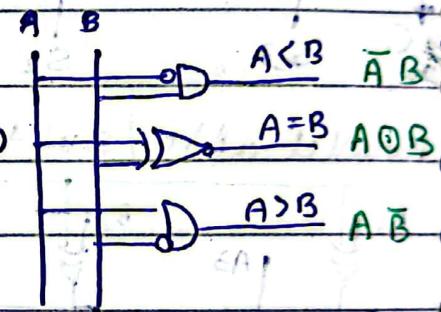
b)

A ————— $\boxed{1 \text{ bit comp.}}$ ————— B

$$Y_0 (A < B) = \bar{A} B$$

$$Y_1 (A = B) = \bar{A} \bar{B} + A B$$

$$Y_2 (A > B) = A \bar{B}$$



c) Ex: 2 bit comparators :-

A: A_1, A_0 | i) $A < B : (A_1 < B_1) \text{ or } (A_1 = B_1) \cdot (A_0 < B_0)$

B: B_1, B_0 | $= (\bar{A}_1 B_1) + (A_1 \oplus B_1) \cdot (\bar{A}_0 B_0)$

ii) $A = B : (A_1 = B_1) \& (A_0 = B_0)$

$= (A_1 \oplus B_1) \cdot (A_0 \oplus B_0)$

iii) $A > B : (A_1 > B_1) \text{ or } (A_1 = B_1) \cdot (A_0 > B_0)$

$= A_1 \bar{B}_1 + (A_1 \oplus B_1) \cdot (A_0 \bar{B}_0)$

d) Ex: 3 bit comparator :-

A: A_2, A_1, A_0 | i) $A < B : (A_2 < B_2) \text{ or } (A_2 = B_2) \cdot (A_1 < B_1) \text{ or } (A_2 = B_2) \cdot (A_1 = B_1) \cdot (A_0 < B_0)$

B: B_2, B_1, B_0 | $= \bar{A}_2 B_2 + (A_2 \oplus B_2) (\bar{A}_1 B_2) + (A_2 \oplus B_2) (A_1 \oplus B_1) (\bar{A}_0 B_2)$

ii) $A = B : (A_2 \oplus B_2) (A_1 \oplus B_1) (A_0 \oplus B_0)$

iii) $A > B : = A_2 \bar{B}_2 + (A_2 \oplus B_2) (A_1 \bar{B}_2) + (A_2 \oplus B_2) (A_1 \oplus B_1) (A_0 \bar{B}_2)$

iv) $A \neq B : (A_2 \oplus B_2) (A_1 \oplus B_1) (A_0 \oplus B_0)$

1) For 3 bit :-

A
(0 to 7)
B
(0 to 7)

A < B has $\frac{2^n - 2^n}{2} = 28$ combinations

A == B has $\frac{2^n}{2} = 8$ combinations

A > B has $\frac{2^n - 2^n}{2} = 28$ combinations

To construct n-bit comparator using 1-bit comparators

1-bit comparators = n

AND gates = 2^{n-1}

OR gates = 2

3) Counters

Synchronous
Ripple (Asynchronous) counts from 0 to $2^n - 1$

n-bit binary counter \Rightarrow n-flip flop \Rightarrow 0 to $2^n - 1$

Synchronous Counters

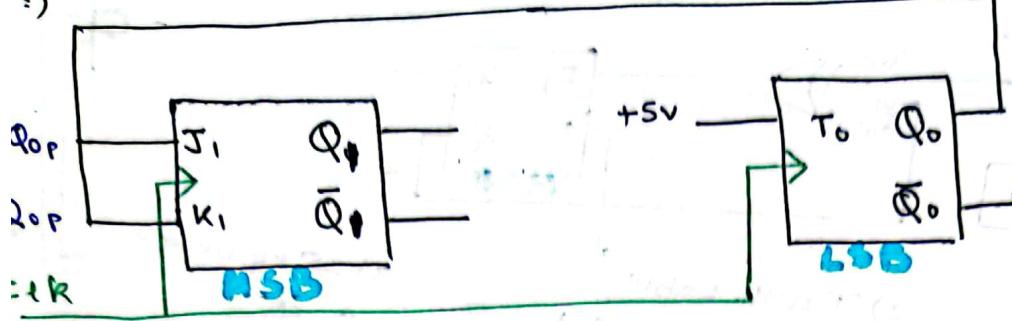
Q:

Note:- • The delay formulas may be incorrect when

FA's are implemented using HA's.

• In that case, draw logic diagram & calculate delay manually.

7



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1) characteristic eqn :-

$$JK: Q_{n+1} = J \bar{Q}_n + \bar{K} Q_n$$

$$T: Q_{n+1} = T \oplus Q_n$$

$$Q_{DN} = 1 \oplus Q_{op} = \bar{Q}_{op}$$

$$Q_{IN} = Q_{op} Q_{ip} + \bar{Q}_{op} Q_{ip} = Q_{op} \oplus Q_{ip}$$

2 flipflops

$$\Rightarrow 2^2 = 4$$

\Rightarrow mod 4 counter

2) Truth table:-

PS's		NS's	
Q _{ip}	Q _{op}	Q _{IN}	Q _{DN}
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

mod 4 counter

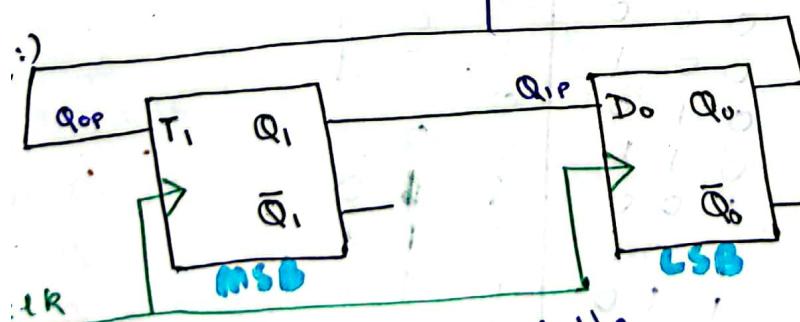
3) Sequence

$$\begin{matrix} Q_1 & Q_0 \\ 0 & 0 \end{matrix} \rightarrow \begin{matrix} 0 & 1 \\ 1 & 1 \end{matrix}$$

$$\begin{matrix} 1 & 1 \\ 1 & 0 \end{matrix} \leftarrow \begin{matrix} 0 & 1 \\ 0 & 0 \end{matrix}$$

$$\begin{matrix} 0 & 1 \\ 0 & 0 \end{matrix} \rightarrow \begin{matrix} 1 & 0 \\ 1 & 1 \end{matrix}$$

$$\begin{matrix} 1 & 0 \\ 1 & 1 \end{matrix} \leftarrow \begin{matrix} 0 & 0 \\ 0 & 1 \end{matrix}$$



char. eqn :-

$$Q_{n+1} = T \oplus Q_n$$

$$\therefore Q_{n+1} = D$$

$$Q_{DN} = Q_{ip}$$

$$Q_{IN} = Q_{op} \oplus Q_{ip}$$

2) Truth table

PS's		NS's	
Q _{ip}	Q _{op}	Q _{IN}	Q _{DN}
0	0	0	0
0	1	1	0
1	0	1	1
1	1	0	0

3) Sequence

$$\begin{matrix} Q_1 & Q_0 \\ 0 & 0 \end{matrix} \rightarrow \begin{matrix} 0 & 1 \\ 1 & 1 \end{matrix}$$

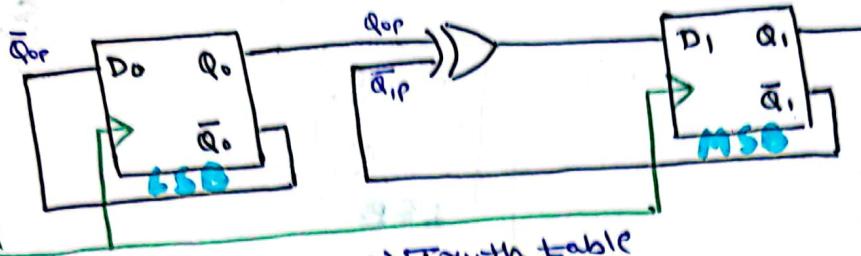
$$\begin{matrix} 0 & 1 \\ 0 & 0 \end{matrix} \rightarrow \begin{matrix} 1 & 0 \\ 1 & 1 \end{matrix}$$

$$\begin{matrix} 1 & 0 \\ 1 & 1 \end{matrix} \rightarrow \begin{matrix} 0 & 0 \\ 0 & 1 \end{matrix}$$

$$\begin{matrix} 0 & 0 \\ 0 & 1 \end{matrix} \leftarrow \begin{matrix} 1 & 0 \\ 1 & 1 \end{matrix}$$

Q1) Each state (in sequence) is stated as $Q_0 Q_1$.

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1) char. eqn:-

$$D: Q_{n+1} = D$$

$$Q_{0N} = \bar{Q}_{0P}$$

$$Q_{1N} = Q_{0P} \oplus \bar{Q}_{1P}$$

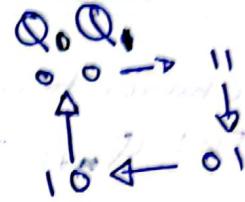
$$= Q_{0P} \cdot Q_{1P} + \bar{Q}_{0P} \cdot \bar{Q}_{1P}$$

$$= Q_{0P} \cdot Q_{1P}$$

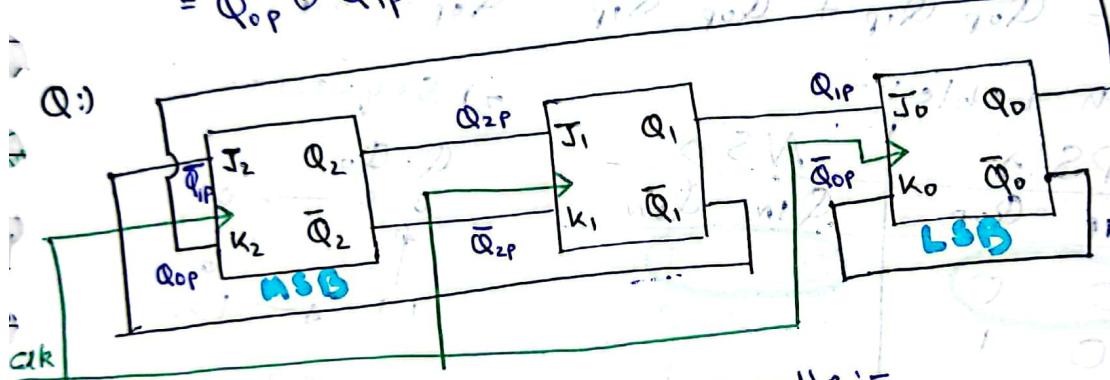
2) Truth table

PS's		NS's	
Q_{1P}	Q_{0P}	Q_{1N}	Q_{0N}
0	0	1	1
0	1	0	0
1	0	0	1
1	1	1	0

3) Sequence



Q2)



1) char. eqn:-

$$\text{JK: } Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

$$Q_{0N} = Q_{1P}\bar{Q}_{0P} + \bar{Q}_{0P} \cdot Q_{0P}$$

$$= Q_{1P}\bar{Q}_{0P} + Q_{0P}$$

$$= Q_{1P} + Q_{0P}$$

$$Q_{1N} = Q_{2P}\bar{Q}_{1P} + Q_{2P} \cdot Q_{1P}$$

$$= Q_{2P}$$

$$Q_{2N} = \bar{Q}_{1P}\bar{Q}_{2P} + \bar{Q}_{0P}Q_{2P}$$

if any sum term = 1

i) if $\bar{Q}_{1P}\bar{Q}_{2P} = 1$

$$\Rightarrow Q_{1P} = 0, Q_{2P} = 0$$

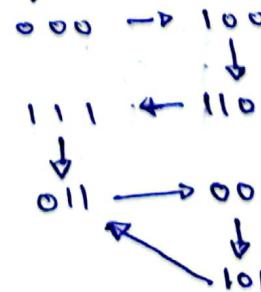
ii) if $\bar{Q}_{0P} \cdot Q_{2P} = 1$

$$\Rightarrow Q_{0P} = 0, Q_{2P} = 1$$

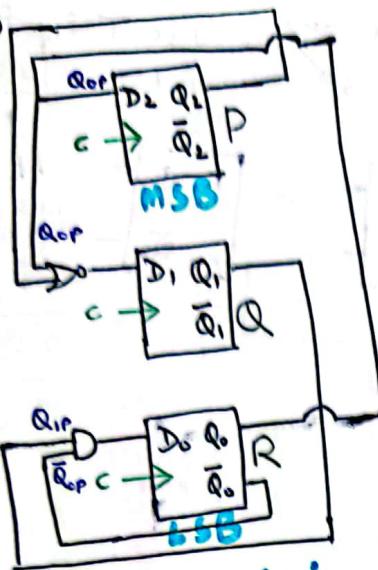
2) Truth table:-

PS's			NS's		
Q_{2P}	Q_{1P}	Q_{0P}	Q_{2N}	Q_{1N}	Q_{0N}
0	0	0	1	0	0
0	0	1	1	0	1
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1

3) sequence:-



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PS			NS		
Q_{2P}	Q_{1P}	Q_{0P}	Q_{2N}	Q_{1N}	Q_{0N}
0	0	0	0	1	0
0	0	1	1	0	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

At an instant PQR have a value 010

Sequence:-

$$D: Q_{n+1} = D$$

$$Q_{0N} = \overline{Q_{1P} \cdot \overline{Q_{0P}}}$$

↓ if $Q_{0P} = 0, Q_{1P} = 1$

$$Q_{1N} = \overline{Q_{0P} + Q_{2P}}$$

$$= \overline{Q_{0P} \cdot \overline{Q_{2P}}}$$

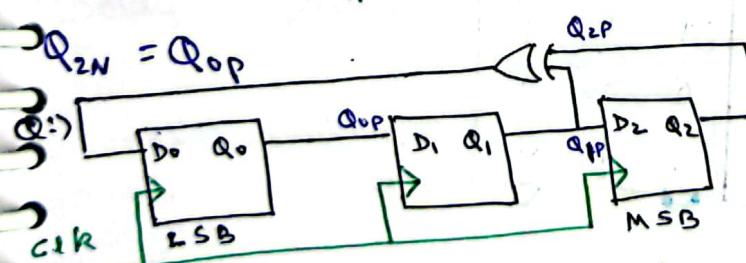
↓ if $Q_{0P} = 0, Q_{2P} = 0$

$$\begin{matrix} Q_2 & Q_1 & Q_0 \\ 0 & 0 & 0 \end{matrix} \rightarrow 010$$

↑ ↓

$$100 \leftarrow 011$$

initial state: $Q_2 Q_1 Q_0$
0 0 1



$$D: Q_{n+1} = D$$

$$Q_{0N} = Q_{2P} \oplus Q_{1P}$$

$$Q_{1N} = Q_{0P}$$

$$Q_{2N} = Q_{1P}$$

PS			NS		
Q_{2P}	Q_{1P}	Q_{0P}	Q_{2N}	Q_{1N}	Q_{0N}
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	1	0	1	1
1	1	0	1	0	0
1	1	1	1	1	0

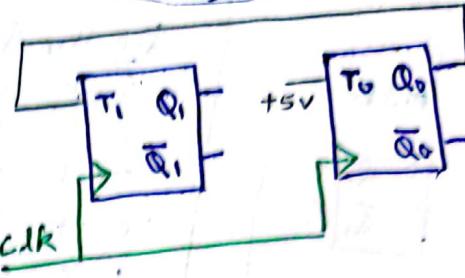
$$\begin{matrix} Q_2 & Q_1 & Q_0 \\ 0 & 0 & 1 \end{matrix} \rightarrow 010$$

↑ ↓

$$101 \leftarrow 110 \leftarrow 011$$

* Sequence is counter of 1111
 Q: Design synchronous counter for seq: 0 → 1 → 2 ; Use T flip-flop
 R 3 → mod 4

PS		NS			T	
Q _{1P}	Q _{0P}	Q _{2N}	Q _{1N}	Q _{0N}	T ₁	T ₀
0	0	0	0	0	0	1
0	1	1	0	0	1	0
1	0	0	1	0	0	1
1	1	1	1	1	0	0



Mod-4 \Rightarrow 2 FF's needed



$T_1 = Q_{0P}$ | $T_0 : T_0 = 1$
 $T_1 \rightarrow 3$; use D flip-flops

Q: Seq: 0 → 2 → 4
 $6 \leftarrow 7 \leftarrow 5$

Sequence \Rightarrow mod 8 \Rightarrow 3 FF's

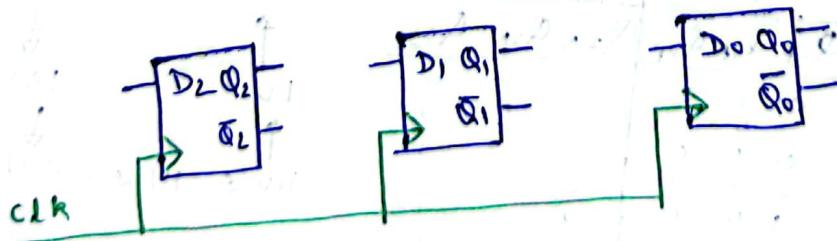
PS		NS			D			
Q _{2P}	Q _{1P}	Q _{0P}	Q _{2N}	Q _{1N}	Q _{0N}	D ₂	D ₁	D ₀
0	0	0	0	1	0	0	1	0
0	0	1	0	1	1	0	1	1
0	1	0	1	0	0	1	0	0
0	1	1	0	0	0	1	0	1
1	0	0	1	0	1	1	0	1
1	0	1	1	1	1	0	0	0
1	1	0	0	0	0	0	0	0
1	1	1	1	0	1	1	1	0

Q _{2P}	Q _{1P}	Q _{0P}	Q _{2N}	Q _{1N}	Q _{0N}
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	1	0	1

$$D_2 = \bar{Q}_{2P} Q_{1P} \bar{Q}_{0P} + Q_{2P} Q_{0P}$$

$$+ \bar{Q}_{1P} Q_{2P}$$

Proceed like previous



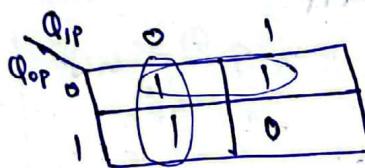
- Q1) 2 bit saturating up-counter.
- Synchronous.
- Use T FF's
- Seq: $0 \rightarrow 1 \rightarrow 2 \rightarrow 3$; 2 FF's there

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PS	NS		T			
	Q_{1P}	Q_{0P}	Q_{1N}	Q_{0N}	T_1	T_0
	0	0	0	1	0	1
	0	1	1	0	0	1
	1	0	1	1	0	0
	1	1	1	1	0	1

$$T_1 = \bar{Q}_{1P} Q_{0P}$$

$$T_0 = \bar{Q}_{1P} + \bar{Q}_{0P}$$



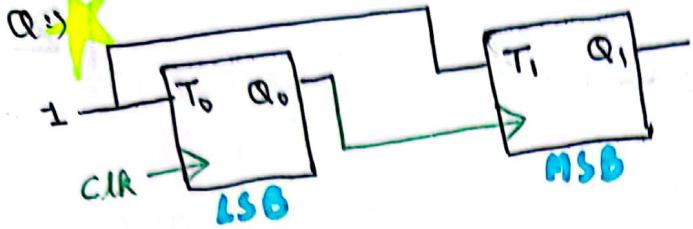
*> Synchronous counter

- All FF's triggered with same clock.
- Faster
- Delay = $T_{FF} + T_{cc}$; T_{FF} = flip flop delay
- T_{cc} = comb. circuit delay
- Parallel counter
- Operate in any desired count sequence
- Ex: Ring counter
Johnson "

Asynchronous (Ripple) counter

- Different FF's triggered with different clock.
- Slower
- Delay = $n \times T_{FF} + T_{cc}$
- Serial counter
- Operate only in fixed count sequence (up / down)
- Ex: Ripple up counter
Ripple down "

* Asynchronous counters:-



i.e. triggering

i) Char. eq'n :-

$$T = Q_{n+1} = T \oplus Q_n$$

$$Q_{0N} = 1 \oplus Q_{0P} = \bar{Q}_{0P}$$

ii) For Q_{IN} observe FF-0 :-

Toggle mode ($Q_0: 0 \rightarrow 1$)

Latch mode (Memory)

$$Q_{n+1} = T \oplus Q_n$$

$$Q_{1N} = 1 \oplus Q_{1P} \\ = \bar{Q}_{1P}$$

$$Q_{IN} = Q_{1P}$$

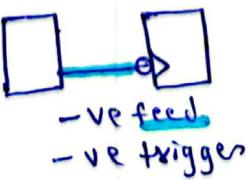
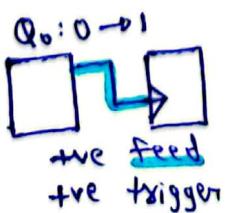


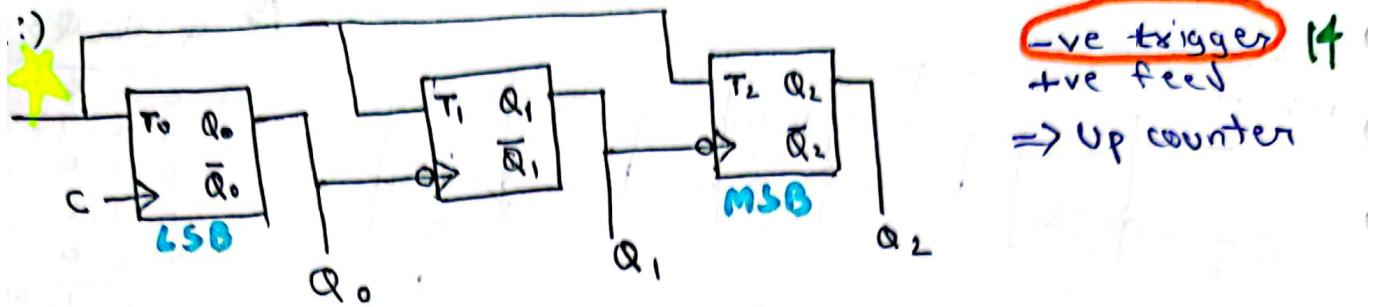
iii) State diagram NS

P	S	Q_{1P}	Q_{0P}	Q_{1N}	Q_{0N}
0	0	0	0	1	1
0	1	1	0	0	1
1	0	0	1	1	0

iv) Sequence:

Note:	+ve Feedback	-ve Feedback
+ve edge trigger	Down Counter	Up Counter
-ve edge trigger	Up Counter	Down Counter





$$T: Q_{n+1} = T \oplus Q_n$$

$$\begin{aligned} Q_{0N} &= 1 \oplus Q_{0P} \\ &= \bar{Q}_{0P} \end{aligned}$$

NOW, for $\times FF - 1$

$$TM(Q_0: 1 \rightarrow 0) \quad LM(\text{else})$$

$$\begin{aligned} Q_{1N} &= 1 \oplus Q_{1P} \\ &= \bar{Q}_{1P} \end{aligned}$$

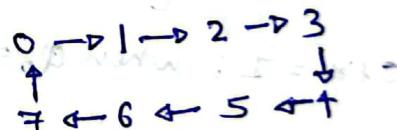
NOW,

		PS	NS	
		Q_{2N}	Q_{1N}	Q_{0N}
		0	0	1
0	0	0	1	0
0	0	0	1	0
0	1	0	1	0
0	1	0	1	0
0	1	0	1	0
1	0	0	1	0
1	0	0	1	0
1	0	0	1	0
1	1	0	1	0
1	1	0	1	0
1	1	0	1	0
1	1	0	1	0
1	1	0	1	0
1	1	0	1	0
1	1	0	1	0
1	1	0	1	0

for ff - 2

$$\begin{array}{c|c} TM(Q_1: 1 \rightarrow 0) & LM(\text{else}) \\ \hline Q_{2N} = 1 \oplus Q_{2P} & Q_{2N} = Q_{2P} \\ = \bar{Q}_{2P} & \end{array}$$

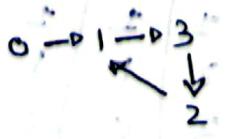
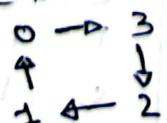
now,
sequence:-



• Self starting counter \Rightarrow Sequence = connected graph
(irrespective of initial state, counter provides counting sequence)

• Free running counter \Rightarrow Sequence = perfect cycle
(counter is maintaining all possible states)
In counting sequence

• Ex:



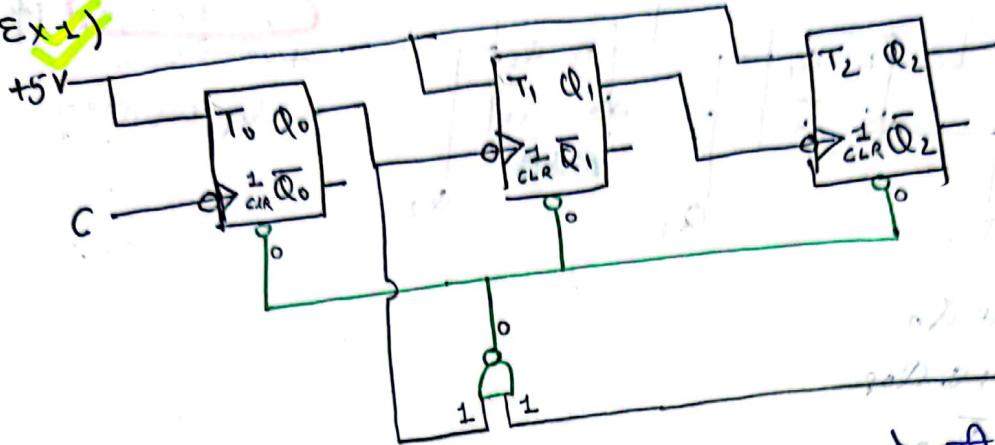
SSV FRV SSV FRV

•



*> Restricted mod counter

Ex-1)



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$Q_2 Q_1 Q_0$

0	0	0
0	0	1
0	1	0
0	1	1
1	0	0

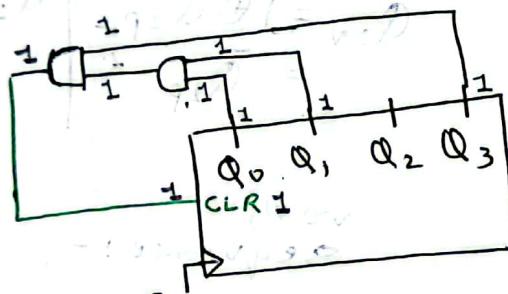
101 → C will
reset here

$0 \rightarrow 1 \rightarrow C$
 $C \leftarrow 3^{\text{rd}}$
 $\Rightarrow \text{mod } 5 \text{ counter}$

ची देरतो की सारी CLR pins 1 करे एवं तो होगा 101

B.C. तक counter reset हो जायेगा

Ex-2)



$C_{180} = 1$; when $Q_0 = 1 \& Q_1 = 1 \& Q_2 = 1$

$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5$
 $10 \leftarrow 9 \leftarrow 8 \leftarrow 7 \leftarrow 6$

mod-11 upcounter

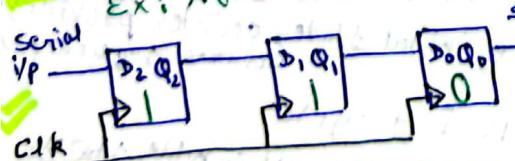
$Q_3 Q_2 Q_1 Q_0$

0	0	0	0
0	0	0	1
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

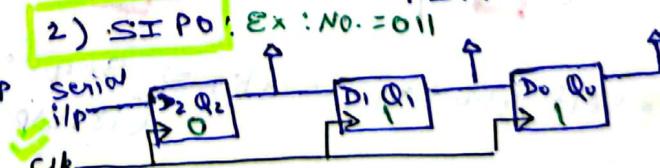
*> Registers:
• Storage device design using FF's (usually D)
• Shift register types / modes

1) SISO

Ex: No. = 110

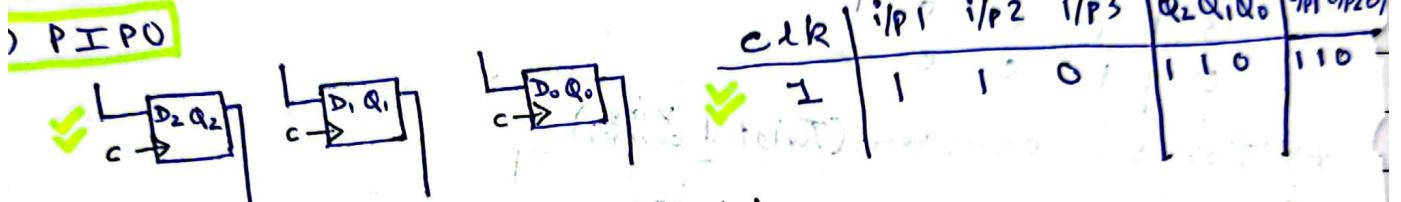
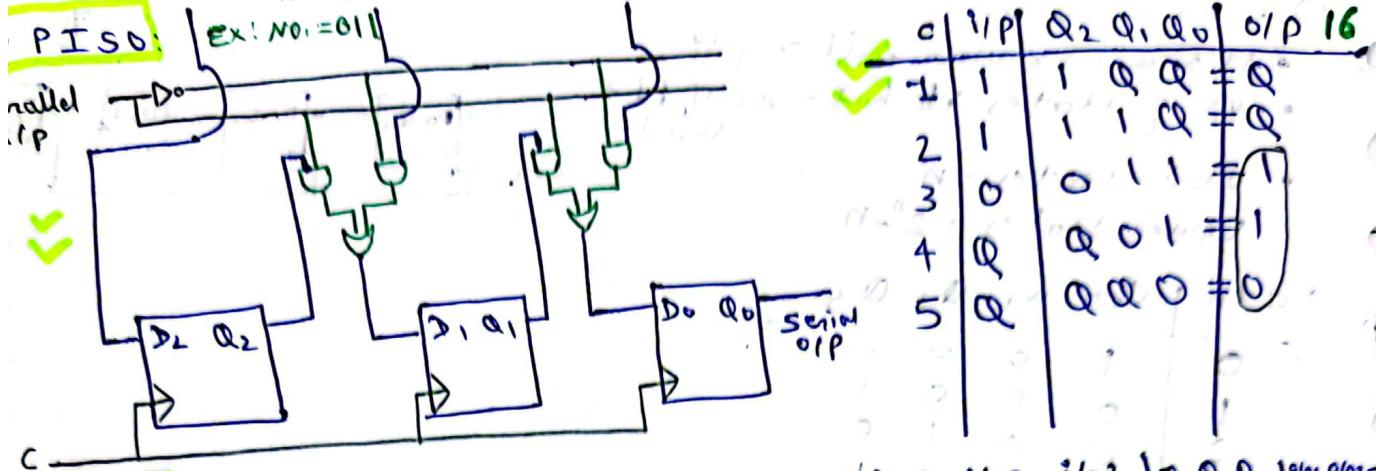


2) SIPO



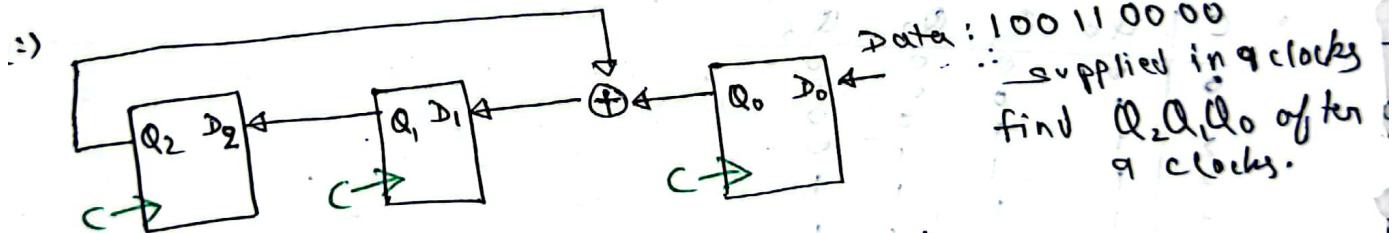
clk	i/p	Q_2	Q_1	Q_0	o/p
1	0	0	0	0	0
2	1	0	0	0	0
3	-1	1	0	0	0
4	0	1	1	0	0
5	0	0	1	1	1
6	0	0	0	1	1

clk	i/p	Q_2	Q_1	Q_0	o/p ₁	o/p ₂	o/p ₃
1	1	1	1	0	1	0	0
2	1	1	1	1	1	0	0
3	0	0	1	1	0	1	1



Note:

	No. of clock (Gxitc)	No. of clock (Xeon)	Total clock
SISO	n	n-1	2n-1
SIPSO	n	0	n
PISO	1	n-1	2
PIPO	1	0	1



c	Q _{2P}	Q _{1P}	Q _{0P}	D	Q _{2N}	Q _{1N}	Q _{0N}
-1	0	0	0	1	0	0	1
2	0	0	1	0	0	1	0
3	0	1	0	0	0	0	0
4	1	0	1	1	1	1	1
5	0	1	1	0	1	0	0
6	1	0	0	0	0	1	0
7	1	0	0	0	1	0	0
8	0	1	0	0	0	1	0
9	1	0	0	0	0	1	0

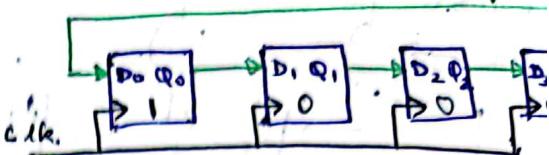
$$Q_{0N} = \text{Data}$$

$$Q_{1N} = Q_{2P} \oplus Q_{0P}$$

$$Q_{2N} = Q_{1P}$$

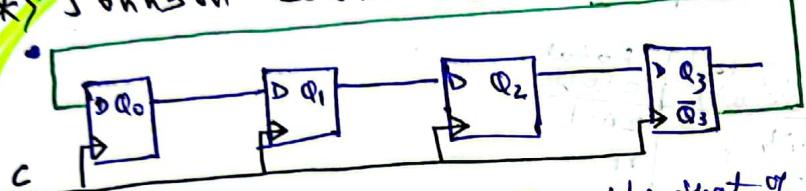
* Ring counter:

- It's a circular shift register
- No. of states it has = No. of FF's used
- Used states = n
- Unused states = $2^n - n$



C_{LR}	Q_0	Q_1	Q_2	Q_3
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
0	1	0	0	0

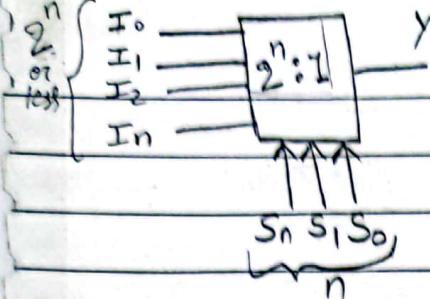
* Johnson counter: (Twisted ring counter)



- Used states = $2n$ (Double that of ring counter)
- Unused states = $2^n - 2n$

C	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
0	0	0	0	0

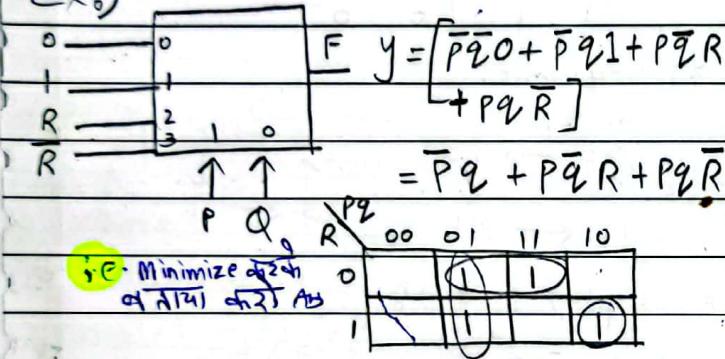
Multiplexer (MUX)



$$2:1) \quad y = \bar{S}_0 I_0 + S_0 I_1$$

$$4:1) \quad y = E(\bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3)$$

Ex:

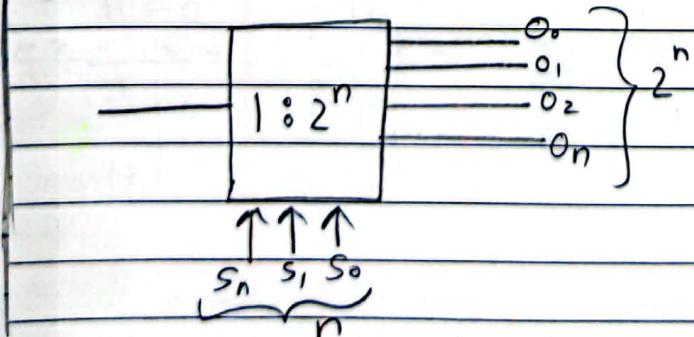


Ex: 128x1 from 4x1

$$\frac{2^1}{4} \quad \frac{2^2}{4} \quad \frac{2^3}{4} \quad \frac{2^4}{4} \quad 32$$

$$1 + 2 + 8 + 32 = 43 \text{ (4x1 mux)}$$

De-Multiplexer (DeMux)

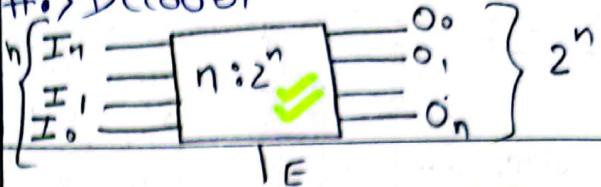


$$1:4) \quad \begin{array}{c|c} & S_1, S_0 \\ \hline O_0 & 0, 0, 0, 0 \\ O_1 & 0, 0, 0, 1 \\ O_2 & 0, 1, 0, 0 \\ O_3 & 1, 0, 0, 0 \end{array}$$

$$O_0 = \bar{S}_1 \bar{S}_0 I$$

$$O_1 = \bar{S}_1 \bar{S}_0 I$$

Decoder



$$2:1) \quad \begin{array}{c|c} & I_1, I_0 \\ \hline O_0 & 0, 0, 0, 0 \\ O_1 & 0, 0, 0, 1 \\ O_2 & 0, 1, 0, 0 \\ O_3 & 1, 0, 0, 0 \end{array}$$

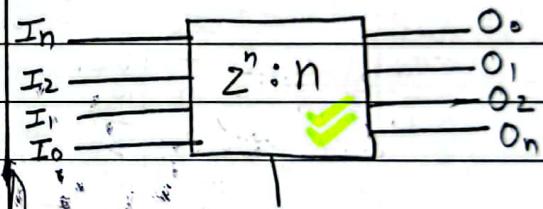
Active high decoder = AND-OR
,, Low " = NAND-NAND

Ex: 7:128 from 3:8

$$\frac{2^1}{8} \quad \frac{2^2}{8} \quad \frac{2^3}{8} \quad 16$$

$$1 + 2 + 16 = 19$$

Encoder



$$4:2) \quad \begin{array}{c|c} & I_3, I_2, I_1, I_0 \\ \hline O_0 & 0, 0, 0, 1 \\ O_1 & 0, 0, 1, 0 \\ O_2 & 0, 1, 0, 0 \\ O_3 & 1, 0, 0, 0 \end{array}$$

$$O_0 = (I_3 \oplus I_1) \cdot \bar{I}_2 \cdot \bar{I}_0$$

$$O_1 = (I_3 \oplus I_2) \cdot \bar{I}_1 \cdot \bar{I}_0$$

Priority encoder) $I_3 > I_2 > I_1 > I_0$

$$O_0 = I_3 + \bar{I}_2 I_1 \quad \begin{array}{c|c} I_3 & I_2 \\ \hline 0 & 0, 0 \\ 1 & 0, 1 \end{array} \quad \begin{array}{c|c} I_2 & I_1 \\ \hline 0 & 0, 0 \\ 1 & 0, 1 \end{array} \quad \begin{array}{c|c} I_1 & I_0 \\ \hline 0 & 0, 0 \\ 1 & 0, 1 \end{array} \quad \begin{array}{c|c} I_0 & O_0 \\ \hline 0 & 0 \\ 1 & 1 \end{array}$$

$$O_1 = I_3 + I_2 \quad \begin{array}{c|c} I_3 & I_2 \\ \hline 0 & 0, 0 \\ 1 & 0, 1 \end{array} \quad \begin{array}{c|c} I_2 & O_1 \\ \hline 0 & 0 \\ 1 & 1 \end{array}$$

$$O_2 = I_3 \quad \begin{array}{c|c} I_3 & O_2 \\ \hline 0 & 0 \\ 1 & 1 \end{array}$$

$$O_3 = I_2 \quad \begin{array}{c|c} I_2 & O_3 \\ \hline 0 & 0 \\ 1 & 1 \end{array}$$

Sequential circuits (combinational circuit + memory)

$$1:4) \quad \begin{array}{c|c} & S_1, S_0 \\ \hline O_0 & 0, 0, 0, 0 \\ O_1 & 0, 0, 0, 1 \\ O_2 & 0, 1, 0, 0 \\ O_3 & 1, 0, 0, 0 \end{array}$$

$$O_0 = \bar{S}_1 \bar{S}_0 I$$

$$O_1 = \bar{S}_1 S_0 I$$

1) SR:



Eq. n:

$$Q_{n+1} = S + \bar{R} \cdot Q_n$$

Truth table:

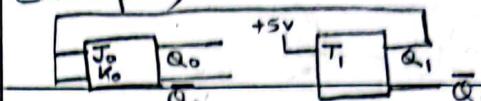
S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	0	0
0	1	0	1

Fx^n table:

S	R	Q_n	Q_{n+1}
0	0	0	0
0	1	0	1
1	0	1	1

Counters:

Example) Derive transition sequence



1) Equations:

$$T\bar{Q}_n \cdot Q_{n+1} = T\bar{Q}_n + \bar{T}Q_n$$

$$T \cdot Q_{n+1} = T \oplus Q_n$$

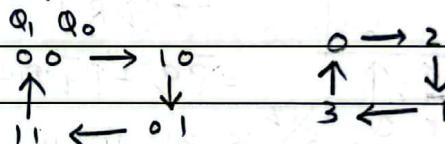
$$Q_{n+1} = Q_{IP} \cdot \bar{Q}_{OP} + \bar{Q}_{IP} \cdot Q_{OP} = Q_{IP} \oplus Q_{OP}$$

$$Q_{IN} = 1 \oplus Q_{IP} = \bar{Q}_{IP}$$

2) Truth table

Present		Next	
Q_{IP}	Q_{OP}	Q_{IN}	Q_{n+1}
0	0	1	0
0	1	1	1
1	0	0	1
1	1	0	0

3) Sequence:



Example) Mod-18

$$2^4 = 16, 2^5 = 32$$

Ans = 5 FF needed

i.e. 2 FFlops $\Rightarrow 2^2 = \text{modulo } 4$ Self-starting counter = Connected graph
Free running = Perfect cycle.

Register Test

Number System:

Decimal, Binary, Octal, Hex

D \rightarrow B

$$(117)_{10} = \frac{2}{2} \begin{matrix} 1 & 1 & 7 \\ 5 & 8 & 0 \end{matrix} \uparrow \quad = \frac{8}{8} \begin{matrix} 1 & 1 & 7 \\ 4 & 6 & 1 \end{matrix} \uparrow \quad = \frac{16}{16} \begin{matrix} 1 & 1 & 7 \\ 5 & 5 & 1 \end{matrix} \uparrow$$

D \rightarrow O

$$= (165)_8 \quad = (75)_{16}$$

D \rightarrow HB \rightarrow D

$$(10101)_2 = \frac{1}{2} \begin{matrix} 0 & 1 & 0 & 1 & 0 & 1 \end{matrix} \uparrow \quad = \frac{2}{2} \begin{matrix} 0 & 1 & 0 & 1 & 0 & 1 \end{matrix} \uparrow \quad = \frac{1}{1} \begin{matrix} 0 & 0 & 0 & 1 & 0 & 10 & 1 \end{matrix} \uparrow$$

B \rightarrow O

$$= (21)_{10} \quad = (25)_8 \quad = (15)_{16} = (F)_{16}$$

B \rightarrow HO \rightarrow D

$$(345)_8 = \frac{3}{2} \begin{matrix} 3 & 4 & 5 \end{matrix} \uparrow \quad = \frac{2}{2} \begin{matrix} 3 & 4 & 5 \end{matrix} \uparrow \quad = \frac{1}{1} \begin{matrix} 0 & 1 & 1 & 100 & 101 \end{matrix} \uparrow$$

O \rightarrow B

$$= (229)_{10} \quad = (11100101)_2 \quad = \frac{1}{1} \begin{matrix} 0 & 1 & 1 & 100 & 101 \end{matrix} \uparrow$$

O \rightarrow H

$$= (E5)_{16} \quad = (E5)_{16}$$

$H \rightarrow D$	$H \rightarrow B$	$(H \rightarrow O)$
$(AES)_{16}$	$A \quad E \quad 5$	$A \quad E \quad 5$
$16^2 \times 10 + 16^1 \times 4 + 16^0 \times 5$	$1010 \quad 1110 \quad 0101$	$1010 \quad 1110 \quad 0101$
$= (2789)_{10}$	$(10101110010)_2$	$5 \quad 3 \quad 4 \quad 5$

$\boxed{1}$	10000100	0100000011001100110010
$s=1$	$K=8$	$m=23$
		$c_{22}06666$

$$(40.1)_{10} = (101000.00011001100)_2$$

$$= 1.0100066611001100 \times 2^{8+1}$$

$$Bias = 2^{K-1} - 1 = 2^3 - 1 = 127$$

$$BE = 127 + 5 = (132)_{10} = (10000100)_2$$

$\# \rightarrow 2's$	$2's \rightarrow \#$
-7	$+17$
$+7 = 0111$	1011
$+1y = 1000$	$= 010001$
$2's = 1001$	$= -5$

$\# \rightarrow 1's$	$1's \rightarrow \#$
-12	$+20$
$+12 = 01100$	$= 01000$
$1's = 10011$	$= -8$

$322's$ comp. \oplus	+ve	-ve
$NO.$ Extension: $00000000000000000000000000000000$	$00000000000000000000000000000000$	$00000000000000000000000000000000$
Sign magnitude:	$-$	$+$
Example: $\begin{array}{c} \oplus \\ \text{---} \\ - \end{array} = \begin{array}{c} 0 \\ 11111111 \end{array}$	11111111	00000000

$\#$ Floating pt. rep. \Rightarrow $sign \cdot exponent \cdot mantissa$

sign	exponent	mantissa
$\boxed{1}1000101$	10101110	$(5.10)_16$

$$\text{I) } (21.75)_{10} = (10101.11)_2$$

$$= 0.1010111 \times 2^5 \rightarrow e$$

$$\text{II) Bias} = 2^{K-1} = 2^7 = 64$$

$$BE = 64 + 5 = (69)_{10} = (1000101)_2$$

Note: $0 \cdot M \rightarrow$ Explicit (DeGaultin)
 $1 \cdot M \rightarrow$ Implicit (DeGaultin and BCD)

IIEEE 754:	s	K	m
Half Precision		5	10
Single	1	8	23
Double	1	11	52

Note:	$+0$	0	0	0	C_F
	-0	1	0	0	C_F
	$+\infty$	0	255	0	C_8
	$-\infty$	255	0	0	C_5
NAN	$\begin{array}{ c c } \hline 0/1 & 255 \\ \hline 0/1 & 0 \\ \hline \end{array}$	255	$\begin{array}{ c c } \hline \#0 & \#0 \\ \hline \#0 & \#0 \\ \hline \end{array}$		C_3
Fraction					C_2
					C_1
					C_0

Example: IIEEE 754

$\boxed{1}$	10000100	0100000011001100110010
$s=1$	$K=8$	$m=23$
		$c_{22}06666$

Note: $(\leftarrow n_1 \text{ bits} \rightarrow)_{x_1} = (\leftarrow n_2 \text{ bits} \rightarrow)_{x_2}$

$x_1 = x_2$

Note: Range:-

$1's$ compl. $\Rightarrow -2^{n-1} \rightarrow 2^{n-1} = 2^n - 1$

$2's$ compl. $\Rightarrow -2^{n-1} \rightarrow 2^{n-1} = 2^n$

Sign magnitude: $-2^{n-1} \rightarrow 2^{n-1} = 2^n - 1$

Note: $g_P P = 101$ then $8P = 2^3 P = 101000$

Note: Sign magnitude, example -

$\begin{array}{c} \oplus \\ \text{---} \\ - \end{array} = \begin{array}{c} 1111 \\ 1111 \end{array}$

Number extension in sign magnitude

8bit 1101 8bit 011101

10000101 00011101

Note: If base is 16, we write things like

$(-1)^s (0.M) \times 16^{E-bits}$

Note: Condition for overflow during addition of two no.s in 2's complement form:-

$(+A) + (+B) = (-C)$ i.e. for msb

$(-A) + (-B) = +C$ $C_{in} \oplus C_{out} = 1$

Note: When two 4-bit no.'s multiplied

$a_3 \ a_2 \ a_1 \ a_0$

$\times b_3 \ b_2 \ b_1 \ b_0$

$a_3 b_3 \ a_2 b_3 \ a_1 b_3 \ a_0 b_3$

$a_3 b_2 \ a_2 b_2 \ a_1 b_2 \ a_0 b_2$

$a_3 b_1 \ a_2 b_1 \ a_1 b_1 \ a_0 b_1$

$a_3 b_0 \ a_2 b_0 \ a_1 b_0 \ a_0 b_0$

$\times \text{XOR}$

$a_3 b_3 \ a_2 b_3 \ a_1 b_3 \ a_0 b_3$

$a_3 b_2 \ a_2 b_2 \ a_1 b_2 \ a_0 b_2$

$a_3 b_1 \ a_2 b_1 \ a_1 b_1 \ a_0 b_1$

$a_3 b_0 \ a_2 b_0 \ a_1 b_0 \ a_0 b_0$

$C_1 = a_0 b_1 \oplus a_1 b_0$

Note: 8085 MP uses 2's complement rep. for no.'s, where first bit is sign & rest is 2's comp. no.

Note: Prime implicant \Rightarrow Biggest possible grouping
 Implicant \Rightarrow Any possible grouping

Note: Q: q's complement of the given number $(122100)_3$ when it is expressed with the base of 9? 21

#) Binary codes:

① Grey code :-

Decimal \rightarrow Gray

$$(123)_{10} = (1111011)_2$$

$$\begin{array}{ccccccc} & \oplus & & \oplus & & \oplus & \\ 1 & 1 & 1 & 1 & 0 & 1 & 1 \\ \downarrow & & & & & & \\ 0 & 0 & 0 & 1 & 1 & & \end{array}$$

Gray \rightarrow Decimal

$$\begin{array}{ccccccc} & & & & & & \\ 1 & 1 & 1 & 0 & 0 & & \\ \downarrow & \oplus & \uparrow & \uparrow & \uparrow & & \\ 1 & 0 & 1 & 1 & 1 & & \end{array}$$

$$= 23$$

$$(122100)_3 \rightarrow (?)_9$$

$$x_1 = 3, x_2 = x_1 = 3$$

$\stackrel{3^1 3^0 3^1 3^0}{\boxed{1} \boxed{2} \boxed{2} \boxed{0}}$ \Rightarrow Grouping of 2

$$(5 \quad 7 \quad 0)_9$$

Now, directly you can't find q's complement

i) 8's complement 888

$$5 \overline{+} 0$$

$$3 \overline{+} 8$$

ii) 9's complement

$$\therefore \text{Base } 9 = \{0 \text{ to } 8\}$$

$$30 \quad 8+1 = 9$$

$$3 \overline{+} 8$$

* Important points:

* Adder:

② → carry lookahead adder delay
when fan in is 2 $\Rightarrow O(\lg n)$

① → Ripple carry adder delay
when fan in is 2 $\Rightarrow O(n)$

③ → Multiplier delay
when n-bit no. is fed $\Rightarrow O(n)$

* Binary Codes:

→ Hamming distance = No of mismatches
occurring at the same
corresponding positions
in two strings

like: 0 0 0 0 0 $\Rightarrow HDs = 3$
0 1 0 1 1

→ If more than 2 strings there
then $HDs = \min$ (All hamming
distances possible)

→ $HDs = 2d+1$; $d = \max^m$ no. of
erroneous bits
that can be corrected
by code.

* Number Rep^n:

→ In binary adder, while we are

Adding unsigned binary no.'s in
2's complement representation

$$\begin{array}{r} a_{n-1} \dots a_0 \\ b_{n-1} \dots b_0 \\ \hline \text{Cout } c_{n-1} \dots c_0 \end{array}$$

overflow $\Rightarrow a_{n-1}b_{n-1}\bar{c}_{n-1} + \bar{a}_{n-1}\bar{b}_{n-1}c_{n-1} = 1$
cond. n

→ In ripple carry adder, while
adding binary no.'s in 2's complement rep^n

$$\begin{array}{r} A_7 \dots A_0 \\ B_7 \dots B_0 \\ \hline \text{carry} \rightarrow C_7 \dots C_0 \\ \text{sum} \rightarrow S_7 \dots S_0 \end{array}$$

overflow $\Rightarrow A_7 \cdot B_7 \cdot \bar{S}_7 + \bar{A}_7 \cdot \bar{B}_7 \cdot S_7 = 1$
cond. n