Design of 2.4 GHz Bluetooth LNA using 45nm CMOS technology

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***Abstract*—The aim of this assignment is to build a high figure-of-merit (FoM) Bluetooth low-noise amplifier that operates properly in the frequency range between 2.4 GHz & 2.5 GHz, using the 45nm CMOS technology. In this document, a comparison is made between two common topologies, the common-source (CS) amplifier & the cascode CS amplifier. Both circuits are designed to achieve the highest possible FoM within the allowable power budget & also maintain suitable impedance matching. Both circuits are tested through software simulations using Cadence Virtuoso's Analog-Design Environment (ADE).**

***Index Terms*— Common-source amplifier, Low-noise amplifier, Noise figure, S-parameters, Compression point, Impedance Matching**

I. Introduction

In any radio-frequency (RF) integrated circuit system, the low-noise amplifier (LNA) is usually the first active stage of the receiver, thus making its design of crucial importance.[1] The receiver receives a weak signal at the antenna that, in order to be utilized, must be amplified before being processed on in the following stages, making the small-signal AC gain (A_V) a critical design specification of the LNA. The received signal also contains noise that is added to it before reaching the receiver. Completely removing the noise is impossible, but with careful design, the amount of noise added & the amount by which the noise is amplified with respect to the desired signal can be decreased by minimizing the amplifier's noise figure (NF).

Another important consideration is the S_{11}, or the input reflection coefficient. This parameter shows the amount of signal power transferred from the input to the output. To keep S_{11} at a minimum value (for maximum power transfer), careful matching between the antenna & the LNA is ensured using a matching circuit.

Additionally, the linearity of the LNA's circuit determines the maximum allowable power level of the input. This is expressed by the input compression point (P_{-1dB}). As it will be shown later, there is a tradeoff between the desirable values of the S_{11}, NF, A_V, and the linearity. So, the aim of the design is to reach a compromise between the parameters to achieve a high FoM with good matching.

II. CS Amplifier

The CS amplifier circuit along with the matching circuit is shown in Fig. 1. The CS amplifier is one of the commonly used topologies due to its high input impedance & its good gain. An inductive load is employed instead of a resistive load as it sustains a lower DC voltage drop & causes the circuit to operate at higher frequencies.

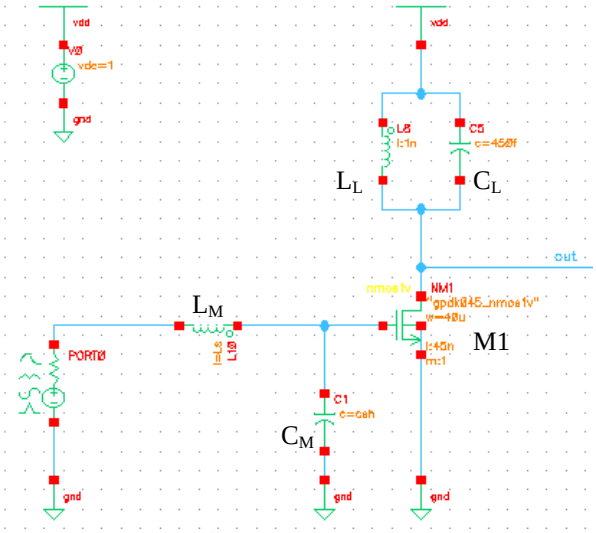

Fig. 1. CS amplifier with inductive & capacitive loads

The input impedance seen by the antenna into the matching circuit is given by equation (1). The values of L_M & C_M of the matching circuit are chosen carefully to match the 50 ohm resistance of the antenna.

$$Z_{in} = j\omega L_M + \frac{1}{j\omega(C_M + C_{GS})} \qquad (1)$$

At the output side of the amplifier, the inductive load L_L is chosen to resonate at 2.45 GHz with the capacitances at the output node, which is a combination of the parasitic capacitances of M_1 at the output node & the load capacitance C_L. The relation between the resonance frequency ω_O & the inductive load is given in equation (2).

Since the inductance & the capacitance cancel out at resonance, the voltage gain at this frequency will depend on the parasitic resistance R_S in series with the inductor, as shown in equation (3). This gain is without considering the matching circuit which will cause an increase in the gain's value as will be discussed later.

$$\omega_O = \frac{1}{\sqrt{L_L \cdot C_{out}}} \quad (2)$$

$$|A_V| = g_m (R_L \parallel r_{ds}) \quad (3)$$

III. Cascode CS Amplifier

Another common topology is the cascode amplifier shown in Fig. 2. In addition to providing greater gain, the cascode amplifier can also provide isolation between the input & the output nodes [2]. In the CS amplifier, the inductive load can cause a negative resistance due to the feedback through C_{GD}, which can in turn cause instability.

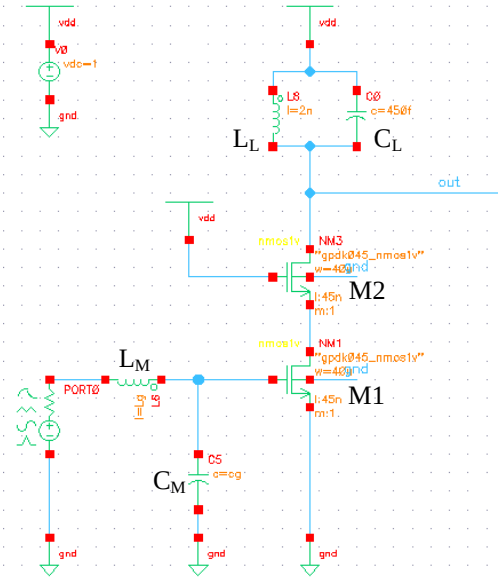

Fig. 2. Cascode CS amplifier

IV. Specifications

The specifications which the design of the LNA along with the matching circuit is based on are shown in Table I.

TABLE I
Desired Design Specs

Specifications	Values
Supply Voltage	1 V
|S11|	< -10 dB
Voltage Gain	> 15 dB
Noise Figure	< 3.5 dB
P_{-1dB}	> -10 dBm
P_{dc}	< 2 mW

Since there are tradeoffs between the different design parameters, it is very difficult to achieve all of the specs together. Thus, the parameters are optimized such that the maximum FoM is achieved, according to equation (4) [3].

$$\text{FoM} = \frac{A_v \cdot f \cdot P_{-1dB}}{(NF - 1) \cdot P_{dc}} \quad (4)$$

where A_v & NF are in their absolute values, and P_{-1dB} & P_{dc} are in milliwatts. The operation frequency, f, is given in MHz.

A. Input Reflection Coefficient

The input reflection coefficient (S_{11}) is an indication of how well the input impedance matching is done with the antenna's 50 ohm impedance. It is defined by the ratio of the reflected wave & the incident wave at the input port when there's no reflection coming from the output port. S_{11} can be found using the relation in equation (5). For better power transfer, the matching should bring Z_{in} close to R_S, which is 50 ohms. The better the matching, the less the value of S_{11} will be.

$$S_{11} = \frac{Z_{in} - R_S}{Z_{in} + R_S} \quad (5)$$

B. Noise Figure

The noise figure is considered a measurement of the noise performance of a circuit. It is the ratio between the input SNR & the output SNR of the LNA. From equation (6), it is shown that by increasing the gain of the circuit, the NF is decreased. This is done by increasing gm, but this also increases the current, which in turn causes the power dissipation of the circuit to go up.

$$NF = 1 + \frac{\bar{v}_{n,out}^2}{A_v^2 \cdot \bar{v}_{n,RS}^2} \quad (6)$$

C. AC Small-Signal Gain

The LNA is designed as a narrowband amplifier where the gain is high in a specific frequency range, around the resonance frequency, as mentioned in equation (3). Adding the matched circuit also helps in increasing the gain by a factor of Q, which is the quality factor of the RLC matching circuit.

$$|A_V| = Q \cdot G_m \cdot R_L \quad (7)$$

D. 1dB Compression Point

P_{-1dB} is the input power level at which the gain decreases from the linear case by 1dB, & can be calculated using the fundamental coefficient (α_1) & the 3rd order non-linearity coefficient (α_3) in the input/output characteristic equation.

$$A_{in,1dB} = \sqrt{0.145 \frac{\alpha_1}{\alpha_3}} \quad (8)$$

$$P_{-1dB} = \frac{A_{in,1dB}^2}{R} \quad (9)$$

The linearity of the circuit is inversely proportional to the gain, so there is a direct tradeoff between P_{-1dB} & A_V. Changing A_V also affects S_{11} & NF, as NF increases as the gain decreases, and S_{11} increases as Q decreases. As a result, improving the linearity comes at the cost of worse A_v, NF, & S_{11} performance.

E. Power Dissipation

One of the ways to increase the gain & decrease the NF is to increase the drain current. But the current drawn from the source is limited by the allowable power budget, given by equation (10).

$$P_{dc} = I_{DS} \cdot V_{DD} \qquad (10)$$

V. Simulation & Results

The transistors' sizes, the passive components & the bias voltage are chosen to meet the required specifications within the allowable power budget for both the CS circuit & the cascode circuit. The values used in each circuit are shown in Table II.

TABLE II
CIRCUIT PARAMETERS FOR THE LNAS

PARAMETERS		CS	Cascode
Biasing	V_b	0.62 V	0.6 V
CS stage	M_1	40 um / 45 nm	40 um / 45 nm
CG stage	M_2	-	40 um / 45 nm
Matching	L_M	88 nH (Q=33.87)	58 nH (Q=29.76)
	R_M	40 Ω	30 Ω
	C_M	20 fF	40 fF
Load	L_L	1 nH (Q=10)	2 nH (Q=10)
	R_L	1.54 Ω	3 Ω
	C_L	50 fF	450 fF

A. AC Analysis

The AC analysis is performed to observe the AC gain of the LNA. As shown in Fig. 3, the gain is small at low frequencies but increases dramatically at the operating frequency due to the resonance of L_L with the output capacitance.

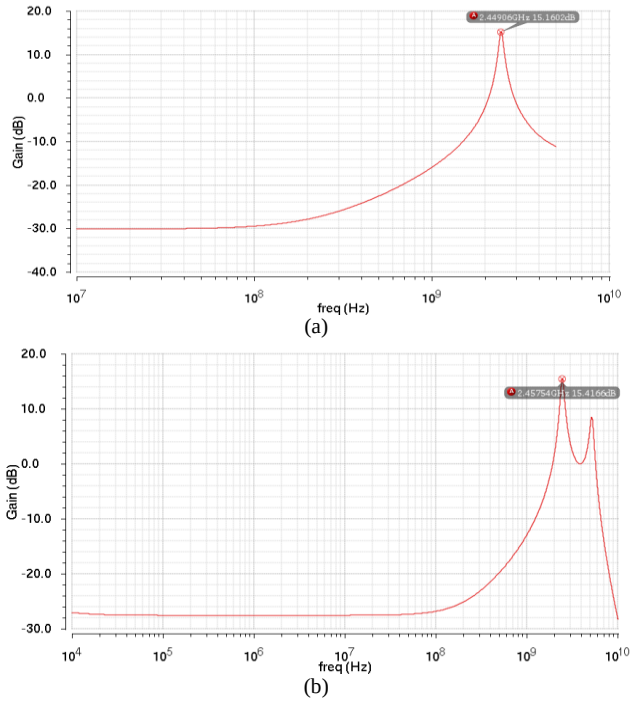

Fig. 3. Gain for (a) CS amplifier, (b) Cascode amplifier

B. S-Parameters Analysis

In the SP analysis, the smith chart is used to choose the suitable values for L_M & C_M to get the minimum S_{11} peak at the 2.45 GHz. Fig. 4. Shows the S_{11} curve on the smith chart after the matching, and S_{11} & NF are plotted against the frequency in Fig. 5.

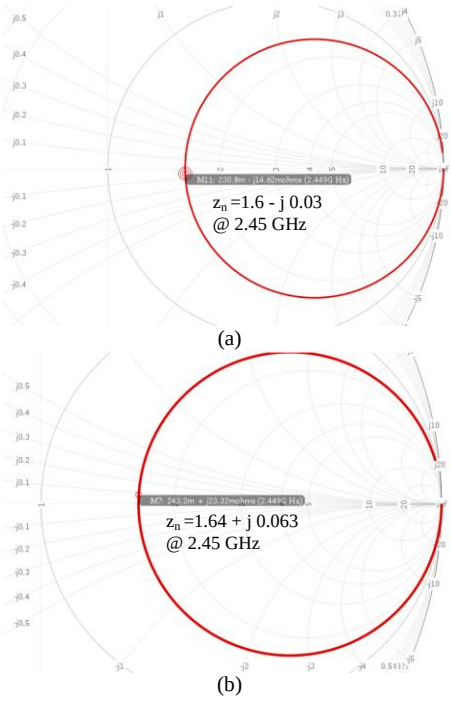

Fig. 4. S11 smith chart for (a) CS amplifier, (b) Cascode amplifier

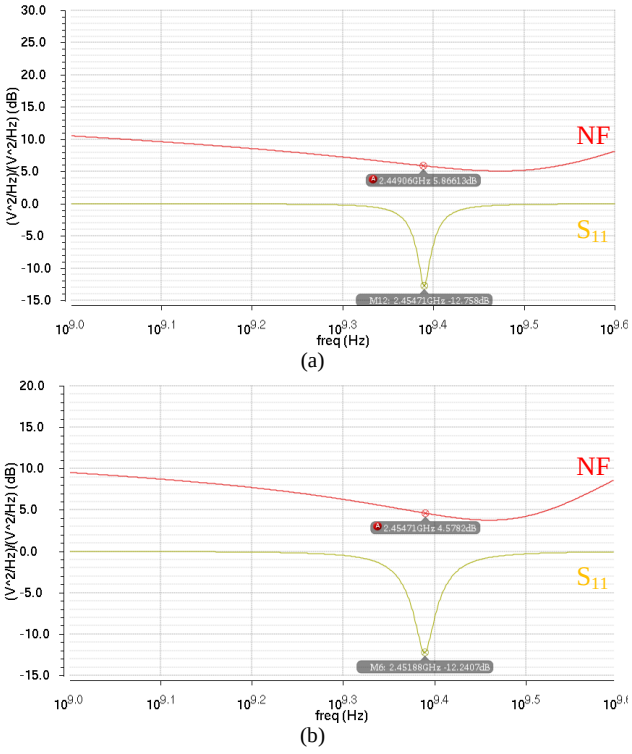

Fig. 5. NF & S11 for (a) CS amplifier, (b) Cascode amplifier

C. Periodic Steady State Analysis

The P_{-1dB} is found by drawing the input power against the output power, then comparing the resulting curve with the linear case using the PSS analysis.

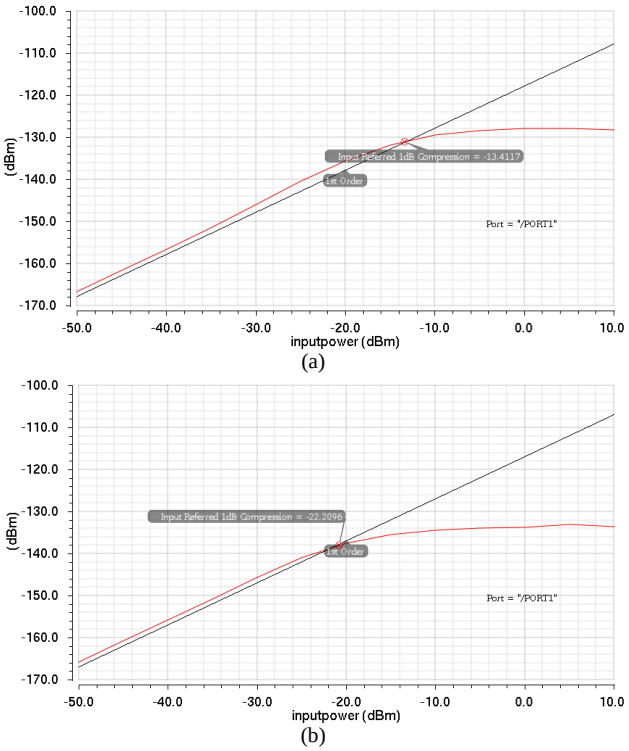

Fig. 6. P_{-1dB} for (a) CS amplifier, (b) Cascode amplifier

VI. Conclusion

This document presented the design procedures of 2 common LNA topologies & the considerations taken into account for the achieved specifications. While the achieved FoM in both the CS amplifier & the Cascode amplifier are not as high as other LNAs presented in reference [3], the S_{11} parameter of the designed LNAs is better than those in reference [3]. It is found that it is very difficult to achieve a low S_{11} & a high FoM at the same time, due to the trade-off between S_{11} & P_{-1dB}.

TABLE III
Achieved Results for the LNAs

	CS LNA	Cascode LNA
Frequency of Operation	2.45 GHz	2.45 GHz
g_m	18.5 mS	16.32 mS
P_{dc}	1.7 mW	1.54 mW
Gain	15.16 dB	15.42 dB
S11	-12.758 dB	-12.241 dB
NF	5.866 dB	4.578 dB
P_{1dB}	-13.411 dBm	-22.209 dBm
FoM	**131.5677 MHz**	**30.1769 MHz**

The final results achieved by both circuits are shown in Table III. It can be seen that the Cascode LNA can achieve almost the same gain & S_{11} with better NF at a lower P_{dc}, while it is easier to achieve a much better P_{1dB} (better linearity) in the case of the CS LNA, which is the reason why the CS LNA has a better FoM.

In future work, other LNA topologies will be studied & compared to be able to find the best option in terms of FoM. Also, other matching circuit topologies need to be investigated with the aim of improving both the S_{11} & the P_{-1dB} performances together.

References

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