ELE404: CE-CE-CC Amplifier Design

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Table of Contents

1.Introduction

This project focuses on designing a single-supply, multistage, inverting transistor amplifier, a challenging task that combines theoretical knowledge with practical application. The objective is to meet a set of precise specifications, including power supply constraints, quiescent current limitations, specific voltage gain requirements under various loads, and a wide frequency response, using no more than three Bipolar Junction Transistors (BJTs). This report documents the design process, from the selection and justification of the amplification stages to the detailed calculations for component values. It also compares the theoretical expectations with simulation results using tools like Multisim, offering insights into the performance and design choices of the amplifier.

2.Theory

The main goal of this project is the design of a CE-CE-CC (Common Emitter-Common Emitter-Common Collector) amplifier, a sophisticated electronic circuit intended for amplifying signals. This section outlines the fundamental theoretical concepts and specifications guiding the design process.

1. Amplifier Configuration: CE-CE-CC

> **Common Emitter (CE) Stage:** Characterized by a high voltage gain, the CE stage is crucial for amplifying the signal's amplitude. Its primary role in this design is to provide the necessary gain to meet the overall specifications. Two CE stages are utilized to achieve a substantial cumulative gain.
>
> **Common Collector (CC) Stage:** Often referred to as an emitter follower, the CC stage is implemented primarily for its ability to provide a high input impedance, low output impedance, and unity voltage gain. This makes it ideal as the final stage, ensuring minimal loading effect on the preceding stages and maintaining the amplifier's overall gain.

2. Specifications

> **Power Supply:** The amplifier operates on a +10V supply, ensuring compatibility with standard electronic devices.
>
> **Quiescent Current:** Limited to no more than 10mA, this specification ensures power efficiency and minimizes thermal stress on the components.
>
> **Voltage Gain:** The design must achieve a no-load voltage gain (|Av0|) of 50 (±10%) at 1 kHz. Under a load of 1 kΩ, the loaded voltage gain should be at least 90% of the no-load gain.

Output Voltage Swing: The maximum no-load output voltage swing should be no smaller than 8V peak-to-peak at 1 kHz. With a load of 1 kΩ, this requirement changes to a minimum of 4V peak-to-peak.

Input Resistance: At a minimum of 20 kΩ, a higher input resistance ensures lower loading of the signal source.

Frequency Response: The amplifier must maintain its performance within a frequency range of 20 Hz to 50 kHz, with a -3dB response at the boundaries of this range.

3. Component Selection

Transistors: Limited to using BJTs, which offer high current gain and can operate efficiently at low power.

Resistors and Capacitors: Values are restricted to those available in the E24 series and specific capacitance values, influencing the frequency response and stability of the amplifier.

4. Distortion and Source Resistance

Output Voltage: It must be free from distortions like clipping under all test conditions, ensuring signal integrity.

Source Resistance: Set at 600Ω for all tests, influencing the design's impedance matching and overall performance.

5. Coupling and Biasing

AC Coupling: Essential for interfacing the load and signal source, it blocks DC components while allowing AC signals to pass.

Biasing: Proper biasing of transistors is critical for ensuring optimal operation and stability of the amplifier.

This theoretical foundation establishes the guidelines for designing the CE-CE-CC amplifier. It addresses the need for a balance between gain, impedance characteristics, frequency response, and power efficiency, all while conforming to specified constraints

3.Results

Hand calculations are to be found in the appendix.

I_B	$I_{B,DC}$	β	I_C	V	g_m
3.5µA	2µA	114.3	400µA	4.25 V	0.015 S

Table1. Values of CE amplifier.

I_B	$I_{B,DC}$	β	I_C	V	g_m
65 mA	30µA	154	10 mA	5 V	0.39 S

Table2. Values of CC amplifier.

C_1	C_2	C_3	C_4	C_5	C_6
10µF	100µF	10µF	100µF	10µF	100µF

Table3. Values of Capacitors.

R_1	R_2	R_3	R_4	R_5	R_6	R_{C1}	R_{C2}	R_{E1}	R_{E2}	R_{E3}	R_{E4}	R_{E5}	R_L
91 kΩ	68 kΩ	91 kΩ	68 kΩ	91 kΩ	200 kΩ	15 kΩ	13 kΩ	15 kΩ	1.5 kΩ	15 kΩ	1.3 kΩ	1 kΩ	1 kΩ

Table4. Values of resistors.

4.Simulation

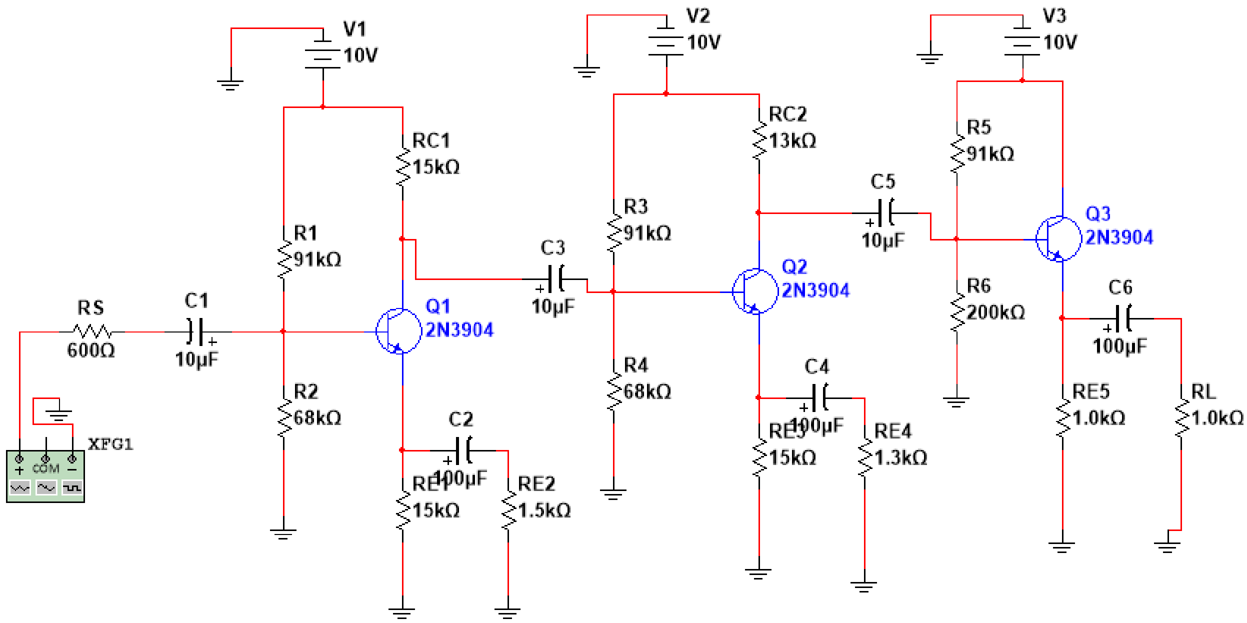


Figure1. Circuit Diagram.

DC sweep analysis was used to determine the load line and the operation point.

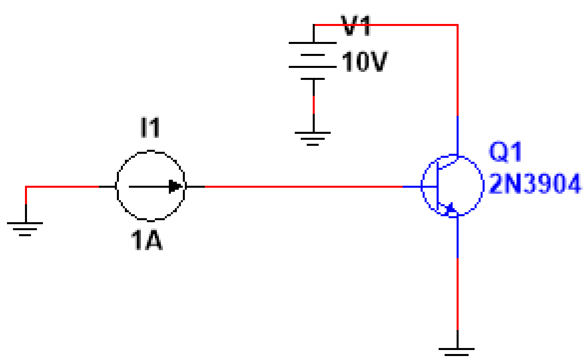


Figure2. DC sweep circuit.

Graphs:

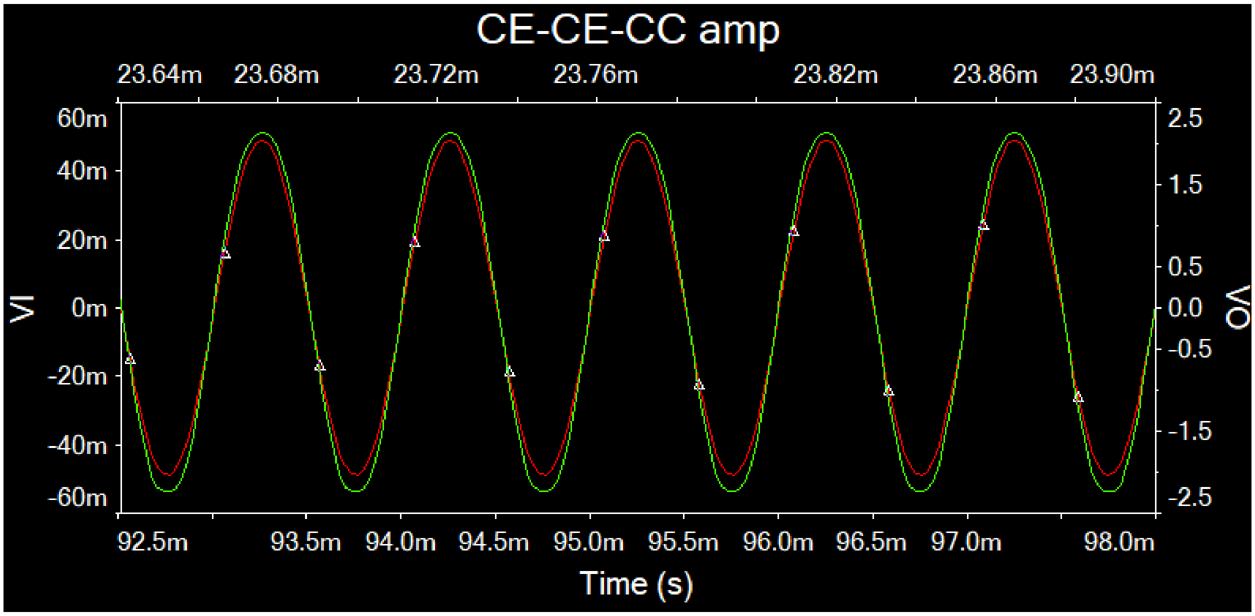


Figure3. Input and output voltages graph (R_L = 1k)

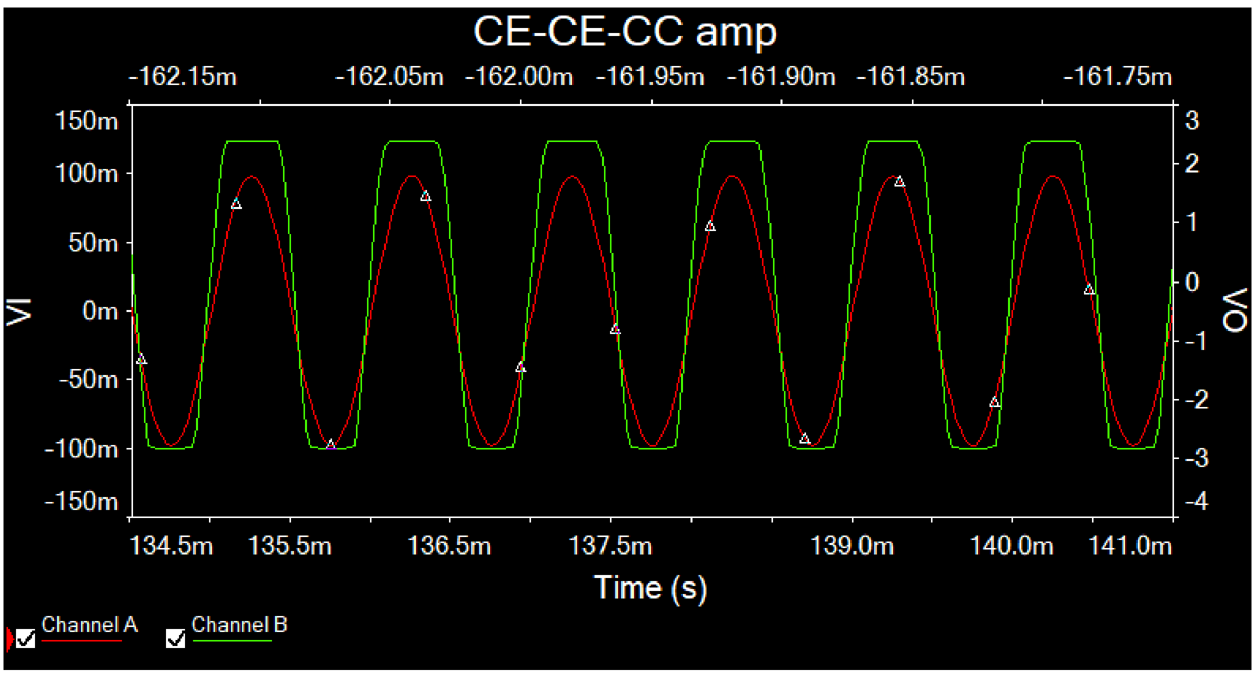


Figure4. Input and output voltages graph (R_L = ∞)

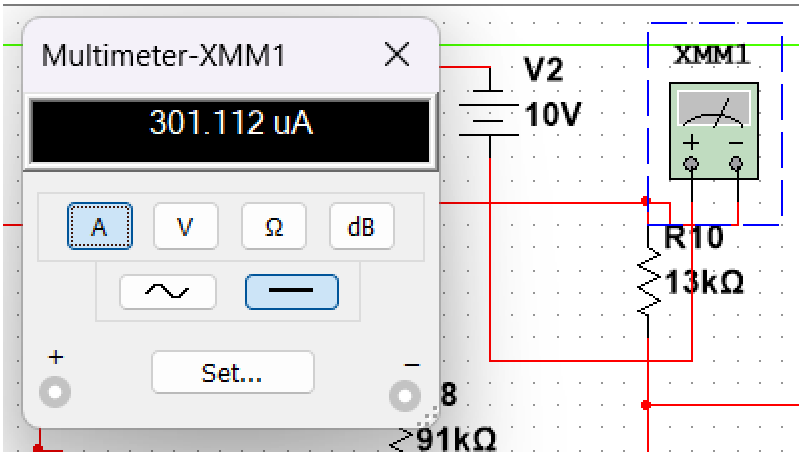


Figure5. Current drawn from power source.

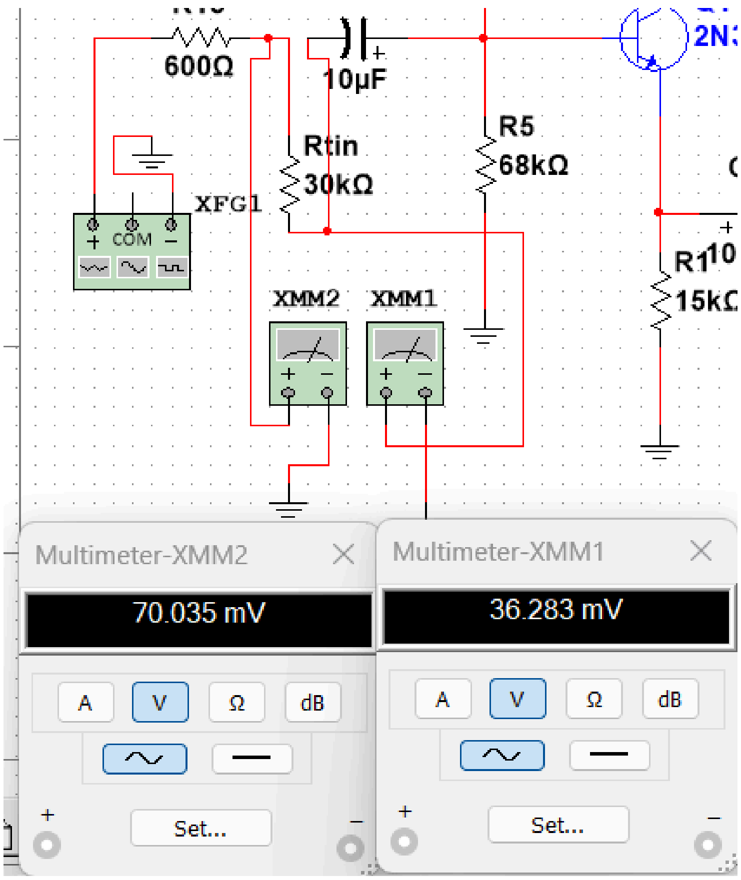


Figure6. V_t and V_I values.

$$R_i = R_{t,in}\left(\frac{v_i}{v_t - v_i}\right)$$

$R_i = 61\ \text{k}\Omega$

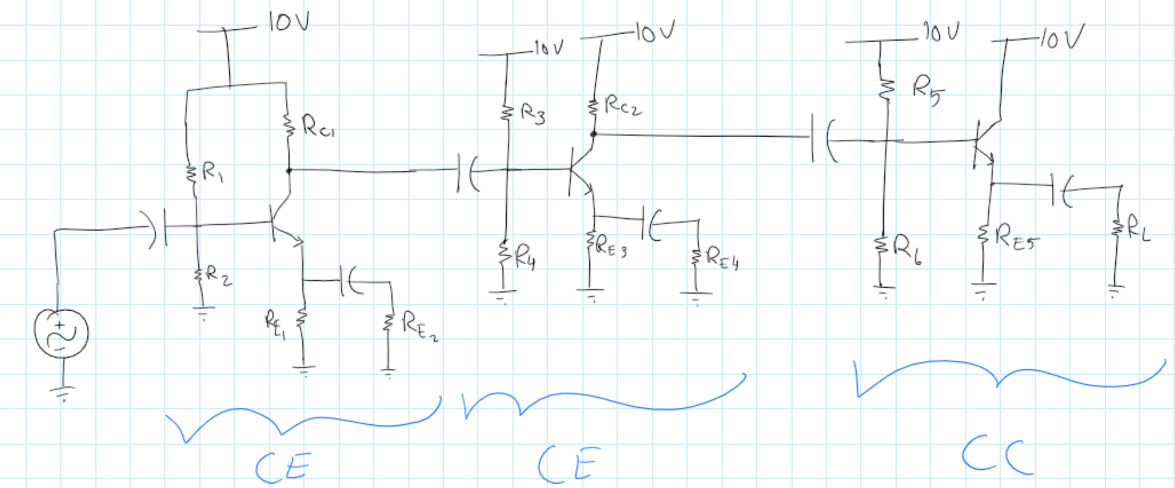
5.Discrepancies and Conclusion

Overall, the experimental and theoretical calculations match and fall within the design specifications. Minor discrepancies are found, most likely due to rounding errors and simulation inaccuracies. Despite the discrepancies, the CE-CE-CC amplifier performs as outlined in the design specifications and passes most of the tests.

6.Appendix

Hand calculations -

Hand Calculations :



$V_{cc} = 10V$, $I_{DC} < 10 mA$, $A_{V_o} = 50$, $V_o \geq 8 V_{pp}$, $V_L \geq 4 V_{pp}$, $R_{in} \geq 20 k\Omega$

Total gain: $50 = A_{V_{o1}} \times A_{V_{o2}} \times A_{V_{o3}}$

gain of CC stage is almost 1 so $A_{V_{o3}} = 1$. So we can say $\underbrace{A_{V_{o1}} = A_{V_{o2}}}_{\text{For the CE amplifier}} = -\sqrt{50} \approx -7.1$

-ve since its an inverting amplifier.

According to the chosen load line, $I_C = 400\ \mu A$

$$g_m = \frac{I_C}{V_T} = \frac{400\ \mu A}{26\ mV} = 0.015\ S$$

$$I_B = 3.5\ \mu A$$

$$\beta = \frac{400}{3.5} = 114.3$$

$$I_{B,DC} = 2\ \mu A$$

Now, for CC amp.

$R_{E5} = 1k\Omega$ so its similar to R_L.

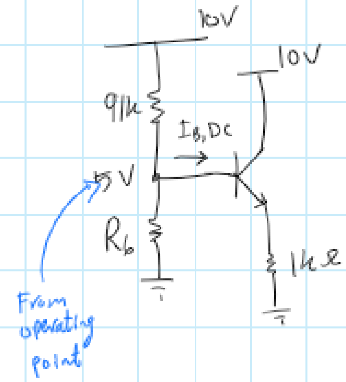
$I_c = 10\ mA$

$I_B = 65\ \mu A$

$$\beta = \frac{10}{65\times10^{-3}} = 154$$

In order to stay within the spec of E24 series, $R_5 = 91\,k\Omega$.

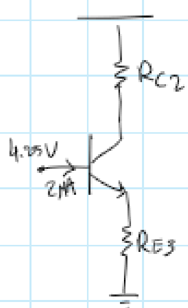
$$g_m = \frac{10}{26} = 0.39$$



KCL:

$$\frac{5-10}{91k} + \frac{5}{R_b} + 30\,\mu A = 0$$

$$\boxed{R_b \approx 200\,k\Omega}$$



KVL:

$$-4.25 + 0.7 + \overset{(1+\beta)I_B}{I_E}(R_{E3}) = 0$$

$$\boxed{R_{E3} \approx 15\,k\Omega}$$

$$I_{C,DC} = \frac{V_{CC}}{R_C + R_{E3}}$$

$$\boxed{R_C = 10\,k\Omega}$$

$$\frac{1}{10k} = \frac{1}{R_{C2}} + \frac{1}{R_{in3}}$$

$$R_{in3} = R_5 \,//\, R_b \,//\, \frac{\beta}{g_m} + (\beta+1)R_E$$

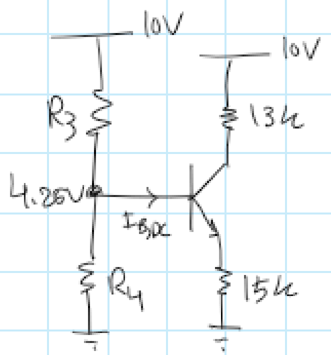
$$\approx 44.6\,k\Omega$$

$$\boxed{R_{C_2} \approx 13\,k\Omega}$$

$$A_{vo2} = \frac{-g_{m_2}(R_{C2} // R_{in3})}{1 + g_{m_2} R_E}$$

$$\boxed{R_E \approx 1.3\,k\Omega}$$

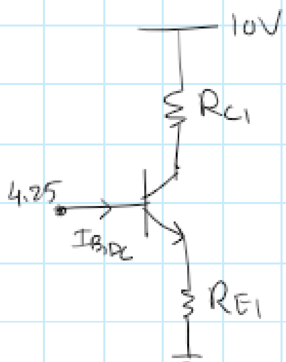
$$1.3k\Omega = \frac{1}{\frac{1}{R_{E3}} + \frac{1}{R_{E4}}} \Rightarrow \boxed{R_{E4} \approx 1.3\,k\Omega}$$



KCL

$$\frac{4.25-10}{91k} + \frac{4.25}{R_4} + 2\mu A = 0$$

$$\boxed{R_4 \approx 68\,k\Omega}$$



KVL

$$-4.25 + 0.7 + (1+\beta) I_B R_{E_1} = 0$$

$$\boxed{R_{E_1} \approx 15\,k\Omega}$$

$$25\,k\Omega = R_{C_1} + R_{E_1}$$

$$R_C = 10\,k\Omega$$

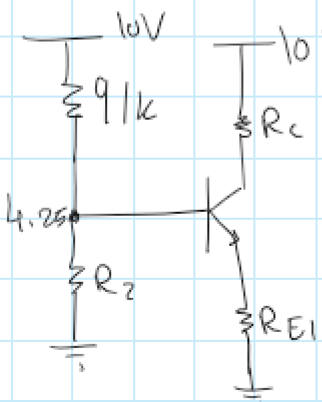
$$R_C = R_{C_1} // \underbrace{R_{in2}} \rightarrow = R_3 // R_4 // \frac{\beta}{g_m} + (\beta+1) R_E$$

$\approx 31\,k\Omega$

$\boxed{R_{C_1} \approx 15\,k\Omega}$

$$A_{V_1} = \frac{-g_m\left(R_{C_1} // R_{in_2}\right)}{1 + g_m R_E} \Rightarrow \boxed{R_E \approx 1.3\,k\Omega}$$

$$R_E = R_{E_1} // R_{E_2} \rightarrow \boxed{R_{E_2} = 1.5\,k\Omega}$$



KCL

$$\frac{4.25-10}{91k} + \frac{4.25}{R_2} + 2\,\mu A = 0$$

$\boxed{R_2 \approx 68\,k\Omega}$

Capacitors C_2, C_4, C_6 need to be higher so we'll use 100 μF.

The rest can be 10 μF.

Now,

$$I_{DC,total} = I_{C_1} + I_{R_1} + I_{C_2} + I_{R_3} + I_{C_3} + I_{R_5}$$

$$= \beta I_{B_1} + \frac{V_{CC}}{R_1+R_2} + \beta I_{B_2} + \frac{V_{CC}}{R_3+R_4} + \beta I_{B_3} + \frac{V_{CC}}{R_5+R_6}$$

$$\approx \boxed{5.23\ \text{mA}}$$