#### **Features**

- High Performance, Low Power AVR® 8-Bit Microcontroller
- Advanced RISC Architecture
  - 131 Powerful Instructions Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 20 MIPS Throughput at 20 MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory Segments
  - 4/8/16/32K Bytes of In-System Self-Programmable Flash progam memory (ATmega48P/88P/168P/328P)
  - 256/512/512/1K Bytes EEPROM (ATmega48P/88P/168P/328P)
  - 512/1K/1K/2K Bytes Internal SRAM (ATmega48P/88P/168P/328P)
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C<sup>(1)</sup>
  - Optional Boot Code Section with Independent Lock Bits In-System Programming by On-chip Boot Program True Read-While-Write Operation
  - Programming Lock for Software Security
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Six PWM Channels
  - 8-channel 10-bit ADC in TQFP and QFN/MLF package Temperature Measurement
  - 6-channel 10-bit ADC in PDIP Package Temperature Measurement
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Byte-oriented 2-wire Serial Interface (Philips I<sup>2</sup>C compatible)
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
  - Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
- I/O and Packages
  - 23 Programmable I/O Lines
  - 28-pin PDIP, 32-lead TQFP, 28-pad QFN/MLF and 32-pad QFN/MLF
- Operating Voltage:
  - 1.8 5.5V for ATmega48P/88P/168PV
  - 2.7 5.5V for ATmega48P/88P/168P
  - 1.8 5.5V for ATmega328P
- Temperature Range:
  - -40°C to 85°C
- Speed Grade:
  - ATmega48P/88P/168PV: 0 4 MHz @ 1.8 5.5V, 0 10 MHz @ 2.7 5.5V
  - ATmega48P/88P/168P: 0 10 MHz @ 2.7 5.5V, 0 20 MHz @ 4.5 5.5V
  - ATmega328P: 0 4 MHz @ 1.8 5.5V, 0 10 MHz @ 2.7 5.5V, 0 20 MHz @ 4.5 5.5V
- Low Power Consumption at 1 MHz, 1.8V, 25°C for ATmega48P/88P/168P:
  - Active Mode: 0.3 mA
  - Power-down Mode: 0.1 μA
  - Power-save Mode: 0.8 μA (Including 32 kHz RTC)



8-bit **AVR**® Microcontroller with 4/8/16/32K Bytes In-System Programmable Flash

ATmega48P/V ATmega88P/V ATmega168P/V ATmega328P

**Preliminary** 

**Summary** 

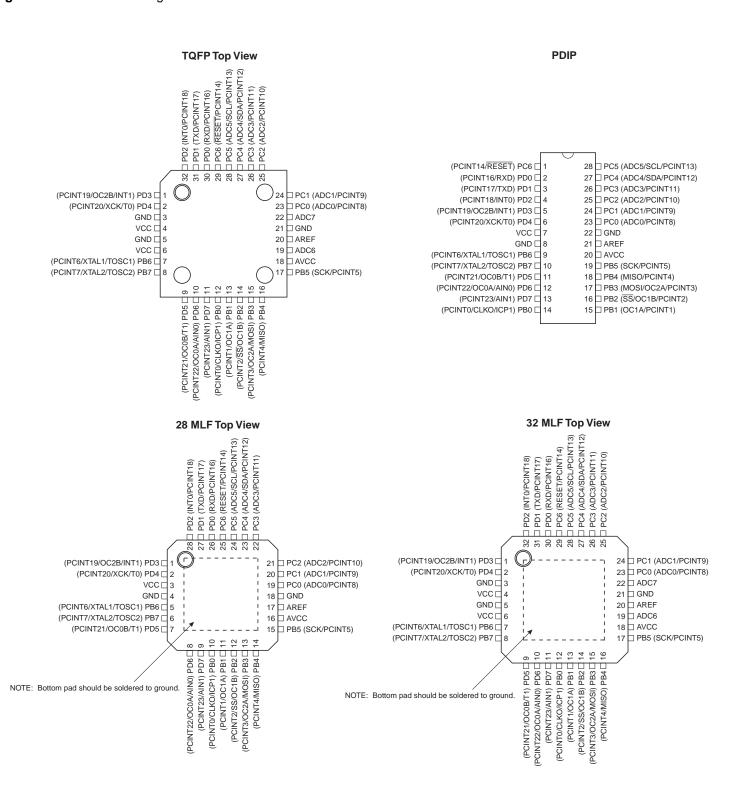






# 1. Pin Configurations

Figure 1-1. Pinout ATmega48P/88P/168P/328P



### 1.1 Pin Descriptions

#### 1.1.1 VCC

Digital supply voltage.

#### 1.1.2 GND

Ground.

#### 1.1.3 Port B (PB7:0) XTAL1/XTAL2/TOSC1/TOSC2

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Depending on the clock selection fuse settings, PB6 can be used as input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

Depending on the clock selection fuse settings, PB7 can be used as output from the inverting Oscillator amplifier.

If the Internal Calibrated RC Oscillator is used as chip clock source, PB7..6 is used as TOSC2..1 input for the Asynchronous Timer/Counter2 if the AS2 bit in ASSR is set.

The various special features of Port B are elaborated in "Alternate Functions of Port B" on page 82 and "System Clock and Clock Options" on page 26.

#### 1.1.4 Port C (PC5:0)

Port C is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The PC5..0 output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

#### 1.1.5 PC6/RESET

If the RSTDISBL Fuse is programmed, PC6 is used as an I/O pin. Note that the electrical characteristics of PC6 differ from those of the other pins of Port C.

If the RSTDISBL Fuse is unprogrammed, PC6 is used as a Reset input. A low level on this pin for longer than the minimum pulse length will generate a Reset, even if the clock is not running. The minimum pulse length is given in Table 28-3 on page 320. Shorter pulses are not guaranteed to generate a Reset.

The various special features of Port C are elaborated in "Alternate Functions of Port C" on page 85.

#### 1.1.6 Port D (PD7:0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.





The various special features of Port D are elaborated in "Alternate Functions of Port D" on page 88.

# 1.1.7 AV<sub>CC</sub>

 $AV_{CC}$  is the supply voltage pin for the A/D Converter, PC3:0, and ADC7:6. It should be externally connected to  $V_{CC}$ , even if the ADC is not used. If the ADC is used, it should be connected to  $V_{CC}$  through a low-pass filter. Note that PC6..4 use digital supply voltage,  $V_{CC}$ .

#### 1.1.8 AREF

AREF is the analog reference pin for the A/D Converter.

#### 1.1.9 ADC7:6 (TQFP and QFN/MLF Package Only)

In the TQFP and QFN/MLF package, ADC7:6 serve as analog inputs to the A/D converter. These pins are powered from the analog supply and serve as 10-bit ADC channels.

#### 1.2 Disclaimer

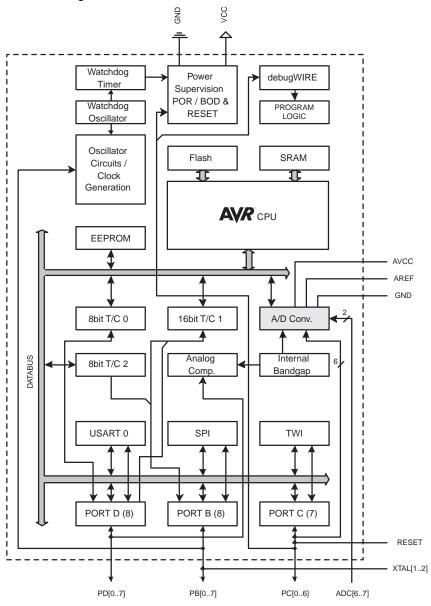
Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

#### 2. Overview

The ATmega48P/88P/168P/328P is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega48P/88P/168P/328P achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

## 2.1 Block Diagram

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting





architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega48P/88P/168P/328P provides the following features: 4K/8K/16K/32K bytes of In-System Programmable Flash with Read-While-Write capabilities, 256/512/512/1K bytes EEPROM, 512/1K/1K/2K bytes SRAM, 23 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte-oriented 2-wire Serial Interface, an SPI serial port, a 6-channel 10-bit ADC (8 channels in TQFP and QFN/MLF packages), a programmable Watchdog Timer with internal Oscillator, and five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, USART, 2-wire Serial Interface, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip Boot program running on the AVR core. The Boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega48P/88P/168P/328P is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega48P/88P/168P/328P AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

#### 2.2 Comparison Between ATmega48P, ATmega88P, ATmega168P, and ATmega328P

The ATmega48P, ATmega88P, ATmega168P, and ATmega328P differ only in memory sizes, boot loader support, and interrupt vector sizes. Table 2-1 summarizes the different memory and interrupt vector sizes for the three devices.

Table 2-1.Memory Size Summary

Device	Flash	EEPROM	RAM	Interrupt Vector Size
ATmega48P	4K Bytes	256 Bytes	512 Bytes	1 instruction word/vector
ATmega88P	8K Bytes	512 Bytes	1K Bytes	1 instruction word/vector
ATmega168P	16K Bytes	512 Bytes	1K Bytes	2 instruction words/vector
ATmega328P	32K Bytes	1K Bytes	2K Bytes	2 instructions words/vector

ATmega88P, ATmega168P, and ATmega328P support a real Read-While-Write Self-Programming mechanism. There is a separate Boot Loader Section, and the SPM instruction can only execute from there. In ATmega48P, there is no Read-While-Write support and no separate Boot Loader Section. The SPM instruction can execute from the entire Flash.

# 3. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

# 4. Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.





# 5. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xFF)	Reserved	-	-	_	_	_	_	_	_	
(0xFE)	Reserved	_	_	_	_	_	_	_	_	
(0xFD)	Reserved	_	_	_	_	_	_	_	_	
(0xFC)	Reserved	_	_	_	_	_	_	_	_	
(0xFB)	Reserved	_	_	_	_	_	_	-	-	
(0xFA)	Reserved	_	_	_	_	_	-	_	-	
(0xF9)	Reserved	-	-	_	_	_	_	_	_	
(0xF8)	Reserved	-	-	_	_	_	_	-	_	
(0xF7)	Reserved	_	_	_	_	_	-	-	_	
(0xF6)	Reserved	-	-	-	-	-	-	-	-	
(0xF5)	Reserved	-	-	-	-	-	-	-	-	
(0xF4)	Reserved	-	_	-	-	_	-	-	-	
(0xF3)	Reserved	-	-	-	-	-	-	-	-	
(0xF2)	Reserved	-	-	_	_	_	_	_	_	
(0xF1)	Reserved	-	-	-	_	_	-	_	_	
(0xF0)	Reserved	-	-	-	_	_	-	_	_	
(0xEF)	Reserved	-	-	_	_	-	-	_	-	
(0xEE) (0xED)	Reserved Reserved	_	_	_	_	_	_	_	_	
(0xEC)	Reserved	_	_	_		_	_	_		
(0xEB)	Reserved	_		_						
(0xEA)	Reserved	_	_	_	_	_	_	_	_	
(0xE9)	Reserved	_	_	_	_	_	_	_	_	
(0xE8)	Reserved	-	_	_	_	_	_	_	_	
(0xE7)	Reserved	-	_	_	_	_	_	_	_	
(0xE6)	Reserved	-	_	-	-	_	-	_	_	
(0xE5)	Reserved	_	_	_	_	_	-	_	-	
(0xE4)	Reserved	-	-	_	_	_	_	_	_	
(0xE3)	Reserved	-	-	_	_	_	_	-	_	
(0xE2)	Reserved	-	-	-	-	-	-	-	-	
(0xE1)	Reserved	_	-	_	_	_	_	-	-	
(0xE0)	Reserved	-	-	-	-	-	-	-	-	
(0xDF)	Reserved	-	-	-	-	-	-	-	-	
(0xDE)	Reserved	_	_	-	-	_	-	_	-	
(0xDD)	Reserved	-	-	_	_	_	_	_	_	
(0xDC)	Reserved	-	_	-	_	_	-	_	-	
(0xDB)	Reserved	-	-	-	_	_	-	_	-	
(0xDA)	Reserved	-	_	_	_	_	-	_	-	
(0xD9) (0xD8)	Reserved Reserved	-	-	_	_	_	_	-	_	
(0xD8)	Reserved	_		_			_			
(0xD6)	Reserved	_	_	_	_	_	_	_	_	
(0xD5)	Reserved	_	_	_	_	_	_	_	_	
(0xD4)	Reserved	_	_	_	_	_	_	_	_	
(0xD3)	Reserved	-	_	_	_	_	_	_	_	
(0xD2)	Reserved	-	_	-	-	_	_	_	_	
(0xD1)	Reserved	-	_	_	_	=	=	_	-	
(0xD0)	Reserved	-	-	_	_	-	_	_	-	
(0xCF)	Reserved	-	-	_	_	-	_	_	-	
(0xCE)	Reserved	-	-	_	-	-	-	-	-	
(0xCD)	Reserved	-	_	-	-	_	-	_	-	
(0xCC)	Reserved	-	-	-	-	-	-	-	-	
(0xCB)	Reserved	-	-	_	_	-	_	_	-	
(0xCA)	Reserved	-	-	-	-	-	-	-	-	
(0xC9)	Reserved	-	_	_	-	-	_	-	-	
(0xC8)	Reserved	-	-	-	-	_	-	_	-	
(0xC7)	Reserved	-	-	-	-		_	_	-	
(0xC6)	UDR0				USART I/O	Data Register				195
(0xC5)	UBRR0H				LICART Device	ete Desirter I		Rate Register High	1	199
(0xC4)	UBRR0L					ate Register Low				199
(0xC3)	Reserved UCSR0C	- LIMSEL01	- LIMSELOO	UPM01	- LIPMOD	- LISBSU	LICEZO1 /LIDORDO	LICEZOO (LICELIA)	UCPOL0	197/212
(0xC2) (0xC1)	UCSR0C UCSR0B	UMSEL01 RXCIE0	UMSEL00 TXCIE0	UDRIE0	UPM00 RXEN0	USBS0 TXEN0	UCSZ01 /UDORD0 UCSZ02	UCSZ00 / UCPHA0 RXB80	TXB80	197/212
(0xC1)	UCSR0B UCSR0A	RXC0	TXC0	UDRE0	FE0	DOR0	UPE0	U2X0	MPCM0	195
(UXCU)	UCOKUA	KACU	IACU	UDKEU	I FEU	DOK0	UPEU	UZAU	IVIPCIVIU	195

# ■ ATmega48P/88P/168P/328P

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xBF)	Reserved	_	_	=	_	_	=	_	_	
(0xBE)	Reserved	_	_	_	_	_	_	_	_	
(0xBD)	TWAMR	TWAM6	TWAM5	TWAM4	TWAM3	TWAM2	TWAM1	TWAM0	_	245
(0xBC)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	=	TWIE	242
(0xBB)	TWDR			•	2-wire Serial Inter	face Data Regist	er			244
(0xBA)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	245
(0xB9)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	-	TWPS1	TWPS0	244
(0xB8)	TWBR				2-wire Serial Interfa	ice Bit Rate Regis	ster			242
(0xB7)	Reserved	=		_	=	-	-	-	_	
(0xB6)	ASSR	_	EXCLK	AS2	TCN2UB	OCR2AUB	OCR2BUB	TCR2AUB	TCR2BUB	164
(0xB5)	Reserved	-	-	_	_	-	-	-	_	
(0xB4)	OCR2B			Tir	ner/Counter2 Outpo	ut Compare Regis	ster B			162
(0xB3)	OCR2A			Tir	mer/Counter2 Outp	ut Compare Regi	ster A			162
(0xB2)	TCNT2		1	1	Timer/Cou	nter2 (8-bit)	1	•		162
(0xB1)	TCCR2B	FOC2A	FOC2B	-	-	WGM22	CS22	CS21	CS20	161
(0xB0)	TCCR2A	COM2A1	COM2A0	COM2B1	COM2B0	-	-	WGM21	WGM20	158
(0xAF)	Reserved	-	-	-	-	-	-	-	-	
(0xAE)	Reserved	-	-	-	-	-	-	-	-	
(0xAD)	Reserved	-	-	-	-	-	-	-	-	
(0xAC)	Reserved	-	-	-	-	-	-	-	-	
(0xAB)	Reserved	-	-	_	-	-	-	-	-	
(0xAA)	Reserved	_	_	_	-	_	_	_	_	
(0xA9)	Reserved	_	-	_	-	-	-	_	-	
(0xA8)	Reserved	_	-	-	_	-	-	_	-	
(0xA7)	Reserved	_	-	-	_	-	-		-	
(0xA6)	Reserved	-	-	-	-	-	-	-	-	
(0xA5)	Reserved	-	-	-	-	-	-	-	-	
(0xA4)	Reserved	-	-	-	-	-	-	_	-	
(0xA3)	Reserved	_	_	-	_	_	_	_	-	
(0xA2)	Reserved	-	-	-	-	-	-	-	-	
(0xA1)	Reserved	-	-	-	-	-	-	-	-	
(0xA0)	Reserved	-	-	-	-	-	-	=	-	
(0x9F)	Reserved	-	-	_	_	_	-	=	-	
(0x9E)	Reserved	_	_	-	_	-	-	_	-	
(0x9D)	Reserved	_	_	-	_	=	_	=	_	
(0x9C)	Reserved	_	_	_	_	_	_	_	_	
(0x9B)	Reserved	_		_	_	_	_		_	
(0x9A) (0x99)	Reserved Reserved	_	_	_		_	_	_	_	
(0x98)	Reserved	_	_	_	_		_		_	
(0x97)	Reserved	_	_	_			_		_	
(0x96)	Reserved	_							_	
(0x95)	Reserved	_	_	_	_	_	_		_	
(0x94)	Reserved	_							_	
(0x93)	Reserved	_	_	_	_				_	
(0x92)	Reserved	_	_	_	_	_	_		_	
(0x91)	Reserved	_	_						_	
(0x90)	Reserved	_	_	_	_	_	_		_	
(0x8F)	Reserved	_	_	_	_	_	_	_	_	
(0x8E)	Reserved	_	_	_	_	_	_	_	_	
(0x8D)	Reserved	_	_	_	-	-	-	-	-	
(0x8C)	Reserved	_	_	_	-	-	-	-	-	
(0x8B)	OCR1BH				ounter1 - Output Co					138
(0x8A)	OCR1BL				ounter1 - Output Co					138
(0x89)	OCR1AH				ounter1 - Output Co					138
(0x88)	OCR1AL				ounter1 - Output Co					138
(0x87)	ICR1H				/Counter1 - Input C					139
(0x86)	ICR1L				/Counter1 - Input C					139
(0x85)	TCNT1H				ner/Counter1 - Cou					138
(0x84)	TCNT1L				ner/Counter1 - Cou		•			138
(0x83)	Reserved	-	_	_	_	_	_	-	-	
(0x82)	TCCR1C	FOC1A	FOC1B		-	-	-	-	_	137
(0x81)	TCCR1B	ICNC1	ICES1	_	WGM13	WGM12	CS12	CS11	CS10	136
(0x80)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	-	-	WGM11	WGM10	134
(0x7F)	DIDR1	=	=	=	-	-	-	AIN1D	AIN0D	250
(0x7E)	DIDR0	_	_	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D	267





Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0x7D)	Reserved	_	_	_	_	_	_	_	_	
(0x7C)	ADMUX	REFS1	REFS0	ADLAR	_	MUX3	MUX2	MUX1	MUX0	263
(0x7B)	ADCSRB	_	ACME	_	_	_	ADTS2	ADTS1	ADTS0	266
(0x7A)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	264
(0x79)	ADCH				ADC Data Reg	gister High byte				266
(0x78)	ADCL			ı	ADC Data Re	gister Low byte	ı	ı		266
(0x77)	Reserved	-	-	-	-	_	-	-	-	
(0x76)	Reserved	_	_	_	_	_	_	_	-	
(0x75) (0x74)	Reserved Reserved		_		_	_	_		_	
(0x74)	Reserved	_	_	_	_	_	_	_	_	
(0x72)	Reserved	_	_	_	_	_	_	_	_	
(0x71)	Reserved	-	-	-	_	_	-	-	-	
(0x70)	TIMSK2	_	_	_	_	_	OCIE2B	OCIE2A	TOIE2	163
(0x6F)	TIMSK1	-	-	ICIE1	-	-	OCIE1B	OCIE1A	TOIE1	139
(0x6E)	TIMSK0	_	-	-	_	_	OCIE0B	OCIE0A	TOIE0	111
(0x6D)	PCMSK2	PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16	74
(0x6C)	PCMSK1	-	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	74
(0x6B)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	74
(0x6A)	Reserved	_	_	_	_	- ISC11	- ISC10	- ISC01	-	74
(0x69) (0x68)	EICRA PCICR	_	_	_	_	ISC11	ISC10 PCIE2	ISC01 PCIE1	ISC00 PCIE0	71
(0x67)	Reserved	_	_	_	_	_	-	-	-	
(0x66)	OSCCAL				Oscillator Calib	oration Register				37
(0x65)	Reserved	-	-	-	_	_	-	-	_	-
(0x64)	PRR	PRTWI	PRTIM2	PRTIM0	_	PRTIM1	PRSPI	PRUSART0	PRADC	42
(0x63)	Reserved	-	-	-	-	-	-	-	-	
(0x62)	Reserved	-	-	-	-	-	-	-	-	
(0x61)	CLKPR	CLKPCE	-	-	_	CLKPS3	CLKPS2	CLKPS1	CLKPS0	37
(0x60)	WDTCSR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	54
0x3F (0x5F)	SREG	  -	T _	H -	S -	V	(OD40) 5	Z	C	9
0x3E (0x5E) 0x3D (0x5D)	SPH SPL	SP7	SP6	SP5	SP4	SP3	(SP10) <sup>5.</sup> SP2	SP9 SP1	SP8 SP0	12 12
0x3C (0x5C)	Reserved	- JF 1	- -	- -	- -	- -	- -	- -	- -	12
0x3B (0x5B)	Reserved	_	_	_	_	_	_	_	_	
0x3A (0x5A)	Reserved	_	-	_	_	_	_	_	_	
0x39 (0x59)	Reserved	-	-	-	-	-	-	-	-	
0x38 (0x58)	Reserved	-	-	-	-	-	-	-	-	
0x37 (0x57)	SPMCSR	SPMIE	(RWWSB) <sup>5.</sup>	-	(RWWSRE) <sup>5.</sup>	BLBSET	PGWRT	PGERS	SELFPRGEN	293
0x36 (0x56)	Reserved	-	-		-	_	-	-	-	
0x35 (0x55)	MCUCR	-	BODS	BODSE	PUD	- WDDE	_ 	IVSEL	IVCE	44/68/92
0x34 (0x54) 0x33 (0x53)	MCUSR SMCR	-	_	_	_	WDRF SM2	BORF SM1	EXTRF SM0	PORF SE	54 40
0x32 (0x52)	Reserved	_		_	_	- SIVIZ	- OIVI I	- SIVIO	- -	40
0x31 (0x51)	Reserved	_	_	_	_	_	_	_	_	
0x30 (0x50)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	248
0x2F (0x4F)	Reserved	-	-	-	_	-	-	-	_	
0x2E (0x4E)	SPDR				SPI Data	Register				175
0x2D (0x4D)	SPSR	SPIF	WCOL	-	-	-	-	-	SPI2X	174
0x2C (0x4C)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	173
0x2B (0x4B)	GPIOR2	1				se I/O Register 2				25
0x2A (0x4A)	GPIOR1					se I/O Register 1				25
0x29 (0x49) 0x28 (0x48)	Reserved OCR0B	-	-	– Ti	mer/Counter0 Outp	ut Compare Pegi	- eter R	-	-	
0x28 (0x48) 0x27 (0x47)	OCR0B OCR0A	1			mer/Counter0 Outp					
0x26 (0x46)	TCNT0					nter0 (8-bit)				
0x25 (0x45)	TCCR0B	FOC0A	FOC0B	-	-	WGM02	CS02	CS01	CS00	
0x24 (0x44)	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	-	-	WGM01	WGM00	
0x23 (0x43)	GTCCR	TSM	-	-	_	-	-	PSRASY	PSRSYNC	143/165
0x22 (0x42)	EEARH			(1	EEPROM Address	Register High Byt	e) <sup>5.</sup>			21
0x21 (0x41)	EEARL				EEPROM Address		te			21
0x20 (0x40)	EEDR			ı		ata Register		ı	1	21
0x1F (0x3F)	EECR	-	_	EEPM1	EEPM0	EERIE	EEMPE	EEPE	EERE	21
0x1E (0x3E)	GPIOR0				General Purpos	se I/O Register 0		INITA	INTO	25
0x1D (0x3D)	EIMSK	-	-	-	-	=	-	INT1	INTO	72 72
0x1C (0x3C)	EIFR	_	_	_	_	_	_	INTF1	INTF0	12

# ATmega48P/88P/168P/328P

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x1B (0x3B)	PCIFR	-	-	-	-	-	PCIF2	PCIF1	PCIF0	
0x1A (0x3A)	Reserved	-	-	-	-	-	-	-	-	
0x19 (0x39)	Reserved	-	-	-	-	-	-	-	-	
0x18 (0x38)	Reserved	-	_	_	_	-	_	-	-	
0x17 (0x37)	TIFR2	-	-	-	-	-	OCF2B	OCF2A	TOV2	163
0x16 (0x36)	TIFR1	-	_	ICF1	-	-	OCF1B	OCF1A	TOV1	140
0x15 (0x35)	TIFR0	-	_	_	_	-	OCF0B	OCF0A	TOV0	
0x14 (0x34)	Reserved	-	-	-	-	-	-	-	-	
0x13 (0x33)	Reserved	-	-	-	-	-	-	-	-	
0x12 (0x32)	Reserved	-	_	-	-	-	-	-	-	
0x11 (0x31)	Reserved	-	-	-	-	-	-	-	-	
0x10 (0x30)	Reserved	-	-	-	-	-	-	-	-	
0x0F (0x2F)	Reserved	-	_	-	-	-	-	-	-	
0x0E (0x2E)	Reserved	-	-	-	-	-	-	-	-	
0x0D (0x2D)	Reserved	-	-	-	-	П	-	П	-	
0x0C (0x2C)	Reserved	-	_	_	_	-	_	-	-	
0x0B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	93
0x0A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	93
0x09 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	93
0x08 (0x28)	PORTC	-	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	92
0x07 (0x27)	DDRC	-	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	92
0x06 (0x26)	PINC	-	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	92
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	92
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	92
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	92
0x02 (0x22)	Reserved	-	_	-	_	-	-	-	_	
0x01 (0x21)	Reserved	-	_	-	_	-	-	_	_	
0x0 (0x20)	Reserved	-	-	-	-	_	-	-	-	

- 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
- 2. I/O Registers within the address range 0x00 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
- 3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
- 4. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses. The ATmega48P/88P/168P/328P is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 0xFF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.
- 5. Only valid for ATmega88P/168P.





# 6. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND I	LOGIC INSTRUCTIONS	3		•	
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \bullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
COM	Rd	One's Complement	Rd ← 0xFF – Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← 0x00 – Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (0xFF - K)$	Z,N,V	1
INC	Rd Rd	Increment	$Rd \leftarrow Rd + 1$ $Rd \leftarrow Rd - 1$	Z,N,V	1
DEC TST	Rd	Decrement Test for Zero or Minus	$Rd \leftarrow Rd - 1$ $Rd \leftarrow Rd \bullet Rd$	Z,N,V Z,N,V	1
	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
CLR SER	Rd	Set Register	$Rd \leftarrow Rd \oplus Rd$ $Rd \leftarrow 0xFF$	Z,N,V None	1
MUL	Rd, Rr	Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULS	Rd, Rr	Multiply Signed	R1:R0 ← Rd x Rr	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	$R1:R0 \leftarrow (Rd \times Rr) << 1$	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	$R1:R0 \leftarrow (Rd \times Rr) << 1$	Z,C	2
BRANCH INSTRUC		Traditional manaphy digitod man distinguish	Kinto ( (taxia) 111	1 2,0	-
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC ← Z	None	2
JMP <sup>(1)</sup>	k	Direct Jump	PC ← k	None	3
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
ICALL		Indirect Call to (Z)	PC ← Z	None	3
CALL <sup>(1)</sup>	k	Direct Subroutine Call	PC ← k	None	4
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	1	4
CPSE	Rd,Rr	Compare, Skip if Equal	if $(Rd = Rr) PC \leftarrow PC + 2 \text{ or } 3$	None	1/2/3
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd - Rr - C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if $(Rr(b)=1) PC \leftarrow PC + 2 \text{ or } 3$	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if $(SREG(s) = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if $(Z = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
		·	# (C 4) #ham DC - DC - 1 4	Nama	
BRCS	k	Branch if Carry Set	if (C = 1) then PC $\leftarrow$ PC + k + 1	None	1/2
BRCC	k k	Branch if Carry Set Branch if Carry Cleared	if (C = 0) then PC $\leftarrow$ PC + k + 1	None	1/2
BRCC BRSH	k k k	Branch if Carry Set Branch if Carry Cleared Branch if Same or Higher	if (C = 0) then PC $\leftarrow$ PC + k + 1 if (C = 0) then PC $\leftarrow$ PC + k + 1	None None	1/2 1/2
BRCC BRSH BRLO	k k k	Branch if Carry Set Branch if Carry Cleared Branch if Same or Higher Branch if Lower	$\begin{split} &\text{if } (C=0) \text{ then } PC \leftarrow PC+k+1 \\ &\text{if } (C=0) \text{ then } PC \leftarrow PC+k+1 \\ &\text{if } (C=1) \text{ then } PC \leftarrow PC+k+1 \end{split}$	None None None	1/2 1/2 1/2
BRCC BRSH BRLO BRMI	k k k k	Branch if Carry Set Branch if Carry Cleared Branch if Same or Higher Branch if Lower Branch if Minus	if $(C = 0)$ then $PC \leftarrow PC + k + 1$ if $(C = 0)$ then $PC \leftarrow PC + k + 1$ if $(C = 1)$ then $PC \leftarrow PC + k + 1$ if $(N = 1)$ then $PC \leftarrow PC + k + 1$	None None None	1/2 1/2 1/2 1/2
BRCC BRSH BRLO BRMI BRPL	k k k k k	Branch if Carry Set Branch if Carry Cleared Branch if Same or Higher Branch if Lower Branch if Minus Branch if Plus	if $(C = 0)$ then $PC \leftarrow PC + k + 1$ if $(C = 0)$ then $PC \leftarrow PC + k + 1$ if $(C = 1)$ then $PC \leftarrow PC + k + 1$ if $(N = 1)$ then $PC \leftarrow PC + k + 1$ if $(N = 0)$ then $PC \leftarrow PC + k + 1$	None None None None	1/2 1/2 1/2 1/2 1/2
BRCC BRSH BRLO BRMI BRPL BRGE	k k k k k	Branch if Carry Set Branch if Carry Cleared Branch if Same or Higher Branch if Lower Branch if Minus Branch if Plus Branch if Greater or Equal, Signed	if (C = 0) then PC $\leftarrow$ PC + k + 1 if (C = 0) then PC $\leftarrow$ PC + k + 1 if (C = 1) then PC $\leftarrow$ PC + k + 1 if (N = 1) then PC $\leftarrow$ PC + k + 1 if (N = 0) then PC $\leftarrow$ PC + k + 1 if (N $\oplus$ V = 0) then PC $\leftarrow$ PC + k + 1	None None None None None None None	1/2 1/2 1/2 1/2 1/2 1/2
BRCC BRSH BRLO BRMI BRPL BRGE BRLT	k k k k k k	Branch if Carry Set Branch if Carry Cleared Branch if Same or Higher Branch if Lower Branch if Minus Branch if Plus Branch if Greater or Equal, Signed Branch if Less Than Zero, Signed	if (C = 0) then PC $\leftarrow$ PC + k + 1 if (C = 0) then PC $\leftarrow$ PC + k + 1 if (C = 1) then PC $\leftarrow$ PC + k + 1 if (N = 1) then PC $\leftarrow$ PC + k + 1 if (N = 0) then PC $\leftarrow$ PC + k + 1 if (N $\oplus$ V = 0) then PC $\leftarrow$ PC + k + 1 if (N $\oplus$ V = 1) then PC $\leftarrow$ PC + k + 1	None None None None None None None None	1/2 1/2 1/2 1/2 1/2 1/2 1/2 1/2
BRCC BRSH BRLO BRMI BRPL BRGE BRLT BRHS	k k k k k k k k k k k k k k k k k k k	Branch if Carry Set Branch if Carry Cleared Branch if Same or Higher Branch if Lower Branch if Minus Branch if Plus Branch if Greater or Equal, Signed Branch if Less Than Zero, Signed Branch if Half Carry Flag Set	if (C = 0) then PC $\leftarrow$ PC + k + 1 if (C = 0) then PC $\leftarrow$ PC + k + 1 if (C = 1) then PC $\leftarrow$ PC + k + 1 if (N = 1) then PC $\leftarrow$ PC + k + 1 if (N = 0) then PC $\leftarrow$ PC + k + 1 if (N $\oplus$ V = 0) then PC $\leftarrow$ PC + k + 1 if (N $\oplus$ V = 1) then PC $\leftarrow$ PC + k + 1 if (H $\oplus$ V = 1) then PC $\leftarrow$ PC + k + 1	None None None None None None None None	1/2 1/2 1/2 1/2 1/2 1/2 1/2 1/2 1/2 1/2
BRCC BRSH BRLO BRMI BRPL BRGE BRLT BRHS BRHC	k k k k k k k k k k	Branch if Carry Set Branch if Carry Cleared Branch if Same or Higher Branch if Lower Branch if Minus Branch if Plus Branch if Greater or Equal, Signed Branch if Less Than Zero, Signed Branch if Half Carry Flag Set Branch if Half Carry Flag Cleared	if (C = 0) then PC $\leftarrow$ PC + k + 1 if (C = 0) then PC $\leftarrow$ PC + k + 1 if (C = 1) then PC $\leftarrow$ PC + k + 1 if (N = 1) then PC $\leftarrow$ PC + k + 1 if (N = 0) then PC $\leftarrow$ PC + k + 1 if (N $\oplus$ V = 0) then PC $\leftarrow$ PC + k + 1 if (N $\oplus$ V = 1) then PC $\leftarrow$ PC + k + 1 if (H = 1) then PC $\leftarrow$ PC + k + 1 if (H = 0) then PC $\leftarrow$ PC + k + 1	None None None None None None None None	1/2 1/2 1/2 1/2 1/2 1/2 1/2 1/2 1/2 1/2
BRCC BRSH BRLO BRMI BRPL BRGE BRLT BRHS BRHC BRTS	k k k k k k k k k k k	Branch if Carry Set Branch if Carry Cleared Branch if Same or Higher Branch if Lower Branch if Minus Branch if Plus Branch if Greater or Equal, Signed Branch if Less Than Zero, Signed Branch if Half Carry Flag Set Branch if Half Carry Flag Cleared Branch if T Flag Set	if (C = 0) then PC $\leftarrow$ PC + k + 1 if (C = 0) then PC $\leftarrow$ PC + k + 1 if (C = 1) then PC $\leftarrow$ PC + k + 1 if (N = 1) then PC $\leftarrow$ PC + k + 1 if (N = 0) then PC $\leftarrow$ PC + k + 1 if (N $\oplus$ V= 0) then PC $\leftarrow$ PC + k + 1 if (N $\oplus$ V= 1) then PC $\leftarrow$ PC + k + 1 if (H = 1) then PC $\leftarrow$ PC + k + 1 if (H = 0) then PC $\leftarrow$ PC + k + 1 if (T = 1) then PC $\leftarrow$ PC + k + 1	None None None None None None None None	1/2 1/2 1/2 1/2 1/2 1/2 1/2 1/2 1/2 1/2
BRCC BRSH BRLO BRMI BRPL BRGE BRLT BRHS BRHC	k k k k k k k k k k	Branch if Carry Set Branch if Carry Cleared Branch if Same or Higher Branch if Lower Branch if Minus Branch if Plus Branch if Greater or Equal, Signed Branch if Less Than Zero, Signed Branch if Half Carry Flag Set Branch if Half Carry Flag Cleared	if (C = 0) then PC $\leftarrow$ PC + k + 1 if (C = 0) then PC $\leftarrow$ PC + k + 1 if (C = 1) then PC $\leftarrow$ PC + k + 1 if (N = 1) then PC $\leftarrow$ PC + k + 1 if (N = 0) then PC $\leftarrow$ PC + k + 1 if (N $\oplus$ V = 0) then PC $\leftarrow$ PC + k + 1 if (N $\oplus$ V = 1) then PC $\leftarrow$ PC + k + 1 if (H = 1) then PC $\leftarrow$ PC + k + 1 if (H = 0) then PC $\leftarrow$ PC + k + 1	None None None None None None None None	1/2 1/2 1/2 1/2 1/2 1/2 1/2 1/2 1/2 1/2

# ■ ATmega48P/88P/168P/328P

Mnemonics	Operands	Description	Operation	Flags	#Clocks
BRIE	k	Branch if Interrupt Enabled	if ( I = 1) then PC ← PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if ( I = 0) then PC ← PC + k + 1	None	1/2
BIT AND BIT-TEST	INSTRUCTIONS				
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	$I/O(P,b) \leftarrow 0$	None	2
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z,C,N,V	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	$Rd(0)\leftarrow C,Rd(n+1)\leftarrow Rd(n),C\leftarrow Rd(7)$	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	$Rd(7)\leftarrow C,Rd(n)\leftarrow Rd(n+1),C\leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n=06$	Z,C,N,V	1
SWAP BSET	Rd s	Swap Nibbles Flag Set	$Rd(30) \leftarrow Rd(74), Rd(74) \leftarrow Rd(30)$ $SREG(s) \leftarrow 1$	None SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	C←1	С	1
CLC		Clear Carry	C ← 0	С	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	1	1
CLI		Global Interrupt Disable	1←0	1	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S V	1
SEV CLV		Set Twos Complement Overflow.  Clear Twos Complement Overflow	V ← 1 V ← 0	V	1 1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	Ť	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H←0	Н	1
DATA TRANSFER I	NSTRUCTIONS			•	•
MOV	Rd, Rr	Move Between Registers	$Rd \leftarrow Rr$	None	1
MOVW	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	$Rd \leftarrow K$	None	1
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	$X \leftarrow X - 1$ , $Rd \leftarrow (X)$	None	2
LD	Rd, Y	Load Indirect	$Rd \leftarrow (Y)$	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	$Rd \leftarrow (Y), Y \leftarrow Y + 1$	None	2
LDD	Rd, - Y Rd,Y+q	Load Indirect with Displacement	$Y \leftarrow Y - 1$ , $Rd \leftarrow (Y)$	None None	2 2
LD	Rd, Z	Load Indirect with Displacement  Load Indirect	$Rd \leftarrow (Y + q)$ $Rd \leftarrow (Z)$	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	$Rd \leftarrow (Z), Z \leftarrow Z+1$	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	$Z \leftarrow Z - 1$ , $Rd \leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	$(X) \leftarrow Rr, X \leftarrow X + 1$	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	$X \leftarrow X - 1, (X) \leftarrow Rr$	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	$Y \leftarrow Y - 1, (Y) \leftarrow Rr$	None	2
STD	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2 2
ST	Z, Rr	Store Indirect Store Indirect and Post-Inc.	$(Z) \leftarrow Rr$	None	2
ST	Z+, Rr -Z, Rr	Store Indirect and Post-Inc.  Store Indirect and Pre-Dec.	$(Z) \leftarrow Rr, Z \leftarrow Z + 1$ $Z \leftarrow Z - 1, (Z) \leftarrow Rr$	None None	2
STD	Z+q,Rr	Store Indirect with Displacement	$(Z+q) \leftarrow Rr$	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM	,	Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	$Rd \leftarrow (Z), Z \leftarrow Z+1$	None	3
SPM		Store Program Memory	(Z) ← R1:R0	None	-
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2





Mnemonics	Operands	Description	Operation	Flags	#Clocks
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
MCU CONTROL INS	TRUCTIONS				
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

Note: 1. These instructions are only available in ATmega168P and ATmega328P.

# 7. Ordering Information

# 7.1 ATmega48P

Speed (MHz)	Power Supply	Ordering Code <sup>(2)</sup>	Package <sup>(1)</sup>	Operational Range
		ATmega48PV-10AU	32A	
10 <sup>(3)</sup>	1.8 - 5.5	ATmega48PV-10MMU	28M1	Industrial
10(9)		ATmega48PV-10MU	32M1-A	(-40°C to 85°C)
		ATmega48PV-10PU	28P3	
	2.7 - 5.5	ATmega48P-20AU	32A	
20 <sup>(3)</sup>		ATmega48P-20MMU	28M1	Industrial
		ATmega48P-20MU	32M1-A	(-40°C to 85°C)
		ATmega48P-20PU	28P3	

- 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
- 2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
- 3. See Figure 28-1 on page 317 and Figure 28-2 on page 318.

	Package Type
32A	32-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
28M1	28-pad, 4 x 4 x 1.0 body, Lead Pitch 0.45 mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
32M1-A	32-pad, 5 x 5 x 1.0 body, Lead Pitch 0.50 mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
28P3	28-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)





# 7.2 ATmega88P

Speed (MHz)	Power Supply	Ordering Code <sup>(2)</sup>	Package <sup>(1)</sup>	Operational Range
10 <sup>(3)</sup>	1.8 - 5.5	ATmega88PV-10AU ATmega88PV-10MU ATmega88PV-10PU	32A 32M1-A 28P3	Industrial (-40°C to 85°C)
20 <sup>(3)</sup>	2.7 - 5.5	ATmega88P-20AU ATmega88P-20MU ATmega88P-20PU	32A 32M1-A 28P3	Industrial (-40°C to 85°C)

- 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
- 2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
- 3. See Figure 28-1 on page 317 and Figure 28-2 on page 318.

	Package Type
32A	32-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
28P3	28-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
32M1-A	32-pad, 5 x 5 x 1.0 body, Lead Pitch 0.50 mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

# 7.3 ATmega168P

Speed (MHz) <sup>(3)</sup>	Power Supply	Ordering Code <sup>(2)</sup>	Package <sup>(1)</sup>	Operational Range
10	1.8 - 5.5	ATmega168PV-10AU ATmega168PV-10MU ATmega168PV-10PU	32A 32M1-A 28P3	Industrial (-40°C to 85°C)
20	2.7 - 5.5	ATmega168P-20AU ATmega168P-20MU ATmega168P-20PU	32A 32M1-A 28P3	Industrial (-40°C to 85°C)

- 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
- 2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
- 3. See Figure 28-1 on page 317 and Figure 28-2 on page 318.

Package Type				
32A	32-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)			
28P3	28-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)			
32M1-A	32-pad, 5 x 5 x 1.0 body, Lead Pitch 0.50 mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)			





# 7.4 ATmega328P

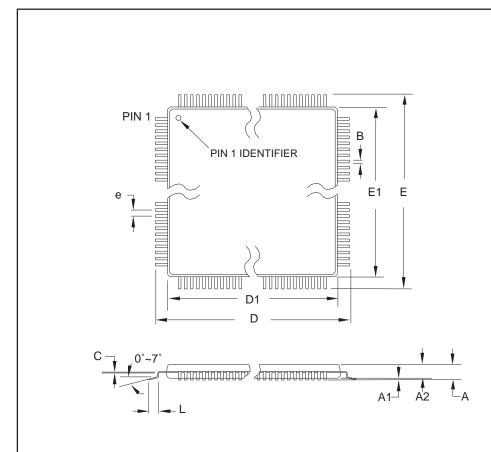
Speed (MHz) <sup>(3)</sup>	Power Supply	Ordering Code <sup>(2)</sup>	Package <sup>(1)</sup>	Operational Range
20	1.8 - 5.5	ATmega328P- AU ATmega328P- MU ATmega328P- PU	32A 32M1-A 28P3	Industrial (-40°C to 85°C)

- 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
- 2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
- 3. See Figure 28-3 on page 318.

Package Type				
32A	32-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)			
28P3	28-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)			
32M1-A	32-pad, 5 x 5 x 1.0 body, Lead Pitch 0.50 mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)			

# 8. Packaging Information

#### 8.1 32A



# COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
Α	_	_	1.20	
A1	0.05	-	0.15	
A2	0.95	1.00	1.05	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
Е	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
В	0.30	_	0.45	
С	0.09	_	0.20	
L	0.45	_	0.75	
е	0.80 TYP			

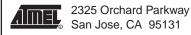
 Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.

TITLE

1. This package conforms to JEDEC reference MS-026, Variation ABA.

3. Lead coplanarity is 0.10 mm maximum.

10/5/2001



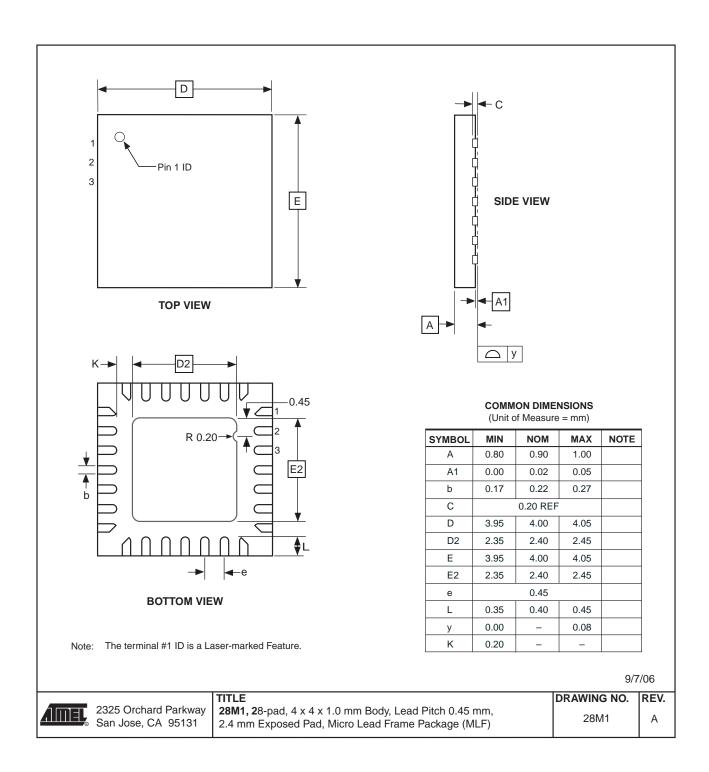
**32A,** 32-lead, 7 x 7 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

DRAWING NO.	REV.	
32A	В	

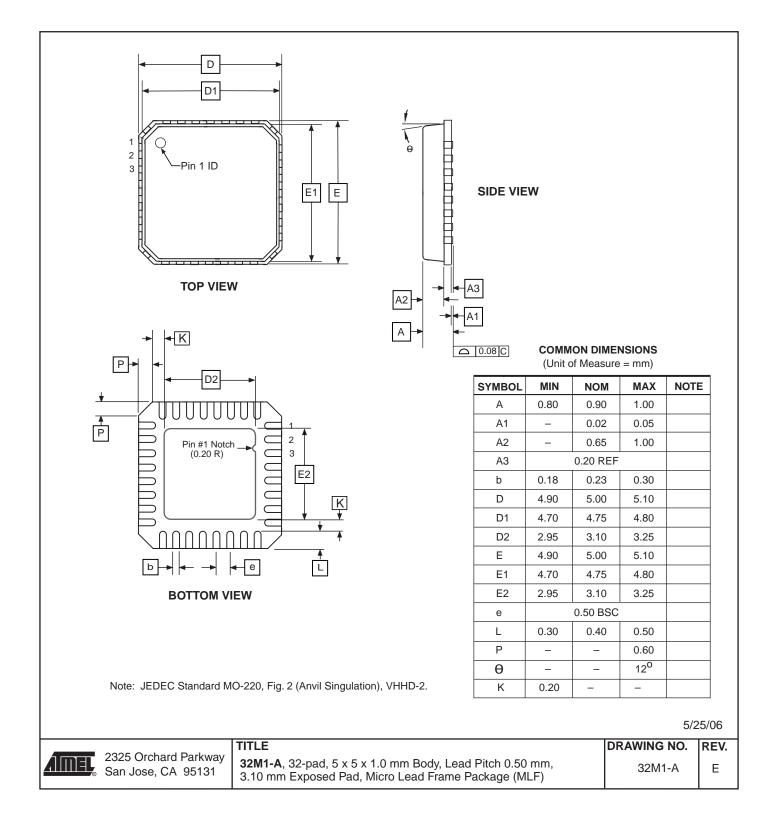




# 8.2 28M1



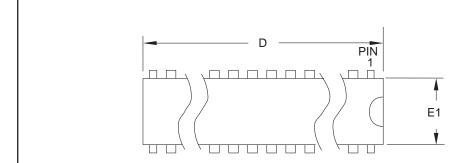
#### 8.3 32M1-A

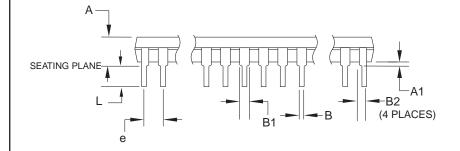


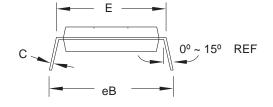




#### 8.4 28P3







1. Dimensions D and E1 do not include mold Flash or Protrusion. Note: Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

# **COMMON DIMENSIONS**

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
А	_	_	4.5724	
A1	0.508	_	_	
D	34.544	_	34.798	Note 1
Е	7.620	_	8.255	
E1	7.112	_	7.493	Note 1
В	0.381	_	0.533	
B1	1.143	_	1.397	
B2	0.762	_	1.143	
L	3.175	_	3.429	
С	0.203	_	0.356	
eВ	_	_	10.160	
е	2.540 TYP			

09/28/01



2325 Orchard Parkway San Jose, CA 95131

TITLE **28P3**, 28-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP) DRAWING NO. REV. 28P3

В

## 9. Errata

# 9.1 Errata ATmega48P

The revision letter in this section refers to the revision of the ATmega48P device.

9.1.1 Rev. B

No known errata.

9.1.2 Rev. A

Not Sampled.

## 9.2 Errata ATmega88P

The revision letter in this section refers to the revision of the ATmega88P device.

9.2.1 Rev. A

No known errata.

#### 9.3 Errata ATmega168P

The revision letter in this section refers to the revision of the ATmega168P device.

9.3.1 Rev A

No known errata.

### 9.4 Errata ATmega328P

The revision letter in this section refers to the revision of the ATmega328P device.

#### 9.4.1 Rev B

Unstable 32 kHz Oscillator

#### 1. Unstable 32 kHz Oscillator

The 32 kHz oscillator does not work as system clock.

The 32 kHz oscillator used as asynchronous timer is inaccurate.

#### **Problem Fix/ Workaround**

None

#### 9.4.2 Rev A

No known errata.





# 10. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

#### 10.1 Rev. 2545F-08/08

- Updated "ATmega328P Typical Characteristics" on page 401 with Power-save numbers.
- 2. Added ATmega328P "Standby Supply Current" on page 408.

#### 10.2 Rev. 2545E-08/08

- Updated description of "Stack Pointer" on page 12.
- 2. Updated description of use of external capacitors in "Low Frequency Crystal Oscillator" on page 32.
- 3. Updated Table 8-9 in "Low Frequency Crystal Oscillator" on page 32.
- 4. Added note to "Address Match Unit" on page 222.
- 5. Added section "Reading the Signature Row from Software" on page 286.
- 6. Updated "Program And Data Memory Lock Bits" on page 295 to include ATmega328P in the description.
- 7. Added "ATmega328P DC Characteristics" on page 317.
- 8. Updated "Speed Grades" on page 317 for ATmega328P.
- 9. Removed note 6 and 7 from the table "2-wire Serial Interface Characteristics" on page 323.
- 10. Added figure "Minimum Reset Pulse width vs. V<sub>CC</sub>." on page 352 for ATmega48P.
- 11. Added figure "Minimum Reset Pulse width vs. V<sub>CC</sub>." on page 376 for ATmega88P.
- 12. Added figure "Minimum Reset Pulse width vs. V<sub>CC</sub>." on page 400 for ATmega168P.
- 13. Added "ATmega328P Typical Characteristics" on page 401.
- 14. Updated Ordering Information for "ATmega328P" on page 18.

#### 10.3 Rev. 2545D-03/08

- Updated figures in "Speed Grades" on page 317.
- 2. Updated note in Table 28-4 in "System and Reset Characteristics" on page 320.
- 3. Ordering codes for "ATmega328P" on page 18 updated.
  - ATmega328P is offered in 20 MHz option only.
- 4. Added Errata for ATmega328P rev. B, "Errata ATmega328P" on page 23.

#### 10.4 Rev. 2545C-01/08

1. Power-save Maximum values removed form "ATmega48P DC Characteristics" on page 315, "ATmega88P DC Characteristics" on page 316, and "ATmega168P DC Characteristics" on page 316.

### 10.5 Rev. 2545B-01/08

- 1. Updated "Features" on page 1.
- 2. Added "Data Retention" on page 7.
- 3. Updated Table 8-2 on page 28.
- 4. Removed "Low-frequency Crystal Oscillator Internal Load Capacitance" table from "Low Frequency Crystal Oscillator" on page 32.
- 5. Removed JTD bit from "MCUCR MCU Control Register" on page 44.
  - Updated typical and general program setup for Reset and Interrupt Vector Addresses
- 6. in "Interrupt Vectors in ATmega168P" on page 62 and "Interrupt Vectors in ATmega328P" on page 65.
- 7. Updated Interrupt Vectors Start Address in Table 11-5 on page 63 and Table 11-7 on page 66.
- 8. Updated "Temperature Measurement" on page 262.
- 9. Updated ATmega328P "Fuse Bits" on page 296.
- 10. Removed V<sub>OL3</sub>/V<sub>OH3</sub> rows from "DC Characteristics" on page 314.
- 11. Updated condition for  $V_{OL}$  in "DC Characteristics" on page 314. Updated max value for  $V_{IL2}$  in "DC Characteristics" on page 314.
- Added "ATmega48P DC Characteristics" on page 315, "ATmega88P DC Characteristics" on page 316, and "ATmega168P DC Characteristics" on page 316.
- 13. Updated "System and Reset Characteristics" on page 320.
  - Added "ATmega48P Typical Characteristics" on page 329, "ATmega88P Typical
- 14. Characteristics" on page 353, and "ATmega168P Typical Characteristics" on page 377.
- 15. Updated note in "Instruction Set Summary" on page 12.

#### 10.6 Rev. 2545A-07/07

1. Initial revision.





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