Real-Time Simulation of HVDC Systems with eMEGAsim

THIRD EDITION

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Executive Summary

This document provides users with benchmark models to evaluate the **OPAL-RT Technologies** system configuration needed to develop research models for the following three HVDC transmission systems:

- Bipolar HVDC model,
- Monopolar back-to-back HVDC system based on the First CIGRE benchmark for HVDC control studies [1], and
- Multi-Terminal HVDC System.

Simulation results with additional comments are provided to demonstrate the feasibility of these models.

The studied systems are modeled in an environment that integrates **Simulink/SimPowerSystems** (SPS) with the **eMEGAsim** simulation platform, which incorporates the **ARTEMiS** software for solving of the real-time simulated model and the **RTeDrive** and **RT-Events** blocksets. This platform enables the simulation of increasingly large systems with real-time performance across multiple CPUs.

Through the use of the **TestDrive** graphical user interface platform from **OPAL-RT Technologies**, it is also demonstrated that observing results and modifying parameters and conditions on a real-time simulated model is both easy and user friendly.

Publication Information

Table of Contents

Table of figures

1. Bipolar HVDC System

This model is a 12-pulse bipolar HVDC system (Figure 1). It was inspired by a demonstration example found in the **SimPowerSystems** examples library [2]. The model is based on a 1000 MW (±500 kV, 1 kA per pole) DC link which is used to transmit power from a 500 kV, 5000 MVA, 60 Hz network with Short Circuit Ratio (SCR) of 5 to a 345 kV, 10000 MVA, 50 Hz network (with SCR of 10). Both poles operate independently of each other.

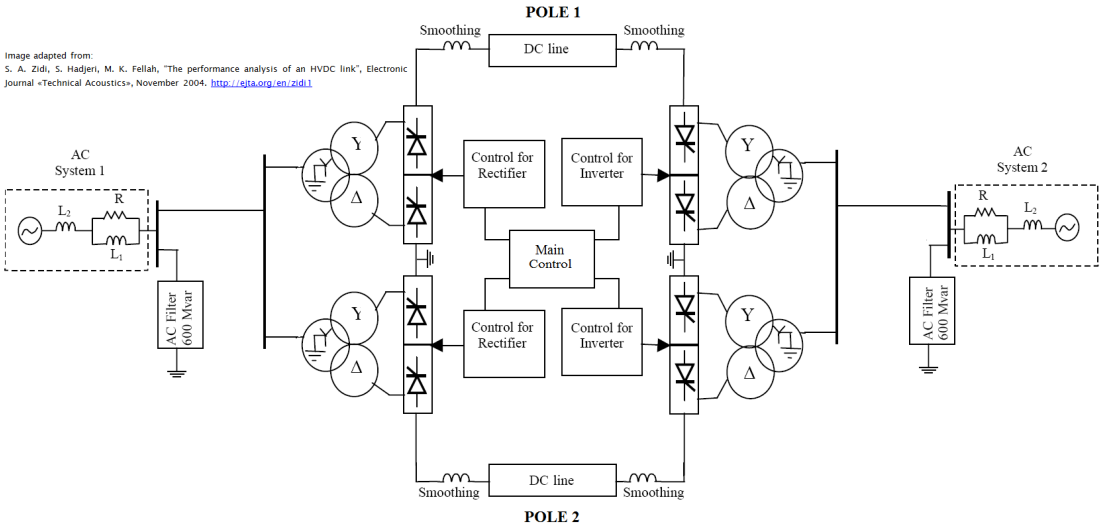

Figure 1- Bipolar HVDC Link.[1]

On the inverter side, a resonant RLC circuit is included to implement, if desired, a difficult operating condition to study controller interactions. This circuit is modeled without SPS allowing the inverter-side grid impedance Z, defined by short-circuit power, resonance frequency and damping to be continuously adjustable during run-time. This feature is illustrated in Figure 2, a print screen of the Graphical User Interface (GUI) built especially for the HVDC system. The GUI feature of the **eMEGAsim** simulator is further explained in section 1.5.

The rectifiers and inverters are composed of one 12-pulse converter per pole. The rectifiers and inverters are interconnected through 300 km lines (simulated as distributed parameter line models) and two 0.5 H smoothing reactors. The reactive power required by the converters is provided by a set of capacitor banks plus 11th, 13th and high-pass filters for a total of 600 MVar on each side. Two circuit breakers are also used to apply faults on the inverter AC side and rectifier DC side.

[1] Image adapted from [3]

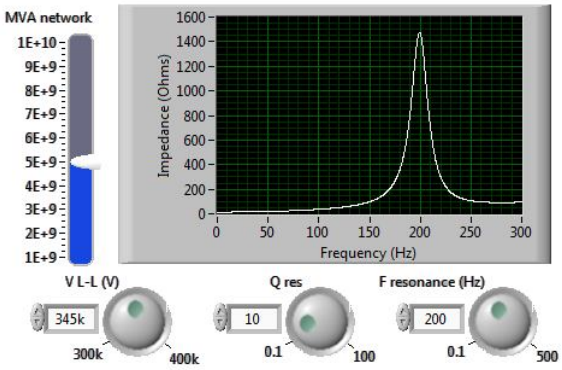

Figure 2 - Variation of the inverter-side network short-circuit power, voltage amplitude, resonance frequency and quality factor of the resonant Thevenin impedance

The rectifier and inverter control systems use a static Vdc-Idc characteristic similar to the one presented in [3]. DC Protection functions are implemented at each converter. At the rectifier, the DC fault protection will detect and force the delay angle into the inverter region so as to extinguish the DC fault current. At the inverter, the commutation failure prevention control will detect AC faults and reduce the maximum delay angle limit in order to decrease the risk of commutation failure(s). The Low AC voltage detection blocks will lock the DC fault protection when a reduction in the AC voltage is detected. The Master Control block initiates the starting/stopping of the converters as well as the ramping up/down of the respective current references. The controllers will be explained further in later sections. Additional details on the controls are available in [2].

1.1 Global HVDC Controls

The global command system in this HVDC model includes two levels of controls. The schematic diagram of the global HVDC controls implemented is illustrated in Figure 3.

A Master controller is used for global control of the HVDC System. First of all, it distributes the ramped current reference to each local controller, which permits a global command of the power transited by the HVDC link. It also includes a basic start-up and shutdown sequence that will ramp up and down the current reference and send blocking signals to local controls.

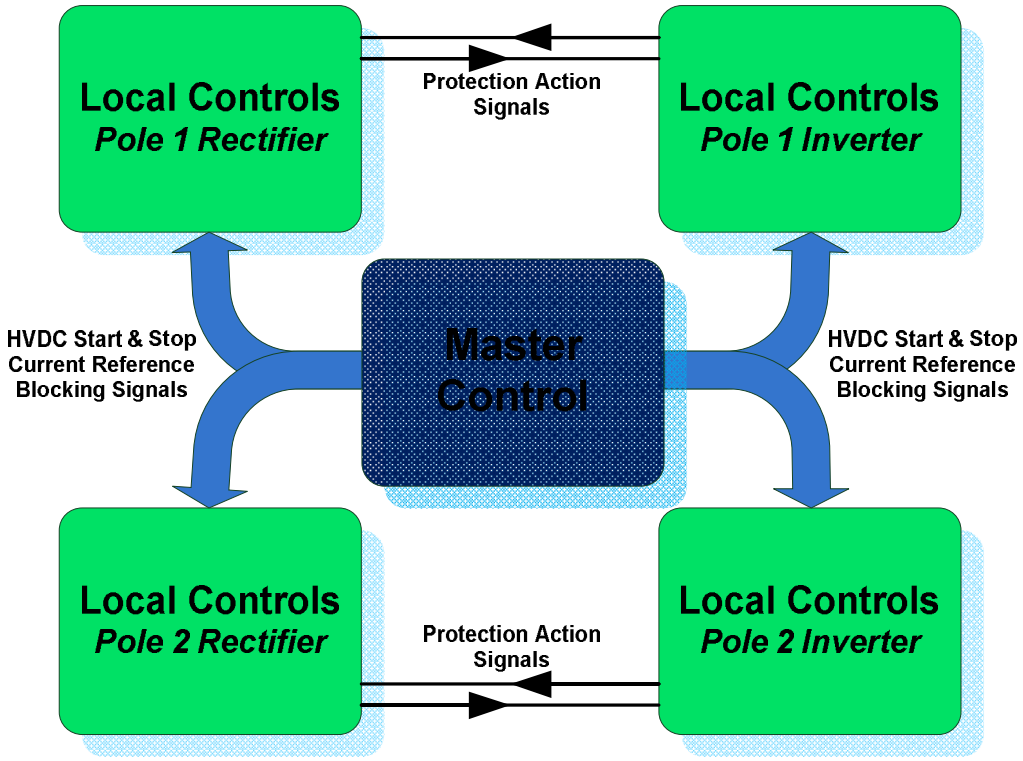

Figure 3 - Schematic Diagram of the Global HVDC Controls

The local controls include the regulators, the fault protection systems and the pulse generation units. The regulators are set to obtain the desired HVDC static characteristic and provide the pulse generation units with the alpha order for thyristor triggering. Each local control module has a set of fault detection blocks which send protective action signals to the regulators. Some of these protective action signals are also communicated between both local control units of the same pole. Each pulse generation unit works under the equidistant firing principle [4][5] and contains a Phase Locked Loop (PLL) to synchronize the firing sequences of a converter, based on the positive sequence component of the fundamental voltage. This unit has to be robust and stable for operation under harmonic perturbations.

The content of each controller unit is described in Table 1. The basic functionalities implemented in this model are sufficient for a majority of studies. It can also be used as a starting point to implement more complex HVDC control systems.

Table 1- Description of the HVDC Controllers Content

Control Group(s)		Functionalities
Master Control		• Start and Stop sequences • Reference Current sent to Local Controls (regulators)
Rectifier Local Controls	Regulators	• Constant DC Current Regulator • Forced Alpha angle control • VDCOL • Control Mode Monitoring
	Protections	• Low AC Voltage Detection • DC Fault Detection and Protection
	Pulse Generation Unit	• Phase Locked Loop • 12-pulse Generator
Inverter Local Controls	Regulators	• Constant DC Current Regulator • Constant DC Voltage Regulator • Gamma Minimum Regulator • Forced Alpha Angle Control • VDCOL • Control Mode Monitoring
	Monitoring	• Gamma Angle Measurement
	Protections	• Low AC Voltage Detection • Commutation Failure Prevention Control
	Pulse Generation Unit	• Phase Locked Loop • 12-pulse Generator

1.2 Regulator Fundamentals

1.2.1 Vdc-Idc Static Characteristic

In steady-state, the HVDC regulators in this model provide constant DC current at the rectifier end and constant DC voltage control at the inverter end [4][5][7][9]. Each pole regulates its DC current and voltage independently. To offer improved stability and recovery from faults, each inverter also has constant DC current and Gamma minimum regulators. Alternatively, the option of using voltage+current+Gamma or Gamma+current control at the inverter is also available [2]. However, in order to keep the inverter from regulating DC current under normal operating conditions, thereby permitting the rectifier controls to perform their tasks, a constant current margin (typically of 0.1 p.u.) is maintained between the current reference at the rectifier and at the inverter. The Vdc-Idc static characteristic is illustrated in Figure 4.

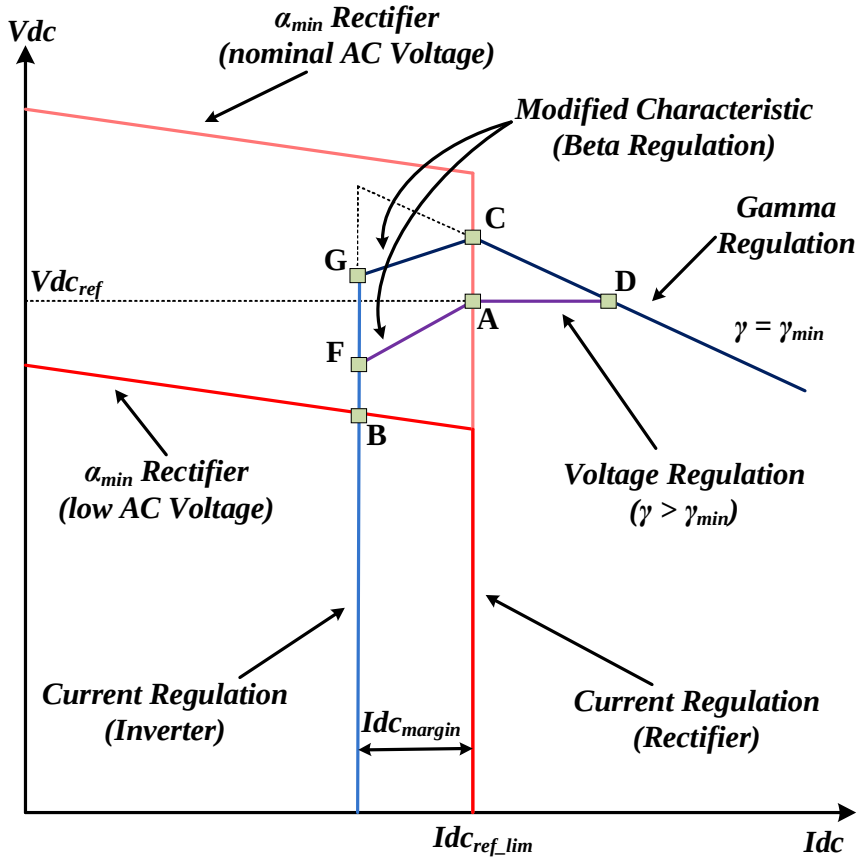

Figure 4 - HVDC Regulators Vdc-Idc Static Characteristic

With the reference values and regulator parameters correctly selected, the inverter side regulation modes are easily and smoothly swapped through the use of the minimum Alpha order outputted by all regulators. Explanations on the main operating conditions are given in Table 2.

Table 2- Description of Major Operating Points on the Vdc-Idc Static Characteristic

Operating Point	Description
A	Normal operating condition when voltage + current + Gamma minimum control modes are activated at the inverter. The rectifier operates in constant current control, and the inverter in constant voltage control. At this operating point, the measured Gamma angle is higher than the reference Gamma minimum.
B	A low AC voltage at the rectifier AC side keeps the DC current from being regulated at nominal value (commutating voltage dependant). The inverter regulator switches to DC current control to maintain a minimal power flow. This action also helps in stabilizing the HVDC System.
C	Normal operating condition when current + Gamma minimum control modes are activated at the inverter. The rectifier operates in constant current control, and the inverter in constant Gamma minimum control. However, when voltage + current + Gamma minimum control modes are activated, this operating condition is obtained only if the measured Gamma angle is lower than the reference Gamma minimum. Switching controls to this mode will help in stabilizing the HVDC link and reduce the probability of commutation failures at the inverter.
CD	Gamma minimum regulation mode.
AD	Constant DC Voltage regulation mode.
AF	Voltage regulation mode stabilization characteristic (Beta regulation).
CG	Gamma min. regulation mode stabilization characteristic (Beta regulation).

1.2.2 Gamma Minimum Regulation

The Gamma minimum regulation mode at the inverter is used for dynamic stability purposes. The inverter's reactive power consumption depends on its Gamma angle [5]. With weak AC systems, the Gamma regulation mode is essential to ensuring voltage stability, and at times Gamma angle modulation may also be used for reactive power regulation. With weak AC systems, a DC current variation at the rectifier will cause larger AC voltage variations at the inverter AC commutation bus. Since DC voltage is directly dependent on the inverter side AC

voltage, such deviations may result in DC power flow perturbations, thereby causing dynamic stability issues. Using the Gamma regulation mode will reduce the probability of commutation failures since this mode helps prevent extinction angles (Gamma) from reaching a value that is lower than the specified minimum Gamma. Allowing for operation in Gamma minimum regulation mode will modulate power flow and contribute to overall system stability.

The Gamma angle measurement for the regulation loop is a discrete sampled value, updated at each thyristor commutation. For a given thyristor, the Gamma angle is defined as the delay between the fall time of the thyristor current and the positive zero-crossing of the thyristor voltage (Figure 5). However, in the measurement function implemented in the described model measures the angle between the fall time of the thyristor current and the positive zero-crossing of the commutating voltage of a given valve. The vector diagram of the calculated commutating voltages is shown in Figure 9. All 12 thyristors of an inverter are monitored for individual Gamma angle measurement, and the minimum measured Gamma over one cycle is used as a feedback to the Gamma minimum regulator. More details are given in [2].

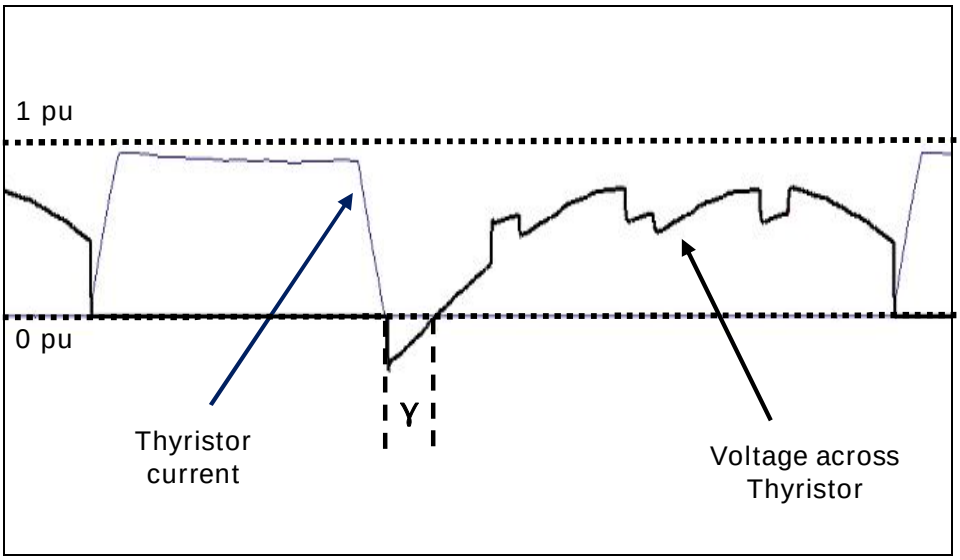

Figure 5 - Gamma angle measurement principle

A typical value of 18 degrees for the minimum Gamma reference is set by default in the present model. This parameter must be selected judiciously since the reactive power increases with Gamma and the probability of commutation failures increases with reduction of this parameter when operating with weak AC systems.

Regulating minimum Gamma angle in steady-state provides the user with the option of maintaining reactive power at a given value. In order to regulate the DC voltage, an online tap changer (which is not implemented in the present model) with a suitable regulator is needed. Also, the tap excursion limits must be taken into account. Note that using this control will result in larger conversion losses and may require additional reactive power compensation.

1.2.3 Combining Regulation Principles for Robust HVDC Controls

As shown in Figure 4 and described in Table 2, the system normally operates at operating point “A” (or “C”). In order to avoid conflict between the rectifier and inverter DC current regulators, a constant current margin (typically, 0.1 p.u.) is maintained between the current references at both the rectifier and at the inverter. However, if during a fault or contingency, a voltage drop occurs at the rectifier side the AC system, the operating condition switches to point “B”. The rectifier is then forced to the minimum Alpha angle (set to 5 degrees) operation, which means that the rectifier current regulator is no longer capable of regulating current. The inverter, therefore, takes over current control mode. This operating point switch at the inverter helps to maintain a current transit of 0.9 p.u. in spite of AC voltage loss at the rectifier and the incapacity of its current regulator to operate at the reference value.

With transformer winding ratios properly set, the inverter works in DC voltage regulation mode in steady-state, under normal operating conditions. This will provide constant (nominal) power flow as the DC current is controlled at the rectifier and the DC voltage is controlled at the inverter. Using constant voltage regulation (segment AD seen in Figure 4, refer to Table 2) avoids dynamic instabilities that exclusive Gamma + current regulation may induce. The schematic diagram of the combined inverter regulators is illustrated in Figure 6.

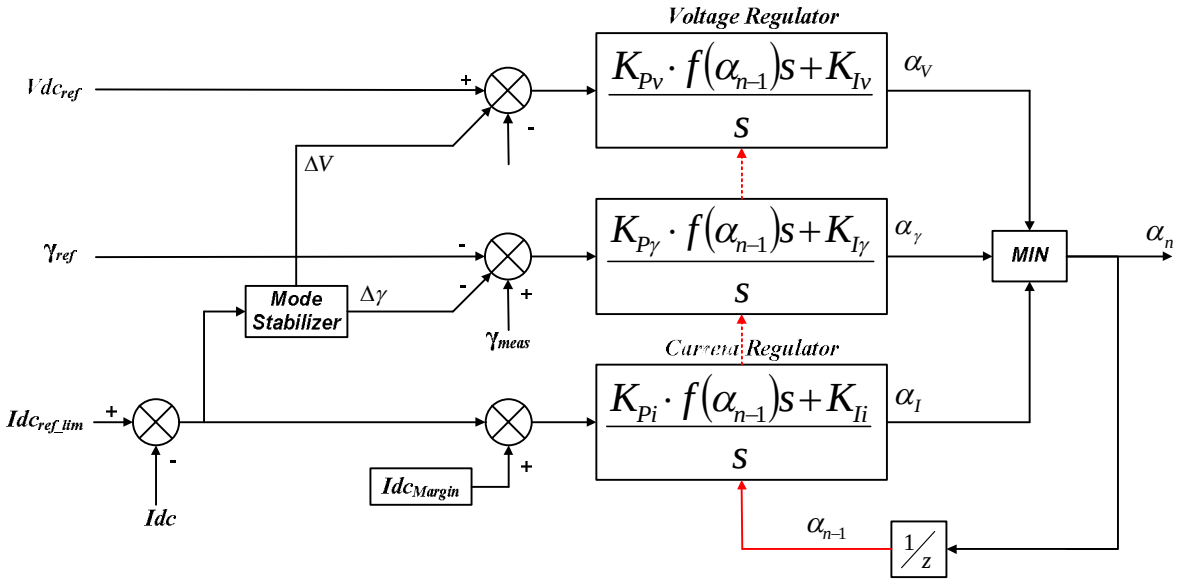

Figure 6 - HVDC Regulators Schematic Diagram

Regulation modes are smoothly switched from one to another through the use of the minimum Alpha order outputted by all regulators. Each regulator has a PI corrector with a partial linearization function acting on the proportional gain. The assumption made is that the integral action is efficient enough to compensate for non-linearity in steady-state. The proportional gain linearization offers better precision, faster recovery from faults and faster start-up of the HVDC link. For instance, with the voltage regulator, as described in equation (1),

a DC voltage deviation multiplied by a proportional gain (linearized) results in an Alpha angle deviation.

$$\frac{\Delta V_{dc}}{\Delta \alpha} = \frac{1}{Kp_{lin}} \qquad (1)$$

However, according to the known steady-state equations for a 12-pulse thyristor converter, one can infer the relationship described in (2).

$$\frac{d}{d\alpha} V_{dc}(\alpha) \propto \sin(\alpha) \qquad (2)$$

The derivative of the DC voltage according to Alpha is proportional to the sinus of Alpha, thus the linearized gain is proportional to the inverse of the sinus of Alpha, as stated in (3).

$$Kp_{lin} \propto \frac{1}{\sin(\alpha)} \qquad (3)$$

$$Kp_{lin} = f(\alpha) \cdot Kp_{fixed} \qquad (4)$$

Depending on the operating point, a function of the Alpha angle is multiplied by the fixed proportional gain, as seen in equation (4), in order to achieve partial linearization on proportional gain. In order to avoid algebraic loops for the computation of this linearization function, the discrete value of the Alpha angle used in the preceding instant is used.

As seen in Figure 6, a mode stabilizer [5] is connected at the inputs of both the constant voltage regulator and the Gamma minimum regulator. This function, which results in the modification of the static characteristic, corresponds to segments CG and AF, as seen in Figure 4 and described in Table 2. The resultant negative slope of the characteristic keeps the regulators from hunting between multiple modes of operation when an AC voltage drop at the rectifier causes regulator mode changes.

AC voltage instabilities in weaker AC systems can occur due to larger voltage deviations (caused by high DC current deviations). Combining the three modes at the inverter offers the best option for dynamic stabilization of the overall system during important voltage (or current) deviations and when the extinction angle crosses the minimum Gamma reference value.

In reality, this mode will also keep the online tap changers from operating continuously, since simple voltage regulator actions on the Alpha angle can compensate for a great margin of operating conditions.

Even with the beneficial effect on power system stability offered by the Gamma minimum control mode, hybrid operation using exclusively Gamma + current regulation is not recommended for control of terminals connected to a weak AC system. In fact, the weaker the

AC system, the steeper the constant Gamma Control characteristic will be (segment CD seen in Figure 4, refer to Table 2). A small variation in DC current will cause a larger variation in DC voltage when exclusively using constant Gamma Regulation with weaker AC systems, thereby providing the HVDC link with poor power stability and robustness.

1.2.4 Voltage Dependant Current Order Limiter (VDCOL)

The Voltage Dependant Current Order Limiter (VDCOL) block is used with both the rectifier and the inverter regulators [2][7]. According to a given DC voltage – DC current profile, this function adapts the current reference sent to the regulators. When important voltage drops occur at the AC system(s) or faults on the DC link cause DC voltage drops, the current reference is limited according to a linear profile determined by the function's internal parameters. As explained in [2], the VDCOL automatically reduces the reference current (*Id_ref*) set point when *VdL* decreases. The current-voltage characteristic of the VDCOL is illustrated in Figure 7.

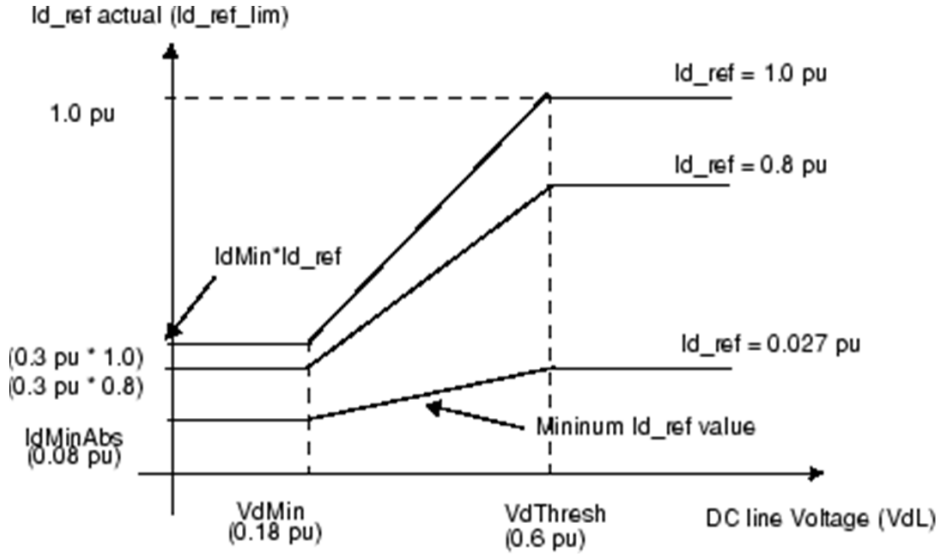

Figure 7 - VDCOL Current-Voltage Characteristic[2]

As described in [2], the *Id_ref* value starts to decrease when the *Vd* line voltage falls below a threshold value *VdThresh* (0.6 pu by default). The actual reference current used by the controllers is named *Id_ref_lim*. *IdMinAbs* is the absolute minimum *Id_ref* value, set at 0.08 pu. When the DC line voltage falls below the *VdThresh* value, the VDCOL drops instantaneously to *Id_ref*. However, when the DC voltage recovers, the VDCOL limits the *Id_ref* rise time with a time constant defined by the parameter *Tup* (80 ms by default).

[2] Image copied from [2].

The automatic reduction of the DC current reference has, first of all, the effect of reducing the reactive power demand and is thus beneficial to fault recovery. The reduced current reference may increase the chances that the inverter will regulate DC voltage at fault recovery. The VDCOL function also reduces the probability of repeated commutation failures during AC system re-establishment. More details on its parameters are given in [2].

1.3 Pulse Generation Unit

The pulse generation unit is comprised of a 12-pulse generator that outputs sequentially firing pulses to the thyristor valves. A PLL is employed to synchronize the 12-pulse firing pulse generator, according to commutation voltage zero-crossings. The PLL is capable of precisely measuring the fundamental frequency and the instantaneous angle of the voltage (positive sequence). It outputs the sinusoidal waveforms of the three-phase voltages (with unitary amplitude) to the pulse generator that will synchronize on zero-crossings and activate the firing signals with a delay given by Alpha order (from the regulators). The PLL also outputs the measured frequency which is used by the Gamma measurement unit to convert the measured Gamma “time delay” to a Gamma “angle” value. The PLL can also adapt to phase and frequency variations on the AC network. Moreover, it eliminates all harmonics that could create false or multiple zero-crossings of the commutation voltage.

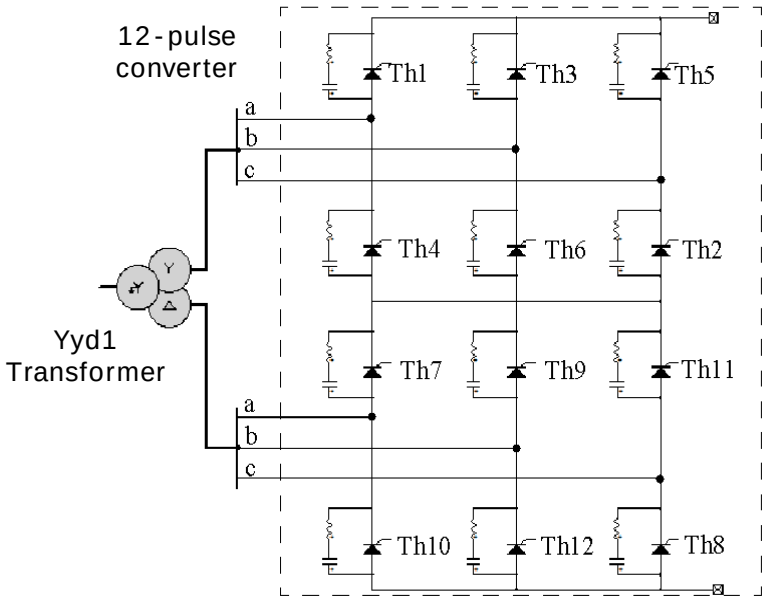

Figure 8 - Thyristor Mapping of a 12-Pulse Converter

The commutation sequence is also dependent on the converter three-phase transformers because the AC voltage timings are different if the delta winding has a phase displacement of plus or minus 30 degrees. This is taken into account in the 12-pulse generator. In the current HVDC system model, Yyd1 (30 degrees lag) transformers are used. The mapping of a 12-pulse converter is illustrated in Figure 8.

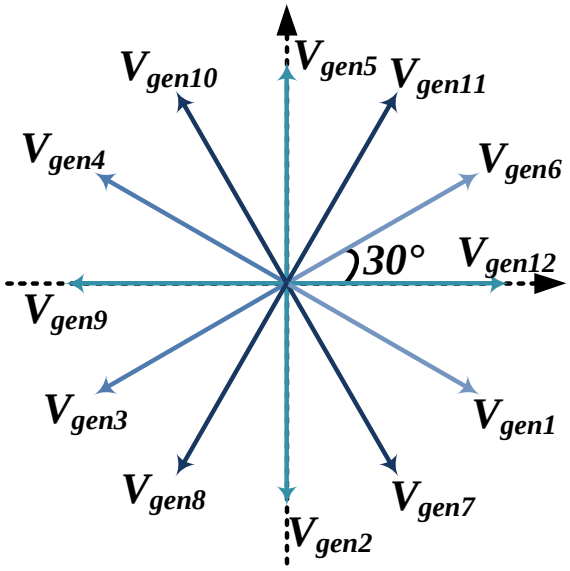

Figure 9 - Vector Diagram - Commutation Voltages of the 12-pulse generator

The 12-pulse generator inputs the three-phase unitary sinusoidal signals given by the PLL and calculates all the instantaneous sinusoidal waveforms needed to synchronize each thyristor firing. The commutation voltages are obtained by applying a combination of phase voltage, phase-to-phase voltage and phase opposition mathematical principles on the given three-phase sinusoidal signals. The vector diagram of the resulting commutation “voltages” is illustrated in **Figure 9**. The positive zero-crossings of each commutation voltage are then monitored and a pulse is generated after a delay of “Alpha” degrees. This commutation process is illustrated in Figure 10 for a thyristor rectifier.

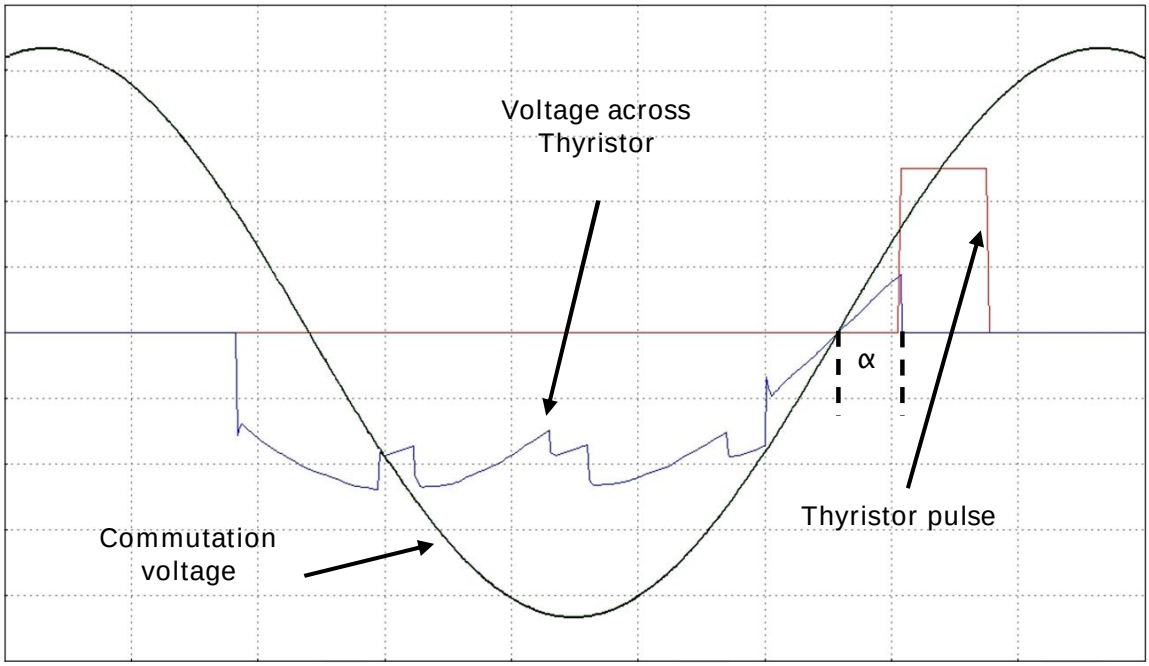

Figure 10 - Commutation Process of Thyristor Rectifier

1.4 Protections

1.4.1 DC Fault Detection and Protection

A short-circuit on the DC side of an HVDC link cannot be extinguished unless the DC current is brought to zero. Deionization of the fault arc is also a requisite. As seen in the static characteristic of the HVDC system, current is normally controlled by the rectifier and the DC power flows from the rectifier to the inverter. In order to lower the DC current to zero by control actions, the rectifier is forced momentarily into inverter operation when a DC fault is detected.

DC faults can be detected by monitoring the instantaneous DC voltage. A detection occurs when the DC voltage level crosses a specified threshold.. Whenever the DC voltage crosses this threshold (0.5 pu by default), a forced Alpha signal is sent to the regulators that will momentarily force the output Alpha order of the rectifier regulators into an inverter mode of operation (166 degrees, by default). To avoid ill-timed actions originating from the protection function, and occurring during fast transients that may not be caused by DC faults, a delay between the instant of detection and the instant of protective action is implemented.. An example of the phenomenon and resulting waveforms are presented and discussed in section 1.7. Other details are given in [2][4].

1.4.2 Low AC Voltage Detection

The low AC voltage detector function measures the magnitude of the combined three-phase voltages (primary winding) by using equation (5), based on the three-phase rectifying principle of a Graëtz bridge.

$$V_{AC}(t) = \frac{\pi}{3\sqrt{3}}\left(\max\{V_a(t), V_b(t), V_c(t)\} - \min\{V_a(t), V_b(t), V_c(t)\}\right) \quad (5)$$

When a low AC voltage is detected (with a default threshold value of 0.7 pu), a detection signal is sent to the DC protection block. This signal serves as a discriminator to the DC fault protection and will deactivate it. In other words, the DC fault protection needs a discriminator to determine whether the DC voltage drop is caused by a DC fault or by an AC system voltage drop (since DC voltage is directly dependent on AC voltage).

1.4.3 Commutation Failure Prevention Control

A commutation failure occurs when the incoming valve fails to take over direct current before the commutating voltage reverses polarity with sufficient extinction time. This phenomenon may be apparent at the inverter due to its valve voltage profile, which is positive when the valve is in blocked state. When a commutation failure occurs, a known practice [4][5] to reduce the probability of successive commutation failures is to force a firing angle advance for the next few commutations. However, the block implemented in this model is not a commutation failure “detector” and does not take direct action on the regulators.

The implemented function is called a Commutation Failure Prevention Control as described in [6][2]. During severe contingencies, a faster response is necessary to increase the commutation margin and consequently to reduce the probability of a commutation failure. The Commutation Failure Prevention Control subsystem simply generates a signal that decreases the maximum limit of the Alpha angle during an AC voltage drop. An example of thyristor misfire and the resulting waveforms simulated using the described model are presented and discussed in section 1.8.

1.5 Using **TestDrive** to Develop HVDC or other Model GUI

The GUI of a real-time simulator is very important. For example, in repetitive fault tests, it is desirable to have the display of certain data triggered on the fault under investigation. **TestDrive** software from **Opal-RT** has an interface based on **LabVIEW** software from **National Instruments;** this interface can also be scripted using **Python**. **TestDrive** uses the **LabVIEW** runtime engine enabling users to build on-the-fly **LabVIEW** displays and control panels by virtually wiring real-time simulation signals to graphical displays. **TestDrive** also has built-in display triggering capability that enables the display of complex waveforms in real-time and the synchronization of those waveforms to specific events like a fault or control signal step. For controlling and monitoring real-time simulations, the **TestDrive** interface has the following advantages over standard **Simulink**:

- Easy, point-and-click dynamic selection of signals to view,
- Synchronous display of data on triggered events,
- Easy management of multiple windows for control signals and acquisition data,
- Built-in Python scripting tool for designing test suites,
- Ability to use advanced graphical features of **LabVIEW**.

Figure 11 shows the main **TestDrive** interface window in which the real-time simulation signals are displayed in the right part of the window. The figure shows the interface in its signal selection mode. In this mode, all signals coming from the real-time simulation are listed in the middle part of the window. The user can select a signal simply by clicking on it and assigning it to one of the scopes on the right side of the window.

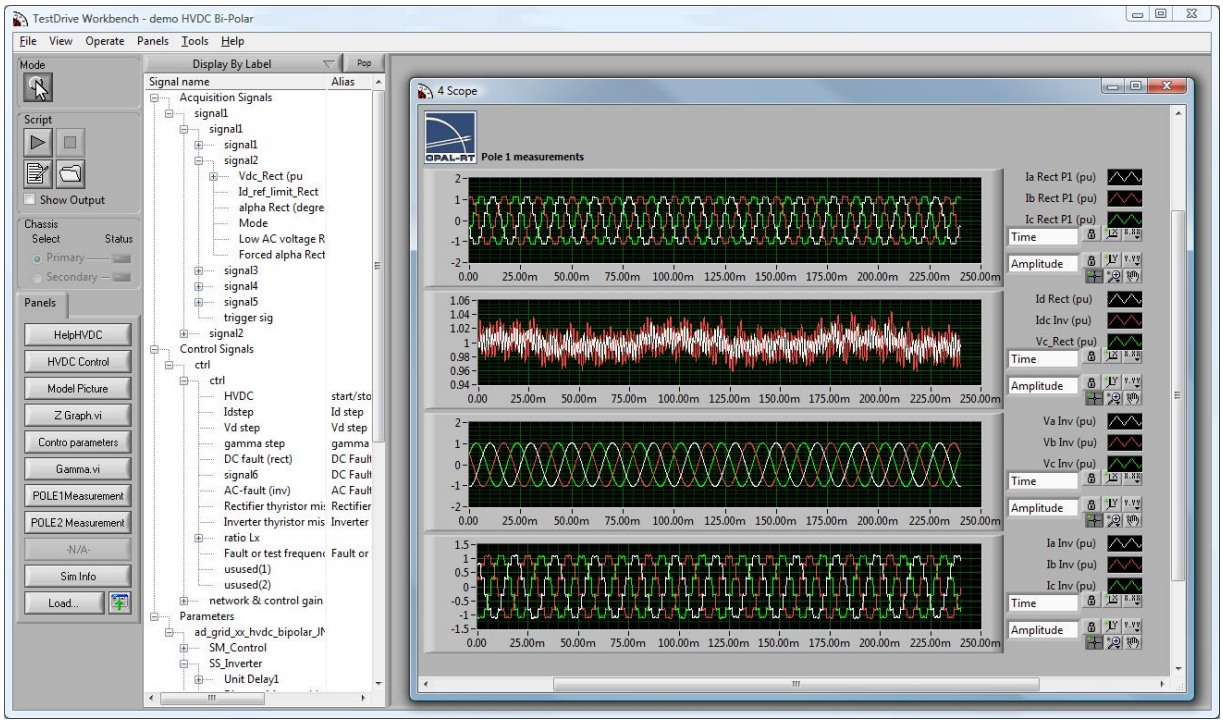

Figure 11 - Main TestDrive panel in signal assignment mode

The left side of the **TestDrive** interface displays a list of available display/control panels (e.g., scopes) for signals. The HVDC control panels, illustrated in Figure 12, are examples of dialog boxes used to control fault and test signals (AC faults, DC faults, and small signal perturbations).

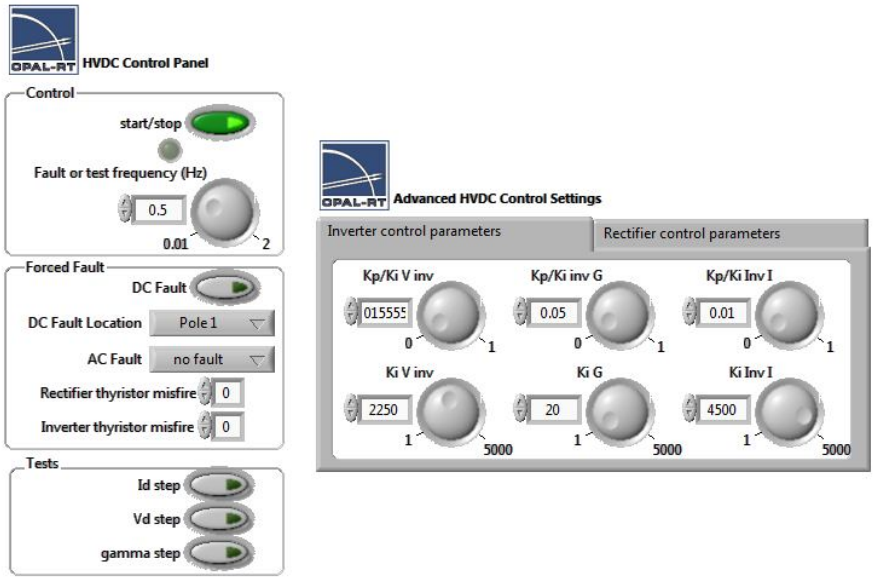

Figure 12 - Example control panels of the HVDC system

An important, yet convivial, aspect of fault study simulations is the ability to synchronize the simulation results on the fault so that the display does not “move”. This enables a user to vary simulation parameters (e.g., network impedance) and dynamically observe the effect of varying these parameters (e.g., DC-link recovery time, modes of operation, etc.)

1.6 Model Distribution and Real-Time Performance

The model was simulated in real-time using an **eMEGAsim** simulator. The model distribution and real-time performance are described in Table 3. The whole system is running at a hard real-time step of 50 μs (without I/O). This model is distributed across **3 CPU cores**.

Table 3- CPU Allocation and real-time performance for the bipolar HVDC model

CPU	Components Content	Model Calc. Time	Minimum time step	Acceleration factor[3][4]
CPU 1: Controller	• 1 HVDC Main control • 2 HVDC Rectifier controls and protections • 2 HVDC Inverter controls and protections	30 μs (30%) (100 μs Time-Step)	22 μs	71 (50 μs)
CPU 2: Rectifier	• 1 ideal 3-phase voltage source • 1 equivalent network impedance • 2 YgYD converter transformers • 2 thyristor rectifiers (12-pulse) • 2 DPL (½ decoupling)[5] • 2 smoothing reactors • 1 capacitor bank • 2 single-tuned AC Filters (RLC branch) • 1 high-pass AC filter (parallel RL w series C)	16 μs (32%) (50 μs Time-Step)		
CPU 3: Inverter	• 1 variable parameters network impedance • 2 YgYD converter transformers • 2 thyristor inverters (12-pulse) • 2 DPL (½ decoupling)[5] • 2 smoothing reactors • 1 capacitor bank • 2 single-tuned AC Filters (RLC branch) • 1 high-pass AC filter (parallel RL w series C)	17 μs (34%) (50 μs Time-Step)		

[3] The **eMEGAsim** target computer used for the test is a dual Intel® Core™ 2 Quad processors, 2.3 GHz, 2 GB RAM

[4] The Windows-based PC station used for the test is an *Intel ® Core™ 2 Duo CPU, 2.10 GHz, 3 GB RAM*

[5] DPL: Distributed Parameter Line for model distribution; ½ the line is calculated in that CPU

Three different tests were conducted to quantify the simulator/model combined performance.

The first test is a performance comparative indicator. The same model was also simulated on a Windows-based PC. As seen in Table 3, the latter was shown to be 71 times slower than the **eMEGAsim** simulator (see the acceleration factor of the **eMEGAsim**), which means that it took 71 “wall clock” seconds in offline mode, on a regular PC, to simulate 1 second of the model (real-time duration).

The second test is the minimum time step test, which is the value of the time step that would still be acceptable to simulate the model without having any overruns (effective time step larger than the real-time clock’s step). In this case, the CIGRE benchmark HVDC link model can be run at a time step as low as 22 ms.

Finally, for the third test, the calculation time of each parallel distributed part of the model was monitored. This value indicates the percentage of a real-time clock step that is needed by the **eMEGAsim** real-time simulator to solve the model equations. These values (30% for controller, 32% for rectifier and 34% for the inverter) also indicate that there is idle time available that each processor could use to simulate additional devices. Therefore, one can conclude that this model’s complexity could be further augmented while maintaining good real-time performance.

1.7 DC Fault on Rectifier side of Pole 1

A DC-fault was applied on the rectifier side of Pole 1 of the bipolar HVDC link. This test shows some specific control actions that occur during a DC fault. As one can observe on Figure 13, at the beginning of the fault, the DC current at the rectifier has a maximum transient of 3 pu, and then goes to the minimum reference value of 0.1 pu, specified by the VDCOL [4][9]. Figure 14 shows the DC voltages and the Alpha orders on the inverter side of the link. The DC-fault brings the DC voltage to zero while the inverter voltage controller lowers the Alpha order, trying to raise back the voltage on Pole 1. It then falls to its minimum value of 92 degrees, putting the Pole 1 inverter controller in Alpha min mode and the Gamma angle to a large value of about 170 degrees (Figure 15).

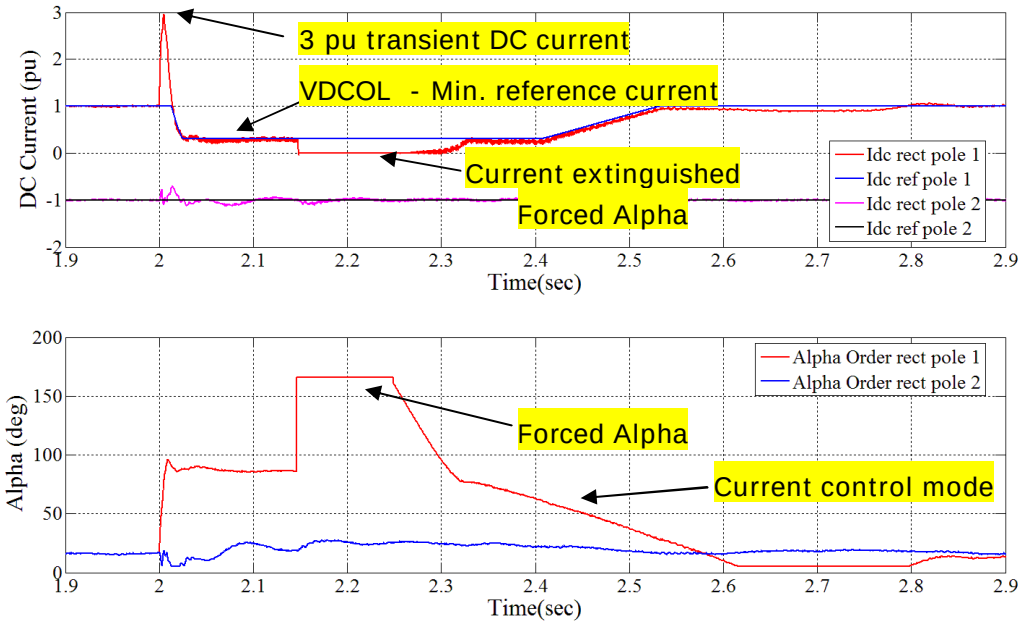

Figure 13 - DC fault on rectifier side of Pole 1: DC current and Alpha order on rectifier side

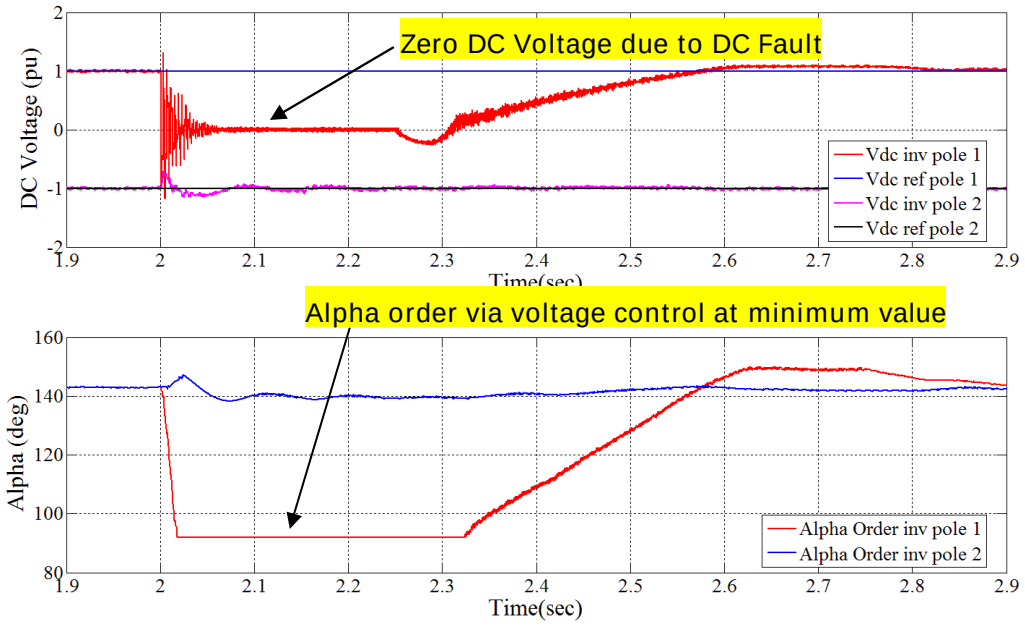

Figure 14 - DC fault on rectifier side of Pole 1: DC voltage and Alpha order on inverter side

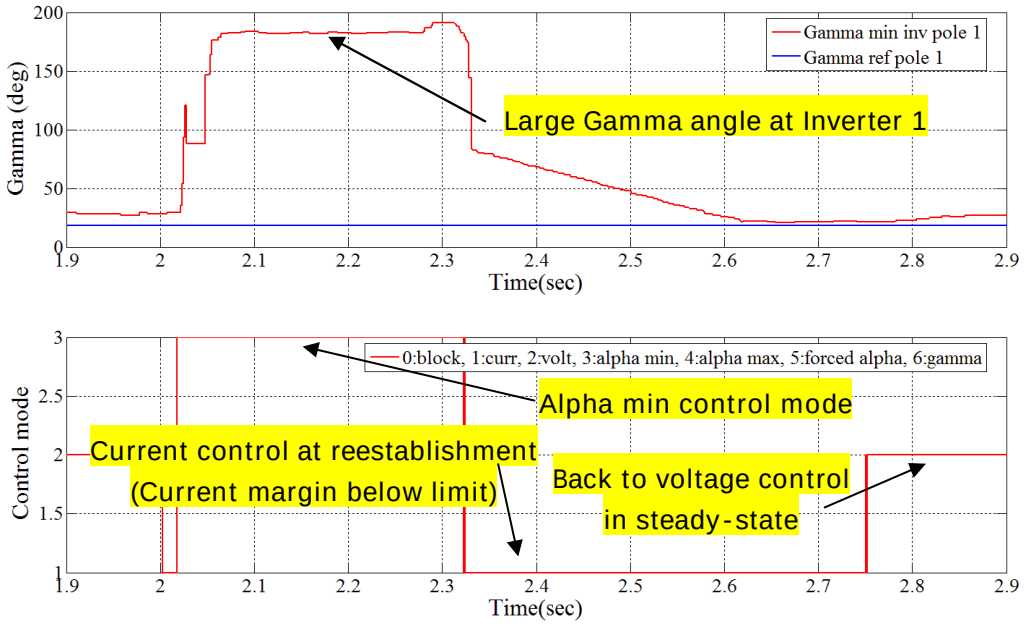

Figure 15 - DC fault on rectifier side of Pole 1: Gamma angle and control mode on inverter side

After a detection delay of 0.15 seconds, the DC protection system of each rectifier controller acts, sending the rectifier control a forced alpha angle order. The rectifier is then forced to its maximum operating value Alpha of 166 degrees (i.e. it acts as an inverter) in order to extinguish any DC current feeding the fault arc (see Figure 13). The arc is extinguished and the forced alpha order is released. The system slowly returns to steady-state with a ramped current reference set by the VDCOL.

One can also observe that Pole 2 of the bipolar HVDC link is controlled independently from Pole 1, since Figure 13 - **Figure 15** reveal some very small, even negligible high frequency perturbations on Pole 2 during the DC fault occurrence on the rectifier side of Pole 1. Moreover, this shows one of the advantages of having a bipolar link: half of the rated power can still be transmitted when a disturbance occurs on only one of the Poles.

1.8 Misfire (Commutation Failure) on Thyristor 2 of Inverter of Pole 2

A commutation failure on the Inverter of Pole 1 is *emulated* by causing a misfire at Thyristor number 2. It is said to be *emulated* because, in practice, a *commutation failure is defined as resulting from the failure of the incoming valve to take over the direct current before the commutating voltage reverses its polarity*. Here, the misfire is artificially created by removing a firing pulse at the stated thyristor. The net effect is similar to a commutation failure.

Figure 16 shows the DC currents and the Alpha orders on both Poles of the HVDC link. Some transients on the DC current and the DC voltage at the Inverters (**Figure 17**) are observed as the misfire causes a perturbation in the switching pattern. As the DC voltage observed on **Figure 17** is moderately affected by this misfire (at zero for less than 1 ms and re-established in less than 200 ms), the DC current is also perturbed for a small amount of time. Since the DC voltage does not cross zero for a sufficient period of time, the DC protection system at the rectifier does not act and the Alpha order is not forced. Instead, the current reference is lowered transiently by the VDCOL (depending on DC voltage level), which maintains good stability of the HVDC system during this contingency.

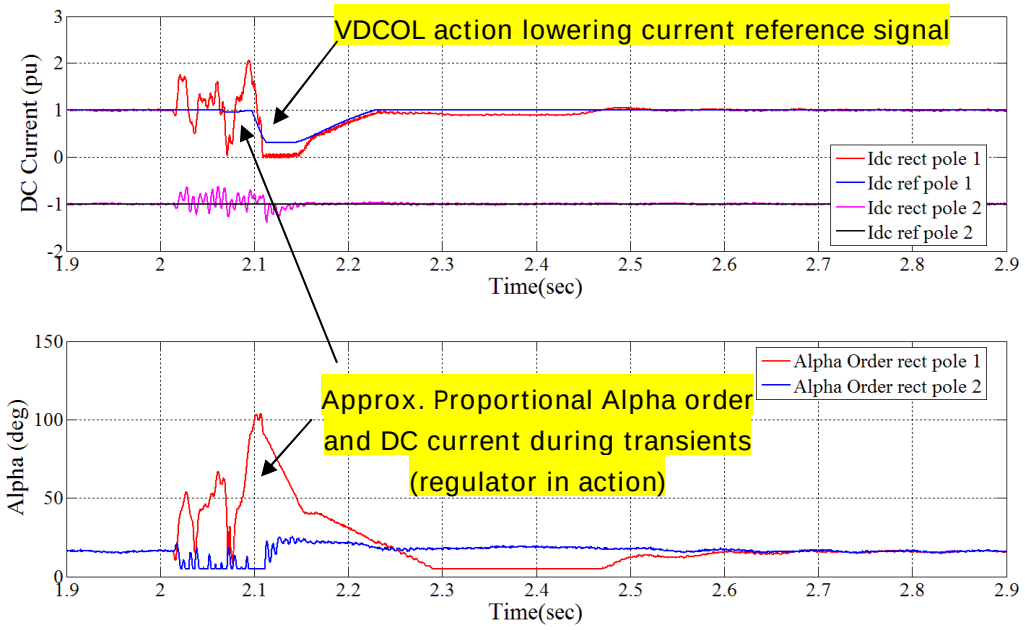

Figure 16 - Misfire Thyristor 2 of Pole 2 Inverter: DC current and Alpha order on rectifier side

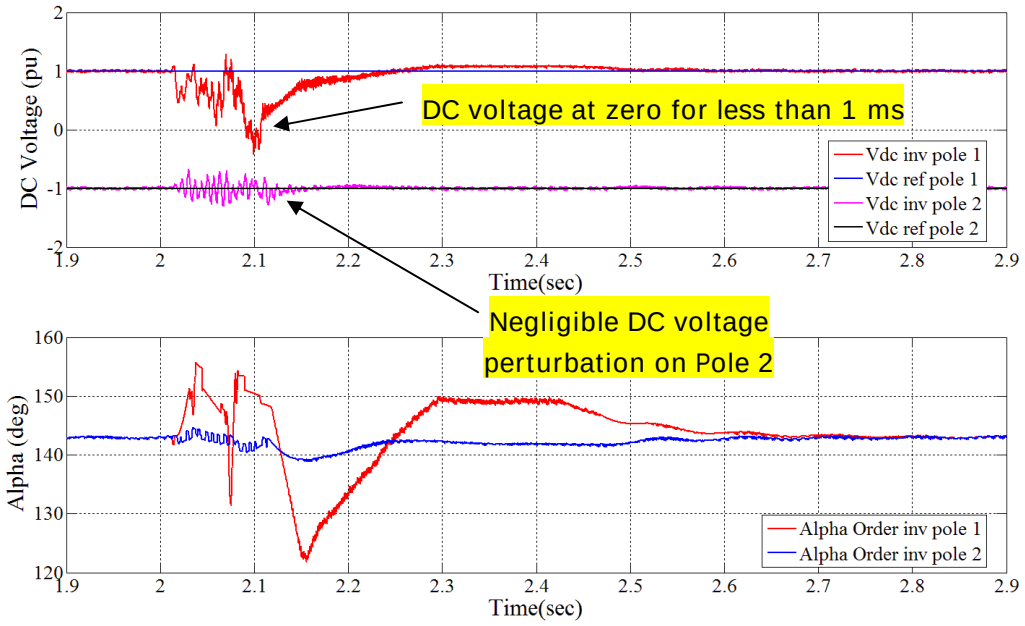

Figure 17 - Misfire Thyristor 2 of Pole 2 Inverter: DC voltage and Alpha order on inverter side

As one can observe in Figure 16 and **Figure 17**, the Alpha angles, at the rectifier and the inverter respectively, are oscillating proportionally to the DC current (on rectifier side) and to the DC voltage (on inverter side) during transients. This shows that both the rectifier current regulator and the inverter's combined voltage + current + Gamma minimum regulators are still in action attempting to re-establish the DC link current and voltage to the referenced values.

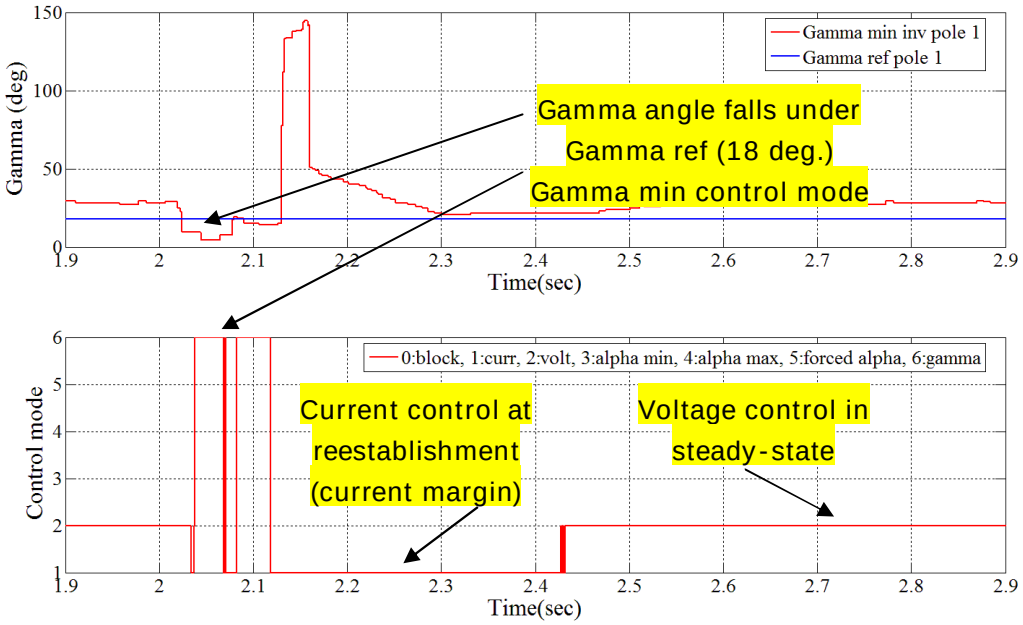

Figure 18 - Misfire Thyristor 2 of Pole 2 Inverter: Gamma angle and control mode on inverter side

During a commutation failure (Figure 18), the measured Gamma angle at the inverter falls to a very low value (below the Gamma reference of 18 degrees), which automatically puts the inverter in Gamma minimum control mode. The Gamma controller contributes to system stability by keeping the Gamma angle at a sufficiently high value, thereby avoiding other commutation failures.

A supplementary commutation failure protection scheme is implemented in this HVDC model. The commutation failure prevention system takes action during a certain type of contingency to avoid commutation failures [2][6]. The commutation failure prevention system is primarily used to mitigate commutation failures that occur due to AC voltage dips. After an AC fault detection (three-phase or one-phase), an Alpha angle value is sent to the converter control in order to be deducted from the maximum Alpha angle limit (alpha_max) of the inverter. In practice, the commutation margin is then consequently enlarged.

One can also observe that Pole 2 of the bipolar HVDC link is controlled independently from Pole 1 since Figure 16 - Figure 18 reveal some very small, even negligible perturbations on Pole 2 during the DC fault occurrence on the rectifier side of Pole 1. Moreover, this shows one of the advantages of having a bipolar link: half of the rated power can still be transmitted when a disturbance occurs on only one of the Poles.

2. First CIGRE Benchmark for HVDC Control Studies

The first CIGRE benchmark for HVDC [1] was primarily developed to test HVDC controller robustness and for use as a tool in the design and optimization of controllers when the HVDC link is connected to weak and resonant AC systems. The AC systems, filters, transformers and DC link parameters are selected to create undesirable oscillations in the controllers and produce stability issues at rated power. The schematic diagram of this system is shown in Figure 19.

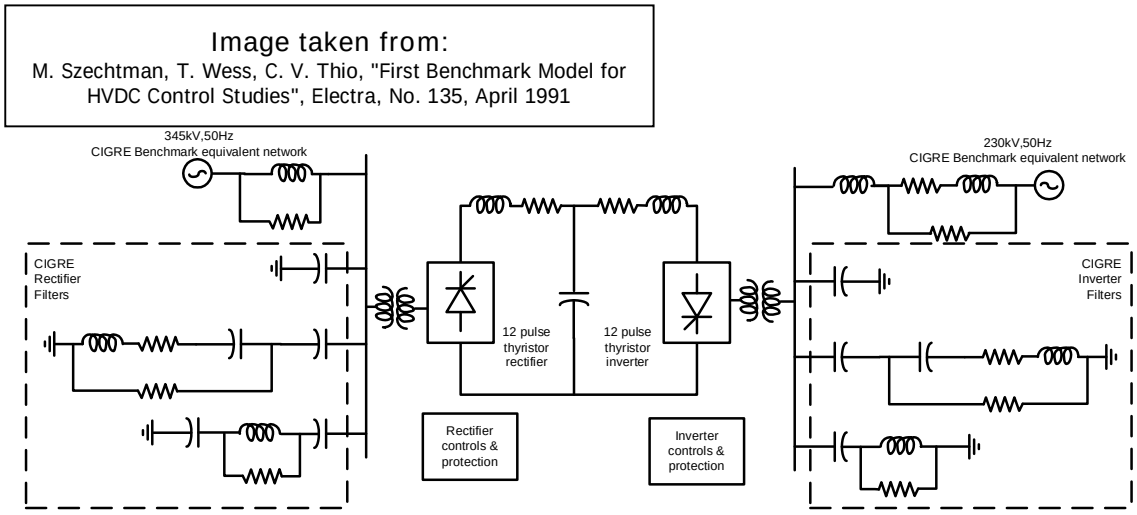

Figure 19 - First CIGRE HVDC Benchmark[6]

The first CIGRE benchmark is designed for an HVDC link rated at a 1000 MW DC power with a DC voltage of 500 kV and a DC current of 2 kA. The monopolar DC-link is modeled with a smoothing reactor on each side and a capacitor in the middle. The AC systems are modeled to get a short-circuit ratio (SCR) of 2.5 on both sides. This is quite problematic, especially on the inverter side, since the Maximum Available Power (MAP) for a fixed value of the extinction angle Gamma is reduced [4]. A weak system forces the HVDC controls to operate near their stability margin. In fact, a network with an SCR of 2.5 is considered to be a weak system, which makes its voltage stability harder to maintain, and thus the operation of the HVDC controls more difficult. The Benchmark is also defined in a way that creates composite resonances between the AC and the DC system, creating difficult conditions for the HVDC controls [4].

The objective of this model is to introduce the user to HVDC controller optimization. The DC link parameters and the AC systems parameters [1] were used to implement this HVDC system. Moreover, the rectifier and inverter controllers described in section 1 were used.

[6] Image from [1]

2.1 Model Distribution and Real-Time Performance

The model was simulated in real-time using an **eMEGAsim** simulator. Model distribution and real-time performance are described in Table 4. The whole system is running at a hard real-time step of 50 µs (without I/O). This model was simulated using only **1 CPU core**.

Table 4- CPU Allocation and real-time performance for the CIGRE HVDC model

CPU	Components Content	Model Calculation Time	Minimum time step	Acceleration factor[7][8]
CPU 1: CIGRE Benchmark for HVDC	• 1 HVDC Main control • 1 HVDC Rectifier control and protections • 1 HVDC Inverter control and protections • 2 ideal 3-phase voltage sources • 1 rectifier-side AC system CIGRE equivalent network branch • 1 inverter-side AC system CIGRE equivalent network branch • 2 YgYD converter transformers • 1 thyristor rectifier (12-pulse) • 1 thyristor inverter (12-pulse) • 1 decoupling DC capacitor • 2 smoothing reactors • 1 set of CIGRE benchmark passive filter and capacitor bank for rectifier side AC system • 1 set of CIGRE benchmark passive filter and capacitor bank for inverter side AC system	29 µs (58%) (50 µs Time-Step)	34 µs	23 (50 µs)

[7] The **eMEGAsim** target computer used for the test is a dual Intel® Core™ 2 Quad processors, 2.3 GHz, 2 GB RAM

[8] The Windows-based PC station used for the test is an *Intel ® Core™ 2 Duo CPU, 2.10 GHz, 3 GB RAM*

Three different tests were conducted to quantify the simulator/model combined performance.

First, as a performance indicator, the same model was also simulated on a Windows-based PC. As seen in Table 4, this produced results 23 times slower than the simulation conducted using the **eMEGAsim** simulator (see the acceleration factor of the **eMEGAsim**), meaning that it took 23 "wall clock" seconds in offline mode, on a regular PC, to simulate 1 second of the model (real-time duration).

The second test is the minimum time step test, which is the minimum time step value that can be used to simulate the model without causing any overruns (effective time step larger than the real-time clock's step). In that case, the CIGRE benchmark HVDC link model could be run at a time step as low as 34 µs.

Finally, the calculation time of the single processor used to simulate the model was monitored. This value indicates the percentage of a real-time clock step that is needed by the **eMEGAsim** real-time simulator to solve model equations. With a value of 58%, it also indicates that there idle time remains available that the processor could use to simulate additional devices. Therefore, one can conclude that this model's complexity could be further augmented while maintaining good real-time performance.

2.2 Comparison: SCR of 4.9 and an SCR of 2.5 of Inverter Network

The results displayed in Figure 20 - **Figure 26** illustrate the start-up and steady-state operation of the HVDC link during simulation of the CIGRE benchmark. The results were obtained using two different SCR values on the inverter side of the HVDC link; where case 1 uses a fairly strong AC system (SCR = 4.9) and case 2 uses a weak AC system (SCR = 2.5). In order to obtain these short-circuit ratios, the value of the series inductor of the equivalent impedance of the inverter side AC system was varied, as illustrated in Table 5.

Table 5 - Test parameters for comparison between an SCR of 4.9 and 2.5

SCR	Series inductance
4.9	1 mH
2.5	36.5 mH

With the controller parameters kept at the same values as in the previously presented model, inspired by [2], important oscillations at a frequency of about 10 Hz are present on the illustrated signals when the SCR is at 2.5. Such oscillations are not present when the SCR is at 4.9. In fact, weak AC systems present slow dynamic poles and thus result in a smaller stability margin. In such a case, dynamic instabilities are bound to occur, taking into account AC-DC

system interactions and the combined effect of a slow power regulation loop (as is the case for demonstrations with an SCR of 2.5, shown in Figure 20 to **Figure 26**). The "stable" limit-cycle causing the oscillation mode at 10 Hz observed in Figure 20 to **Figure 26** is a result of the slow power regulation loop of the weak AC system and the minimum Alpha angle limit at the rectifier. Accelerating the rectifier current regulator loop would, for instance, help displace the dynamically unstable pole in the stability region. Further developments would include the optimization of the controllers for stable and robust control of the CIGRE benchmark.

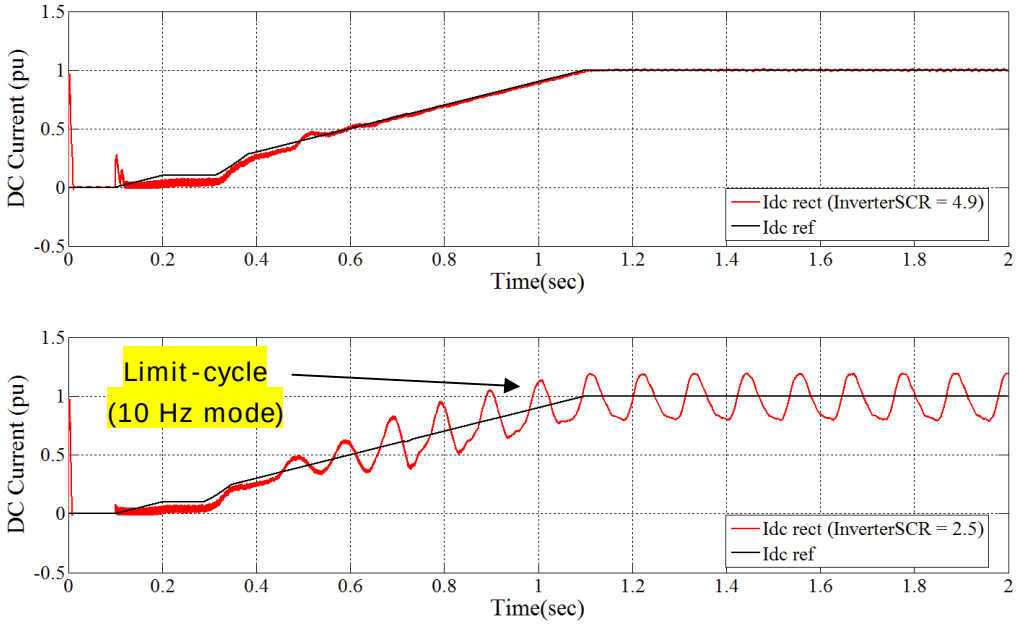

Figure 20 - Comparison between inverter SCR of 4.9 and 2.5: Idc at Rectifier

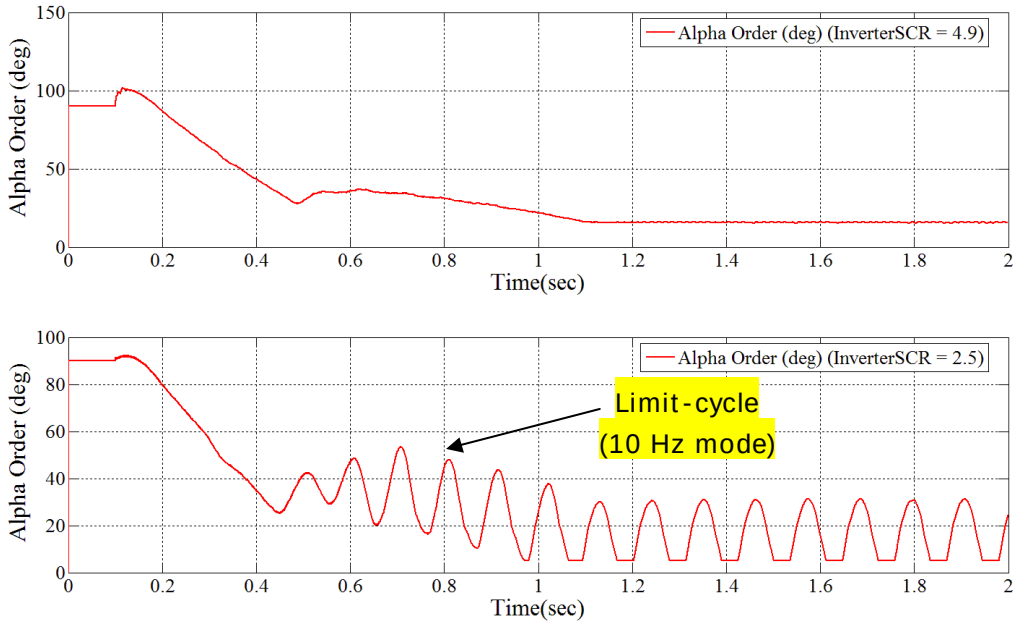

Figure 21 - Comparison between inverter SCR of 4.9 and 2.5: Alpha order at Rectifier

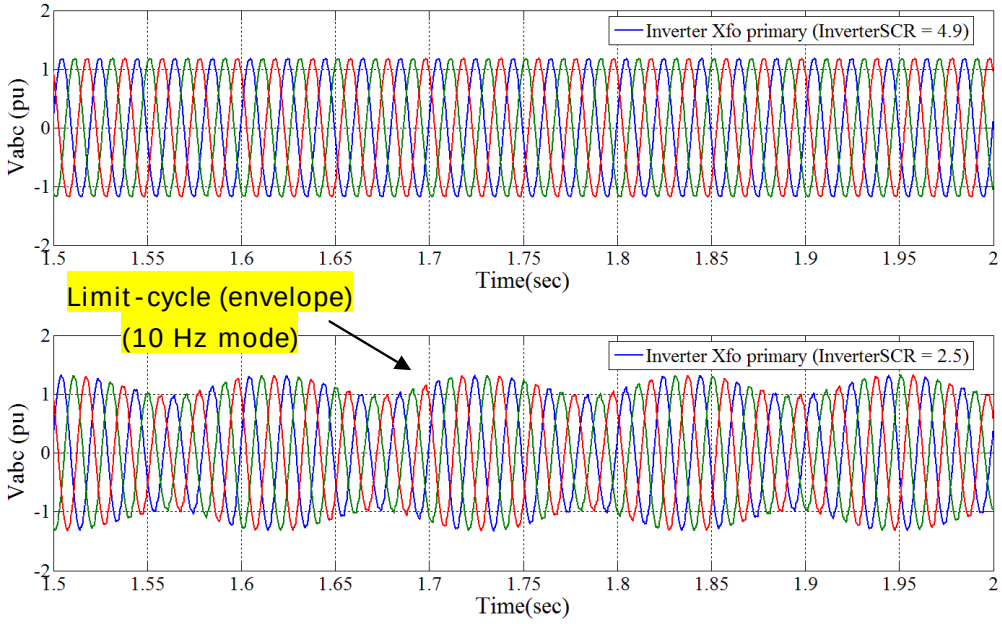

Figure 22 - Comparison between inverter SCR of 4.9 and 2.5: Vabc at Inverter

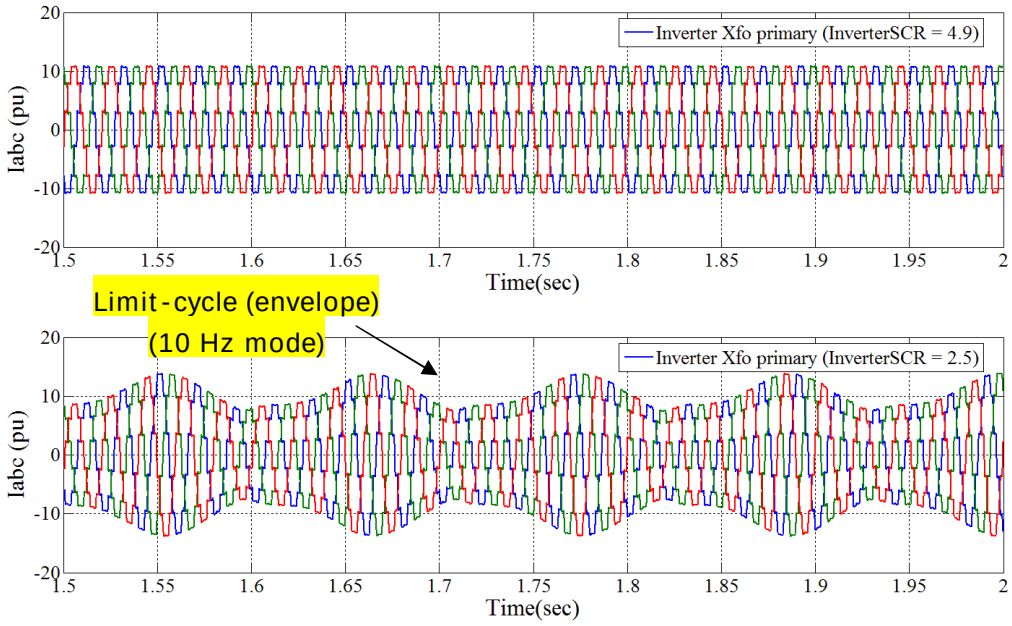

Figure 23 - Comparison between inverter SCR of 4.9 and 2.5: Iabc at Inverter

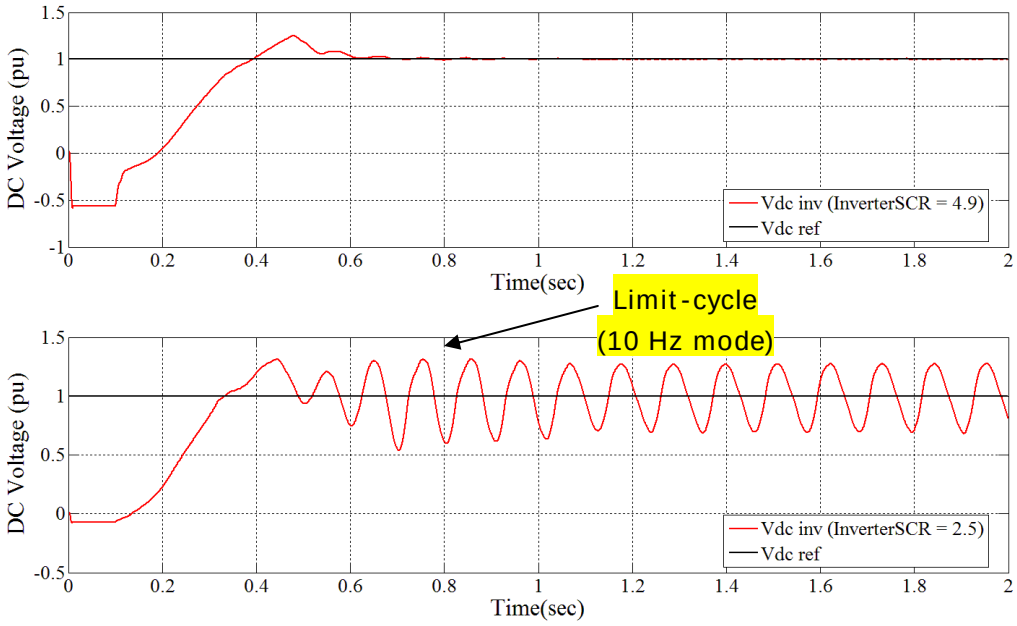

Figure 24 - Comparison between inverter SCR of 4.9 and 2.5: Vdc at Inverter

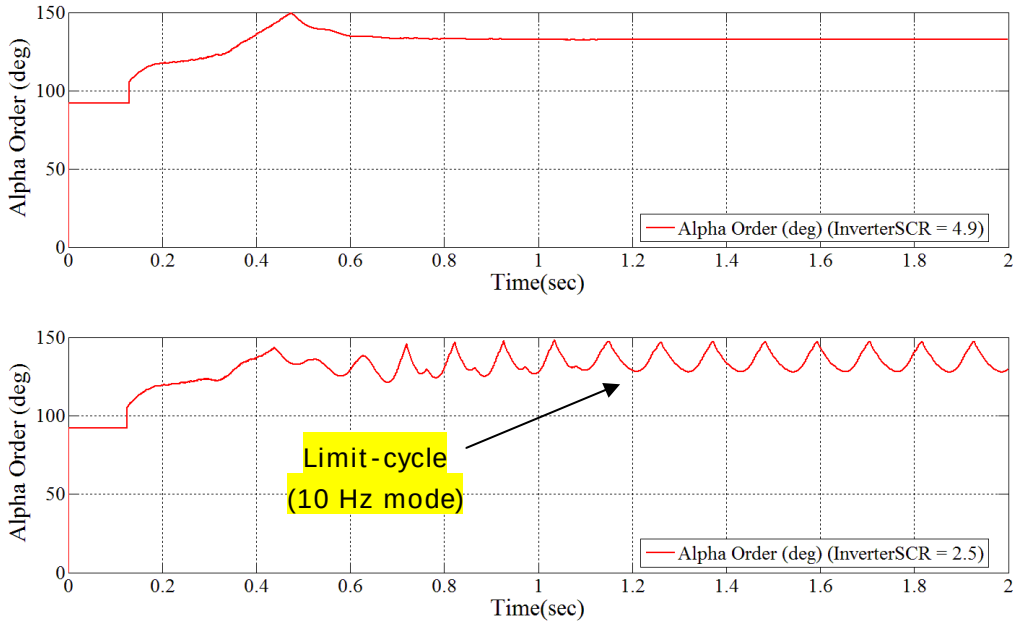

Figure 25 - Comparison between inverter SCR of 4.9 and 2.5: Alpha order at Inverter

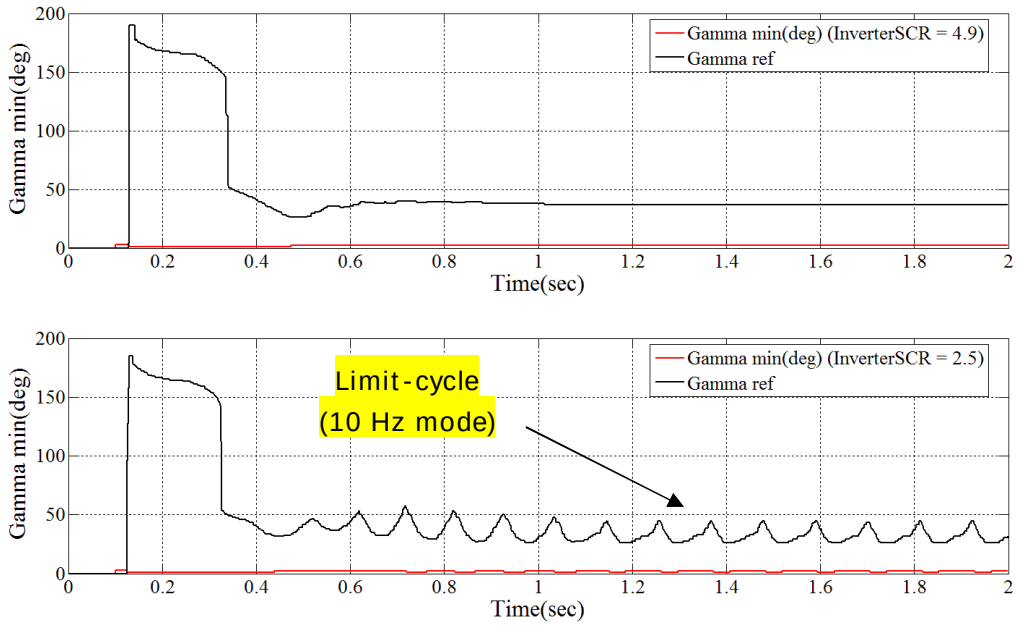

Figure 26 - Comparison between inverter SCR of 4.9 and 2.5: Gamma at Inverter

3. Multi-Terminal HVDC System

As shown in Figure 27, this multi-terminal HVDC system [8] includes eight (8) 12-pulse valve groups with converter transformers, smoothing reactors and generic controls. There are three HVDC converter stations. One station has four 12-pulse valve groups (two bipoles in parallel), and the other two stations have two 12-pulse valve groups (one bipole) each. In each station, there are sixteen (16) 3-phase AC filter sub-banks on the AC side and eight (8) branches of filter banks on the DC side (four at positive pole and four at negative pole) with breakers. The AC filter sub-banks are tuned to filter harmonics of 11th, 13th, and above 24th, and give 15 steps of VAR compensation. In each station, there are two SVCs (Static Var Compensators), six synchronous generators, and a grid source (represented by an ideal source via an impedance) connected to the AC side of the HVDC.

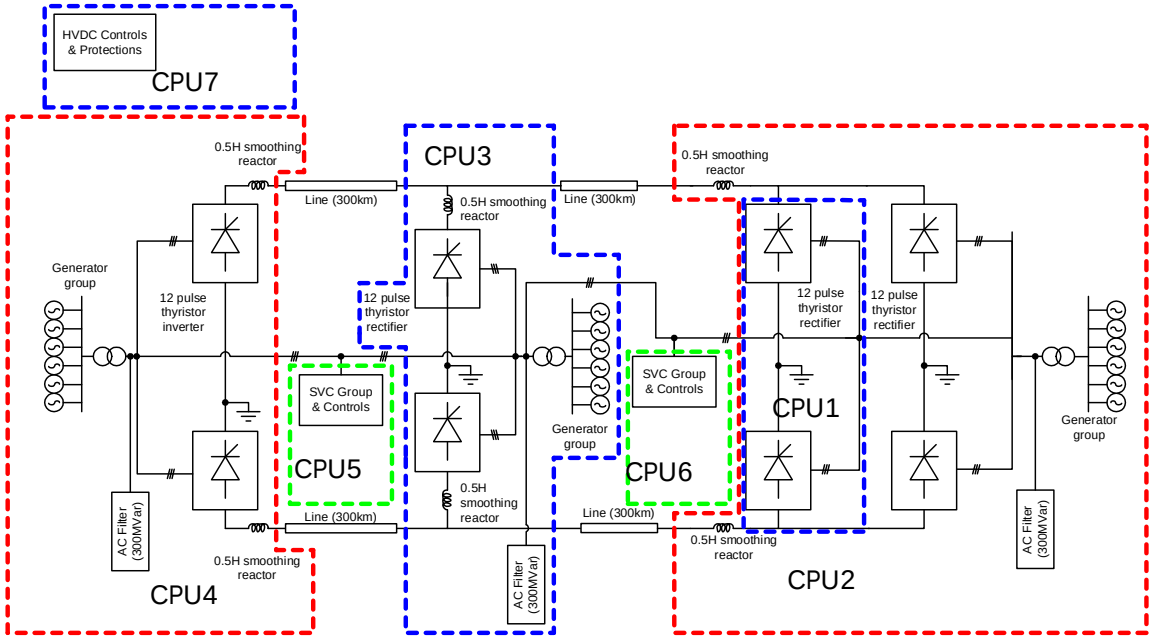

Figure 27 - Multi-terminal HVDC system

3.1 Model Distribution and Real-Time Performance

This multi-terminal HVDC model is used to verify the computational power of the simulator. The model is simulated in real-time using an **eMEGAsim** simulator. Model distribution and real-time performance are described in Table 6. The whole system is running at a hard real-time step of 50μs (without I/O). This model was distributed across **7 CPU cores**.

The first test is a performance indicator. The same model was also simulated on a Windows-based PC. As seen in Table 6, simulation on the Windows-based PC was shown to be 192.5 times slower than simulation on the **eMEGAsim** simulator (see the acceleration factor of the **eMEGAsim**), which means that it takes 192.5 "wall clock" seconds in offline mode, on a regular PC, to simulate 1 second of the model (real-time duration).

The second test is the minimum time step test, which is the minimum time step that the model can be simulated at without causing overruns (effective time step larger than the real-time clock's step). In this case, the multi-terminal HVDC system model could be run at a time step as low as 45 µs.

Finally, the third test is the calculation time of each parallel distributed part of the model was monitored. This value indicates the percentage of a real-time clock step that is needed by the **eMEGAsim** real-time simulation platform to solve the model equations. These values also indicate that idle time remains available that each processor could use to simulate further devices. Therefore, one can conclude that this model's complexity could be further augmented while maintaining very good real-time performance.

Table 6 – CPU Allocation and real-time performance for the multi-terminal HVDC system (table continued on next page)

CPU	Component Content	Model Calculation Time	Minimum time step	Acceleration factor[9][10]
CPU 1: HVDC station1, bipolar1	• 2 12-pulse thyristor rectifiers • 2 YgYD converter transformers • 5 DPL (½ decoupling)[11]	20 µs (40%) (50 µs Time-Step)	45 µs	192.5 (50 µs)
CPU 2: HVDC station1, bipolar2	• 2 12-pulse thyristor rectifiers • 2 YgYD converter transformers • 1 ideal 3-phase voltage source w equiv. network impedance • 6 synchronous generators • 2 smoothing reactors • 4 capacitor banks • 8 single-tuned AC filters	40 µs (80%) (50 µs Time-Step)		

[9] The **eMEGAsim** target computer used for the test is a dual Intel® Core™ 2 Quad processors, 2.3 GHz, 2 GB RAM

[10] The Windows-based PC station used for the test is an *Intel ® Core™ 2 Duo CPU, 2.53 GHz, 3 GB RAM*

[11] DPL: Distributed Parameter Line for model distribution; ½ the line is calculated in that CPU

CPU	Component Content	Model Calculation Time	Minimum time step	Acceleration factor[9][10]
	• 4 high-pass AC filters • 8 DC filters (RC branch) • 10 DPL (½ decoupling)[11]			
CPU 3: HVDC station2	• 2 12-pulse thyristor rectifiers • 2 YgYD converter transformers • 1 ideal 3-phase voltage source with equivalent network impedance • 6 synchronous generators • 2 smoothing reactors • 4 capacitor banks • 8 single-tuned AC filters (RLC branch) • 4 high-pass AC filters (parallel RL w series C) • 8 DC filters (RC branch) • 10 DPL (½ decoupling)[12]	40 µs (80%) (50 µs Time-Step)		
CPU 4: HVDC station3	• 2 12-pulse thyristor rectifiers • 2 YgYD converter transformers • 1 ideal 3-phase voltage source with equivalent network impedance • 6 synchronous generators • 2 smoothing reactors • 4 capacitor banks • 8 single-tuned AC filters (RLC branch) • 4 high-pass AC filters (parallel RL with series C) • 8 DC filters (RC branch) • 5 DPL (½ decoupling)[12]	40 µs (80%) (50 µs Time-Step)		
CPU 5: SVC 1~3	• 3 SVCs • 3 SVC transformers • 3 SVC controllers	35 µs (70%) (50 µs Time-Step)		

[12] DPL: Distributed Parameter Line for model distribution; ½ the line is calculated in that CPU

CPU	Component Content	Model Calculation Time	Minimum time step	Acceleration factor[9][10]
	• 6 DPL (½ decoupling)[12]			
CPU 6: SVC 4~6	• 3 SVCs • 3 SVC transformers • 3 SVC controllers • 6 DPL (½ decoupling)[12]	35 µs (70%) (50 µs Time-Step)		
CPU 7 HVDC controller	• HVDC controller for eight 12-pulse valve groups	45 µs (45%) (100 µs Time-Step)		

4. References

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