This controller hierarchy applies under the following initial conditions: at the end of the previous timestep, the collector-receiver was On and the power cycle was either Off or Starting Up

CR_ON / PC_SU / TES_OFF

q_CR_on + tol > q_PC_su_max — NO → CR_ON / PC_SU / TES_OFF

q_CR_on + tol > q_PC_su_max — YES → **CR_DF / PC_SU / TES_OFF**

q_TES_ch > 0 — NO → q_CR_on + tol > q_PC_su_max

q_TES_ch > 0 — YES ↓

(q_CR_on - q_TES_ch) + tol > q_PC_su_max — YES → **CR_DF / PC_SU / TES_FULL**

(q_CR_on - q_TES_ch) + tol > q_PC_su_max — NO ↓

q_CR_on + tol > q_PC_su_max — YES → **CR_ON / PC_SU / TES_CH**

q_CR_on + tol > q_PC_su_max — NO → **CR_ON / PC_SU / TES_OFF**

is_pc_su_ok — YES → (to CR_ON / PC_SU / TES_OFF)

is_pc_su_ok — NO ↓

1) q_CR_su > 0 2) is_rec_su_ok — YES → is_pc_su_ok

1) q_CR_su > 0 2) is_rec_su_ok — NO ↓

1) q_TES_dc > 0 2) is_pc_su_ok — NO → **CR_OFF / PC_SU / TES_DC**

1) q_TES_dc > 0 2) is_pc_su_ok — NO → **ALL OFF**

q_TES_ch > 0 — NO → **ALL OFF**

q_TES_ch > 0 — YES ↓

q_CR_on - tol < q_TES_ch — NO → **CR_DF / PC_OFF / TES_FULL**

q_CR_on - tol < q_TES_ch — YES → **CR_ON / PC_OFF / TES_CH**