This controller hierarchy applies under the following initial conditions: at the end of the previous timestep, the collector-receiver was Off or Starting Up and the power cycle was either On or in Standby

1) q_CR_su > 0 / 2) is_rec_su_ok

— YES → **1) is_pc_su_ok / 2) is_pc_SB_ok**
- NO → CR_SU / PC_OFF / TES_OFF
- YES → **1) is_pc_su_ok / 2) q_TES_dc_t_CR_su + tol > q_PC_target**
  - YES → CR_SU / PC_TARGET / TES_DC
  - NO → **1) is_pc_su_ok / 2) q_TES_dc_t_CR_su + tol > q_PC_min**
    - YES → CR_SU / PC_RM_LO / TES_EMPTY
    - NO → **1) is_pc_SB_ok / 2) q_TES_dc_t_CR_su + tol > q_PC_sb**
      - YES → CR_SU / PC_SB / TES_DC
      - NO → **1) is_pc_su_ok / 2) q_TES_dc > 0**
        - YES → CR_SU / PC_MIN / TES_EMPTY
        - NO → CR_SU / PC_OFF / TES_OFF

— NO → **1) is_pc_su_ok / 2) is_pc_SB_ok**
- NO → ALL OFF
- YES → **1) is_pc_su_ok / 2) q_TES_dc + tol > q_PC_target**
  - YES → CR_OFF / PC_TARGET / TES_DC
  - NO → **1) is_pc_su_ok / 2) q_TES_dc + tol > q_PC_min**
    - YES → CR_OFF / PC_RM_LO / TES_EMPTY
    - NO → **1) is_pc_SB_ok / 2) q_TES_dc + tol > q_PC_sb**
      - YES → CR_OFF / PC_SB / TES_DC
      - NO → **1) is_pc_su_ok / 2) q_TES_dc > 0**
        - NO → ALL OFF
        - YES → CR_OFF / PC_MIN / TES_EMPTY