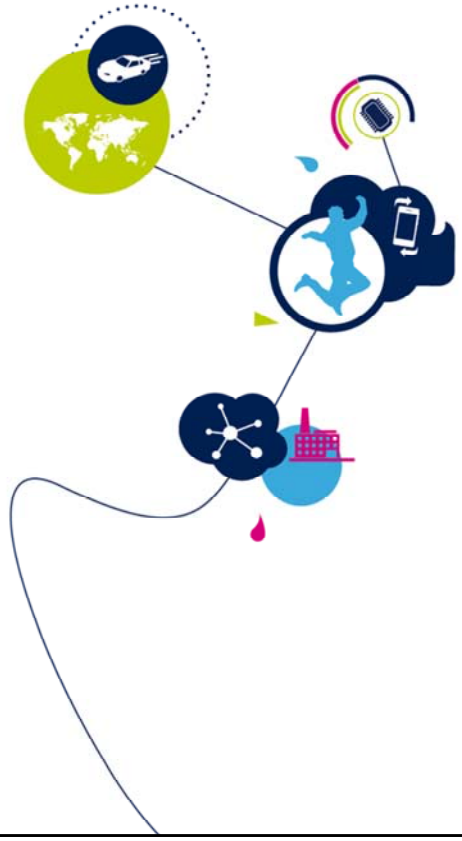
STM32G4 - PWR

Power control

Revision 1.0



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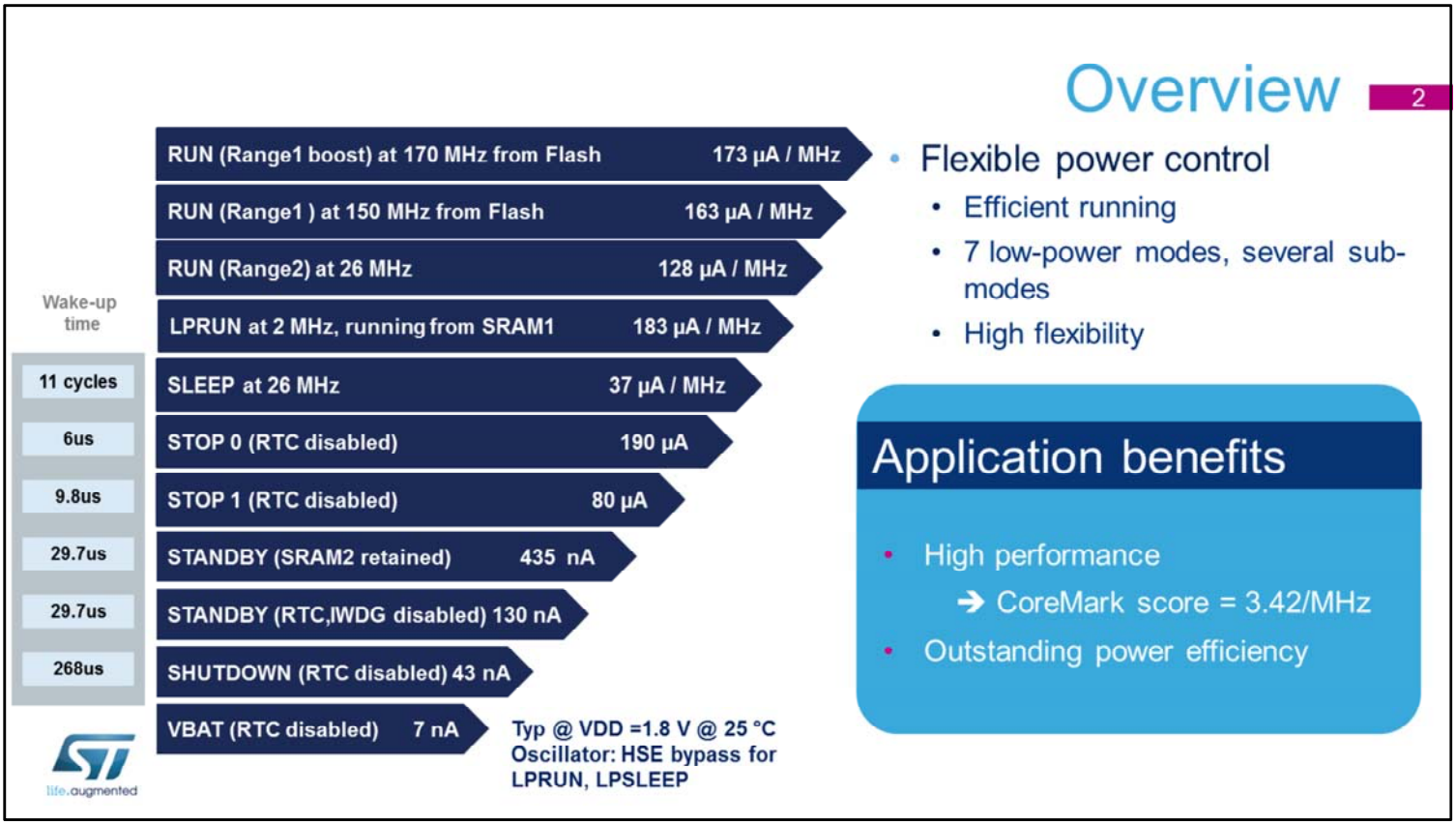
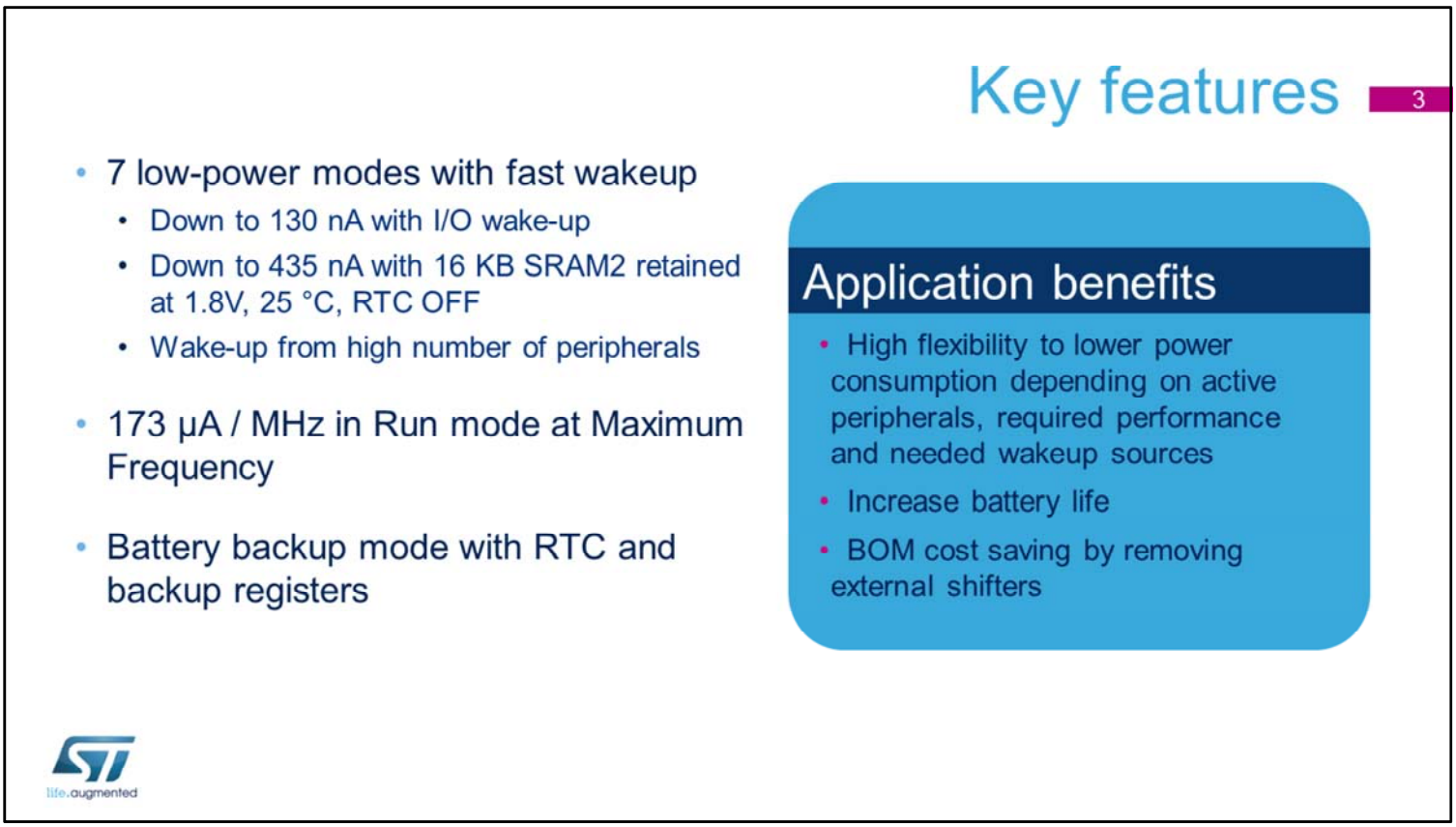
Hello, and welcome to this presentation of the STM32G4 power controller. The STM32G4's power management functions and all low power modes are also be covered in this presentation.



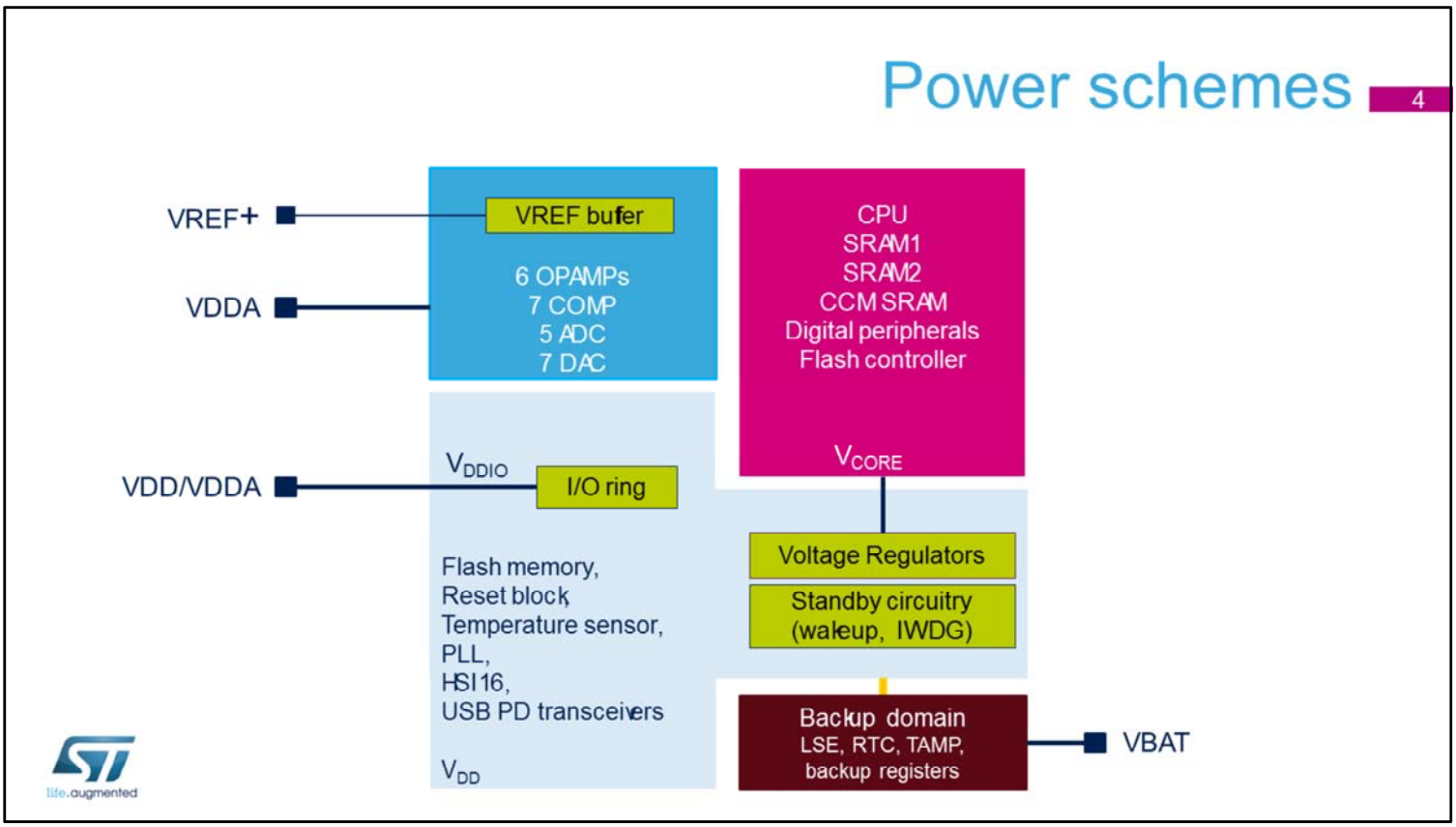
STM32G4 devices feature a flexible power control, which increases flexibility in power mode management and further reduces the overall application consumption.
This slide details the consumption in the various power modes for the STM32G474.
Run mode can support a system clock running at up to 170 MHz, with only 173 µA/MHz.
At 26 MHz, the consumption is even lower: 128 µA/MHz.
STM32G4 devices support 7 main low-power modes: Low-power run, Sleep, Low-power sleep, Stop 0, Stop 1, Standby and Shutdown modes.
Each mode can be configured in many ways, providing several additional sub-modes.
In addition, STM32G4 devices support a battery backup domain, called VBAT.
The high flexibility in power management provides both high performance with a CoreMark score equal to

3.42/MHz, together with an outstanding power efficiency.



The STM32G4 has several key features related to power management:
Several low-power modes, down to 130 nA while it is still possible to wake up the MCU with an event on an I/O.
For only 435 nA, 16 kilobytes of SRAM can be retained assuming a 1.8V VDD power supply.
A large number of peripherals can wake up from the various low-power modes.
Dynamic consumption is down to 128 µA/MHz, executing from Flash memory.
A battery backup domain, called VBAT, includes the RTC and the backup registers.
Several power supplies are independent, enabling the reduction of the MCU power consumption while some peripherals are supplied at higher voltages.
Thanks to the large number of power modes, STM32G4 devices offer high flexibility to minimize the power

consumption and adjust it depending on active peripherals, required performance and needed wake-up sources.



STM32G4 devices have several independent power supplies, which can be set at different voltages or tied together. The main power supply is VDD, supplying almost all I/Os except those part of the VBAT domain . VDD also supplies the flash memory, the reset block, temperature sensor and all internal clock sources. In addition, it supplies the Standby circuitry which includes the wakeup logic and independent watchdog.
VDD supplies voltage regulators which provide the VCORE supply.
VCORE supplies most of the digital peripherals, SRAMs and Flash memory controller.
VDDA voltage supplies the analog peripherals.
The VREF+ pin provides the reference voltage to the analog-to-digital and to digital-to-analog converters.
It is also the output of the internal voltage reference buffer when enabled.

A backup battery can be connected to VBAT pin to supply the backup domain.

Power schemes

- **Optimized power and performance thanks to independent power supplies**
  - V_{DD} from 1.71 to 3.6 V (down to 1.6 V at power-down)
    - VDD must be set if any other independent supply is provided
  - V_{DDA} from 1.62 to 3.6 V
    - 1.62 V minimum when ADCs or COMPs are used
    - 1.71 V minimum when DACs are used
    - 2.0 V when OPAMPs are used
    - 2.4 V minimum when VREFBUF is used
  - V_{REF+} = V_{DDA} when V_{DDA} < 2 V and from 2V to V_{DDA} when V_{DDA} > 2 V
  - V_{BAT} from 1.55 to 3.6V for power domain including the RTC block and TAMP block, which contain the 128-byte backup registers

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The main power supply VDD ensures full feature operation in all power modes from 1.71 up to 3.6 V, enabling it to be supplied by an external 1.8 V regulator. Device functionality is guaranteed down to 1.6 V, the minimum voltage after which a power-down reset is generated. Other independent supplies are provided to enable peripherals to operate at a different voltage.
VDDA is the external analog power supply for Analog to Digital converters, Digital to Analog converters, voltage reference buffer, operational amplifiers and comparators.
When the analog-to-digital converters or comparators are used, the VDDA voltage must be greater than 1.62 V.
When the digital-to-analog converters are used, VDDA must be greater than 1.71 V.
When the operational amplifiers are used, VDDA must be greater than 2.0 V
When the voltage reference buffer is used, VDDA must

be greater than 2.4 V.
A backup domain is supplied by VBAT, which must be greater than 1.55 V. The backup domain contains the RTC, the 32.768-kHz LSE external oscillator and the Tamp block containing the 128-byte backup registers.

Power schemes

Independent voltage reference supplies for analog performance

- VREF+: reference voltage for ADC and DAC
  - It can be provided either by an external reference voltage or by the internal voltage reference buffer (VREFBUF)
  - VREF+ pin, and thus the internal voltage reference, is not available on the 32-pin package
    - On those packages, this pin is double-bonded with VDDA
    - The internal voltage reference buffer is thus not available and must be kept disabled
  - Two VREF+ pins in the LQFP128 package

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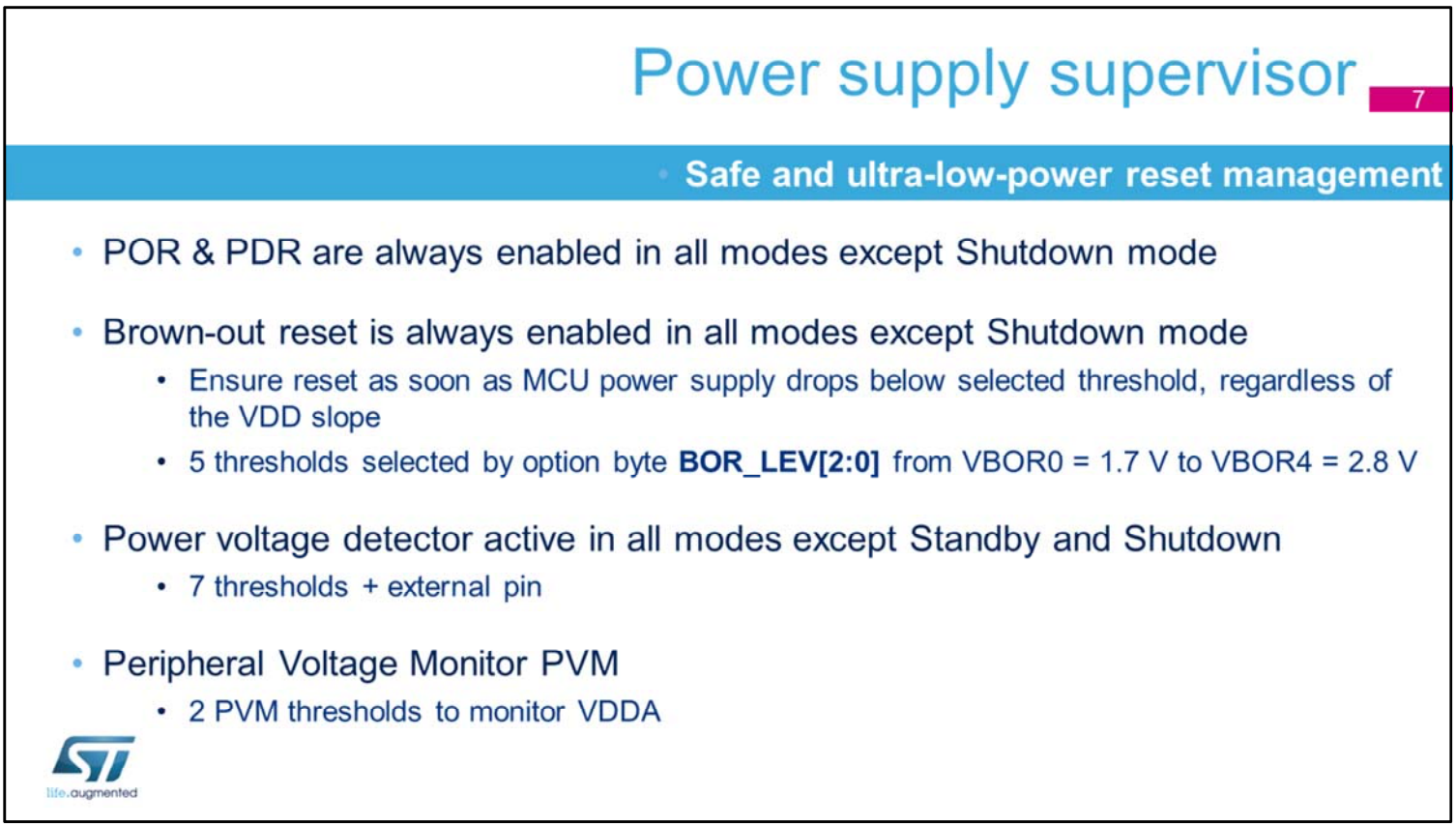
The ADC and DAC voltage references can be provided either by an external supply voltage or by the internal reference buffer.
This improves the performance of the converters by providing an isolated and independent reference voltage.
The VREF+ pin and thus the internal voltage reference, is not available on 32-pin packages.
In those packages, the VREF+ pin is double-bonded with VDDA and the internal voltage buffer must be kept disabled.
The voltage reference can be provided through the VDDA pin in those packages.
LQFP128 package has two VREF+ pins.

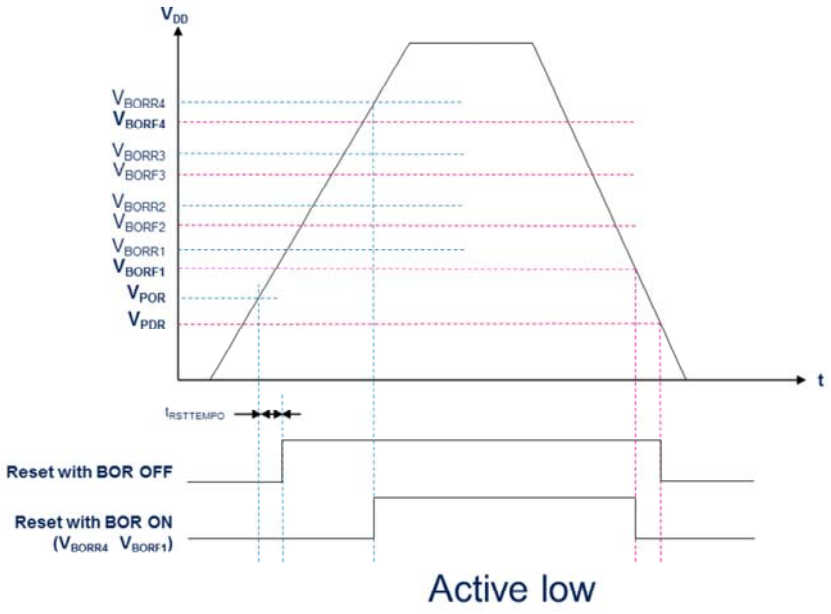


The power supply supervisor guarantees a safe and ultra-low power reset management.
STM32G4 devices embed a Power-On Reset (or POR) and a Power-Down Reset (PDR) which are always enabled in all power modes except Shutdown mode.
The Brown-Out reset (or BOR) ensures reset generation as soon as the MCU power supply drops below the selected threshold, regardless of the VDD slope. Four thresholds from 1.7 to 2.8 V can be selected by option byte programmed in Flash memory.
A Power Voltage Detector (or PVD) can generate an interrupt when VDD crosses the selected threshold. The PVD can be enabled in all modes except Standby and Shutdown modes. The threshold is selected by software among seven possible values.
In addition, comparisons can be done between VREFINT and the PVD_IN external pin.

The VDDA power supply can be independent from VDD and can be monitored with two Peripheral Voltage Monitoring (or PVM).

Brown Out and Power On/Down Reset

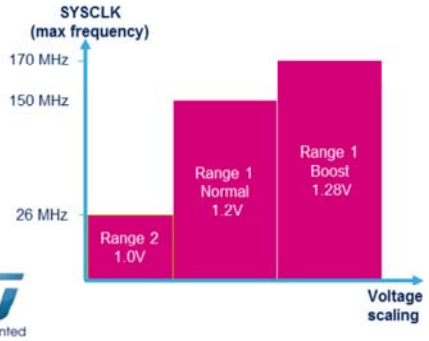
- The Brown-out reset is asserted when VDD is below a programmable threshold
- POR/PDR are always On, except in shutdown mode

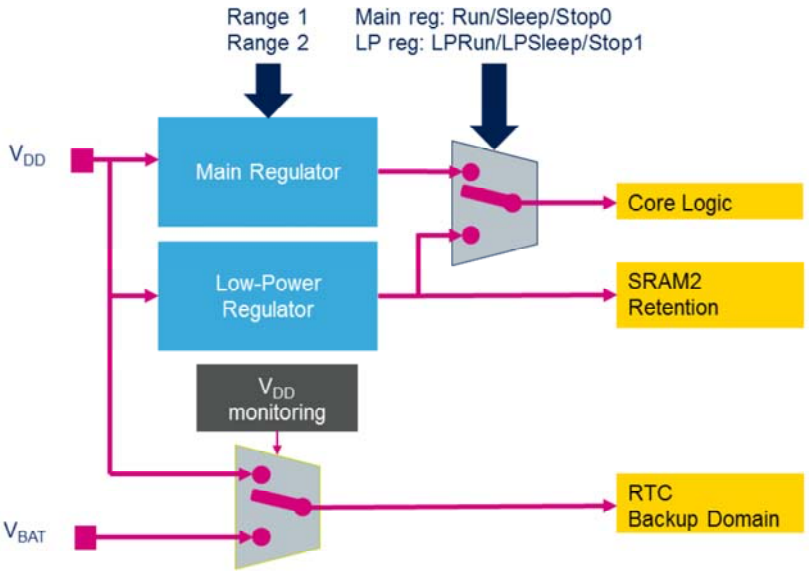


The Power reset (BOR and POR) resets all registers except those in the Backup domain powered by VBAT which contains the RTC and TAMP blocks and the external low-speed oscillator LSE.
When exiting Standby mode, all registers powered by the Main regulator are reset.
When exiting Shutdown mode, a Power reset is generated.
Five BOR levels can be selected through option bytes.
During power-on, the BOR keeps the device under reset until the supply voltage VDD reaches the specified VBORx threshold. When VDD drops below the selected threshold, a device reset is generated.
When VDD is above the VBORx upper limit, the device reset is released and the system can start.

Voltage regulators

- Two Voltage Regulators
  - One Main regulator with two voltage ranges for Dynamic Voltage Scaling; used in Run, Sleep and Stop 0 modes
  - One Low-power regulator for Low-power run, Low-power sleep and Stop 1 modes as well as for RAM retention in Standby mode



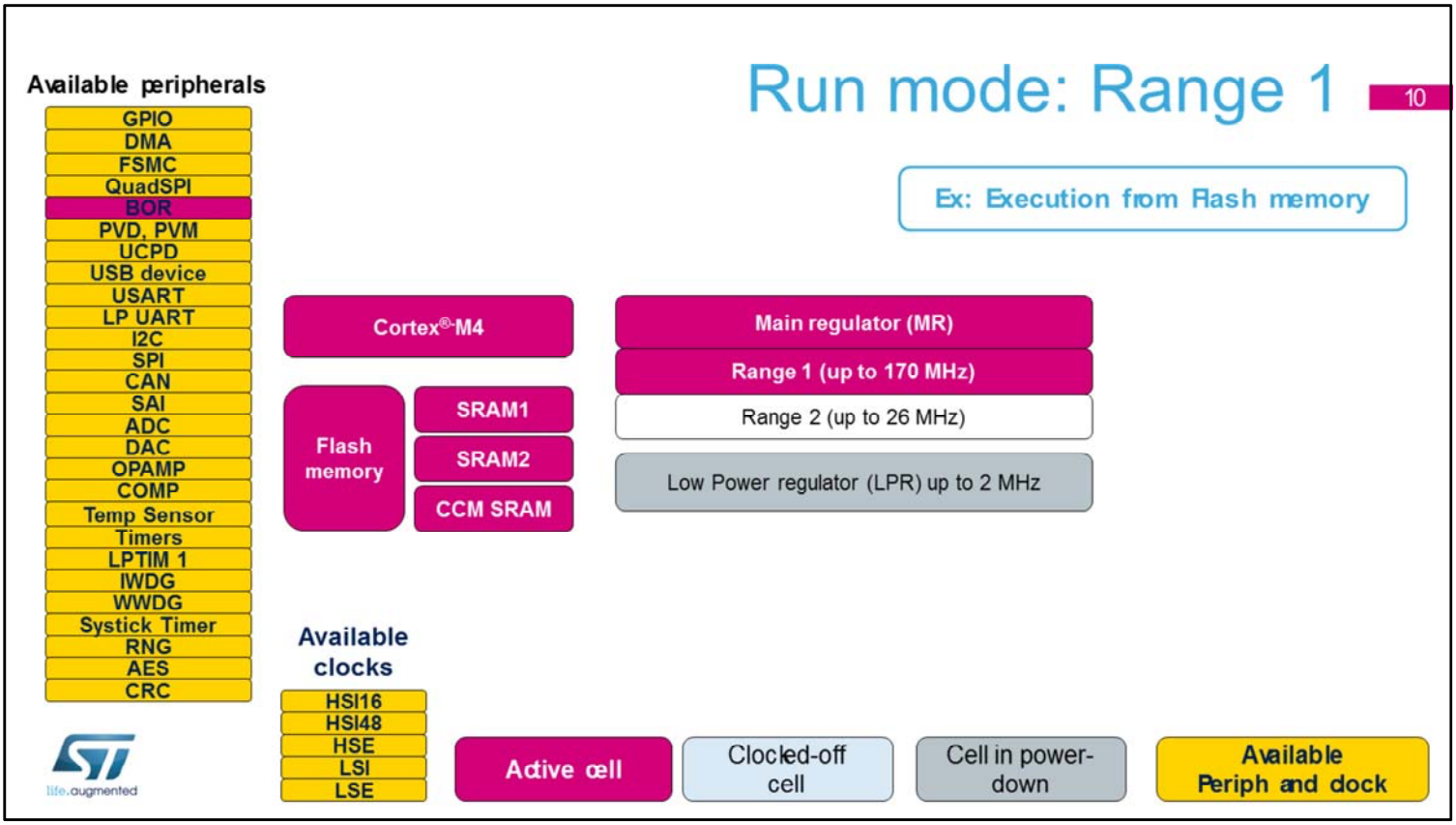


Two embedded linear voltage regulators supply all the digital circuitries except for the Standby circuitry and the Backup domain. The regulator output voltage (V_{CORE}) can be programmed by software to two different values depending on the performance and the power consumption requirements. This is called Dynamic Voltage Scaling.

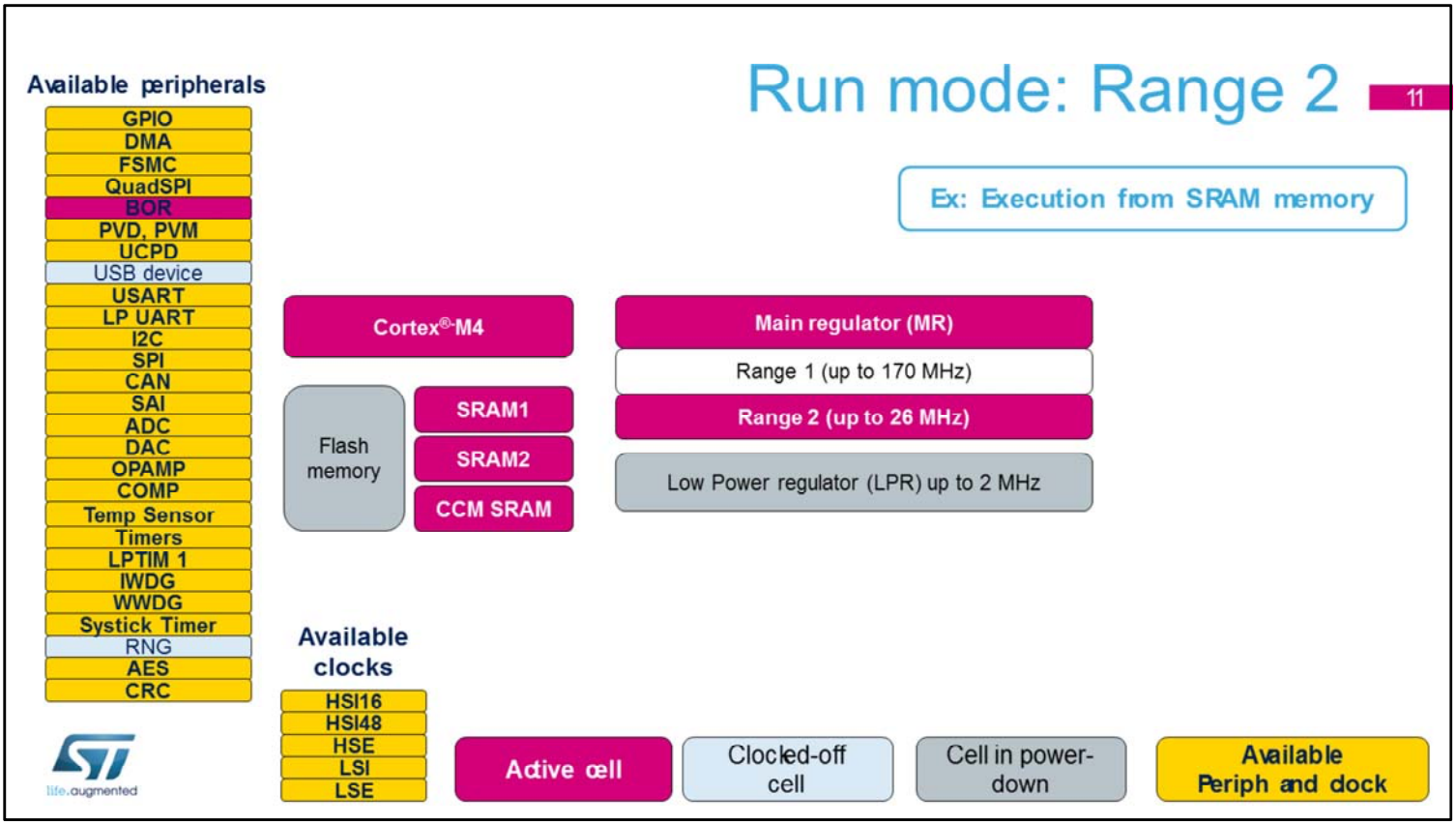
The figure on the left indicates the Vcore voltage level required according to the frequency.

Depending on the application mode, V_{CORE} is provided either by the Main voltage regulator for Run, Sleep and Stop 0 modes, or by the Low-power regulator for Low-power run, Low-power sleep, Stop 1 modes.

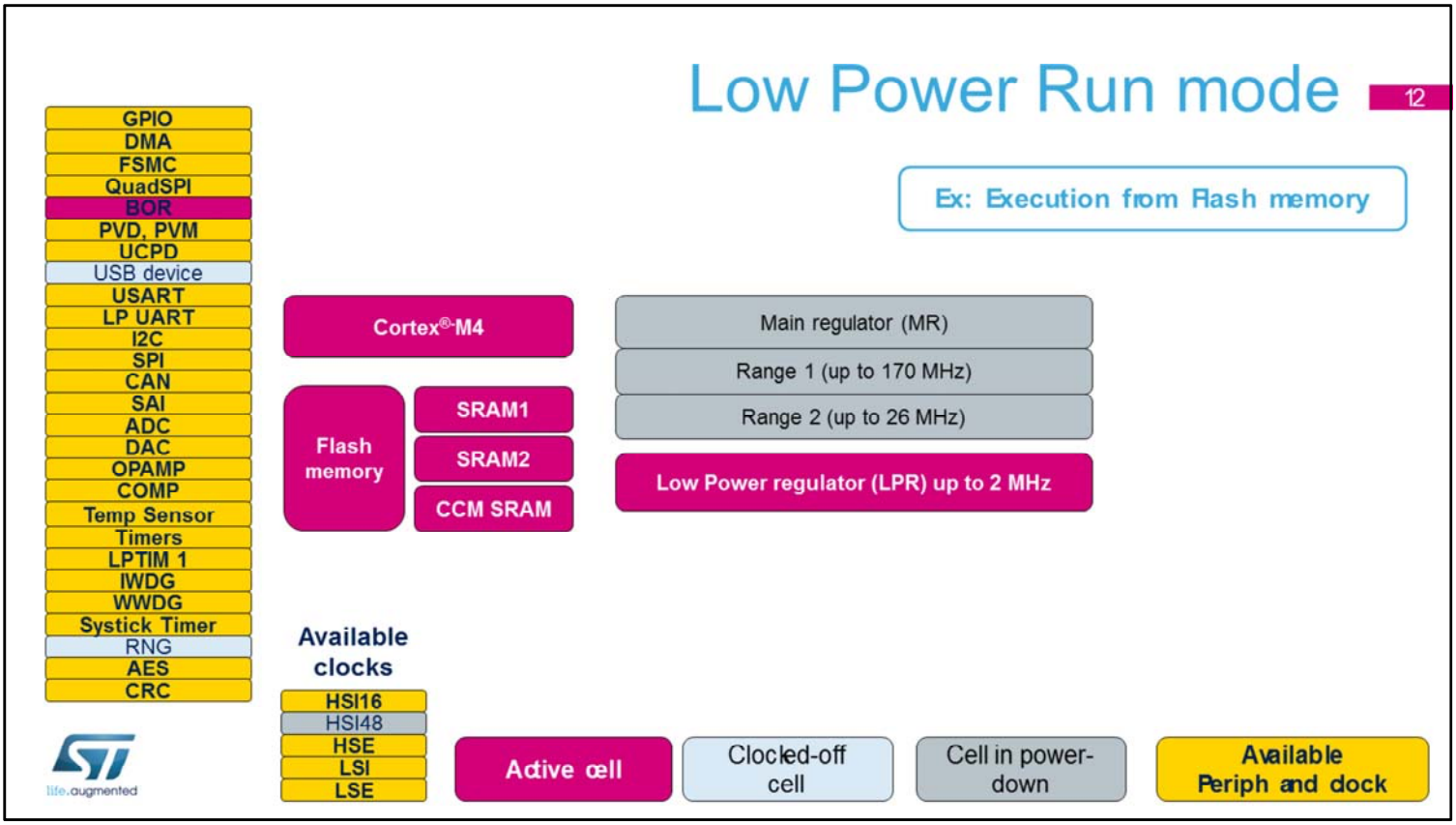
The regulators are OFF in Standby and Shutdown mode. When SRAM2 content is preserved in Standby mode, the Low-power regulator remains ON and provides the SRAM2 supply.



In Run mode, the CPU is clocked and program can be executed from FLASH or SRAM Memory.
In Range 1, the system clock is up to 170 MHz, in Range 2 it is up to 26 MHz.
By default, the SRAM clocks are enabled. They can be individually gated off during Sleep mode by software.
All peripherals can be activated in Range 1.



In Run mode, the voltage scaling Range 2 is the medium performance range, enabling a system clock up to 26 MHz.
When executing from SRAM, the Flash consumption can be saved by configuring the Flash in Power-down mode and by gating its clock off.
All peripherals can be activated except the USB device and Random Number Generator.
All clocks can be enabled.



In Low Power Run mode, the CPU is clocked and program can be executed from FLASH or SRAM, additionally the FLASH can be completely unpowered to save power.
The system clock is limited to 2 MHz.
The Main Regulator is switched off and supply to digital blocks is provided by the Low Power Regulator.
In Low Power mode, all peripherals except the USB device and Random Number Generator can be active.

Run and Low-power run modes

Flexibility between required performance and consumption

Voltage range		SYSCLK	HSI16	HSE	PLL
Range 1	Boost	170 MHz max	16 MHz	48 MHz	170 MHz
	Normal	150 MHz			150 MHz
Range 2		26 MHz max	16 MHz	26 MHz	26 MHz
Low-power run		2 MHz max	Allowed with divider	Allowed with divider	Not allowed

The Run mode, thanks to voltage scaling, and the Low-power run mode, offer flexibility between required performance and consumption.
In Run mode range 1 when boost mode is active, the system clock is limited to 170 MHz and the internal and external oscillators and the PLL can be used.
In Run mode range 1 when boost mode is disabled, the system clock is limited to 150 MHz and the internal and external oscillators and the PLL can be used.
In Run mode range 2, the system clock is limited to 26 MHz and the internal and external oscillators as well as the PLL can be used, but must be limited to 26 MHz.
In Low-power run mode, the system clock must be limited to 2 MHz.

Run and Low-power run modes

- Each peripheral clock can be configured to be ON or OFF
  - After reset, all peripheral clocks are OFF, except Flash interface clock
  - SRAM clocks are always ON in Run mode
- When running from SRAM (in Run or Low-power run):
  - Flash memory can be put in Power-down mode (only in Low-Power run)
  - Flash interface clock can be switched off
  - Interrupt vectors must then be re-mapped to SRAM

Each peripheral clock can be configured to be ON or OFF in Run and Low-power run modes.
By default all peripherals clocks are OFF, except the Flash interface clock.
The SRAM clock is always ON in Run mode.
When running from SRAM (in Run or Low-power run modes), the Flash memory can be put in Power-down mode thanks to software, and the Flash clock can be switched off.
The Flash memory must not be accessed when it is switched off, consequently interrupt vectors must be mapped in SRAM, using the Cortex-M4 Vector Table Offset Register.

Run and Low-power run modes

- Current consumption in Run mode depends on several parameters:
  - Executed binary code (program itself + compiler impact)
  - Program location in memory (depending on address of executed code)
  - Device configuration (depending on application)
  - I/O pin loading and switching rate
  - Temperature
  - Execution from Flash memory or SRAM
    - When execution from Flash memory: Accelerator configuration (Cache, Prefetch)
    - ➢ Energy efficiency better with Prefetch + Cache ON
    - When execution from SRAM:
    - ➢ Energy efficiency better versus Flash

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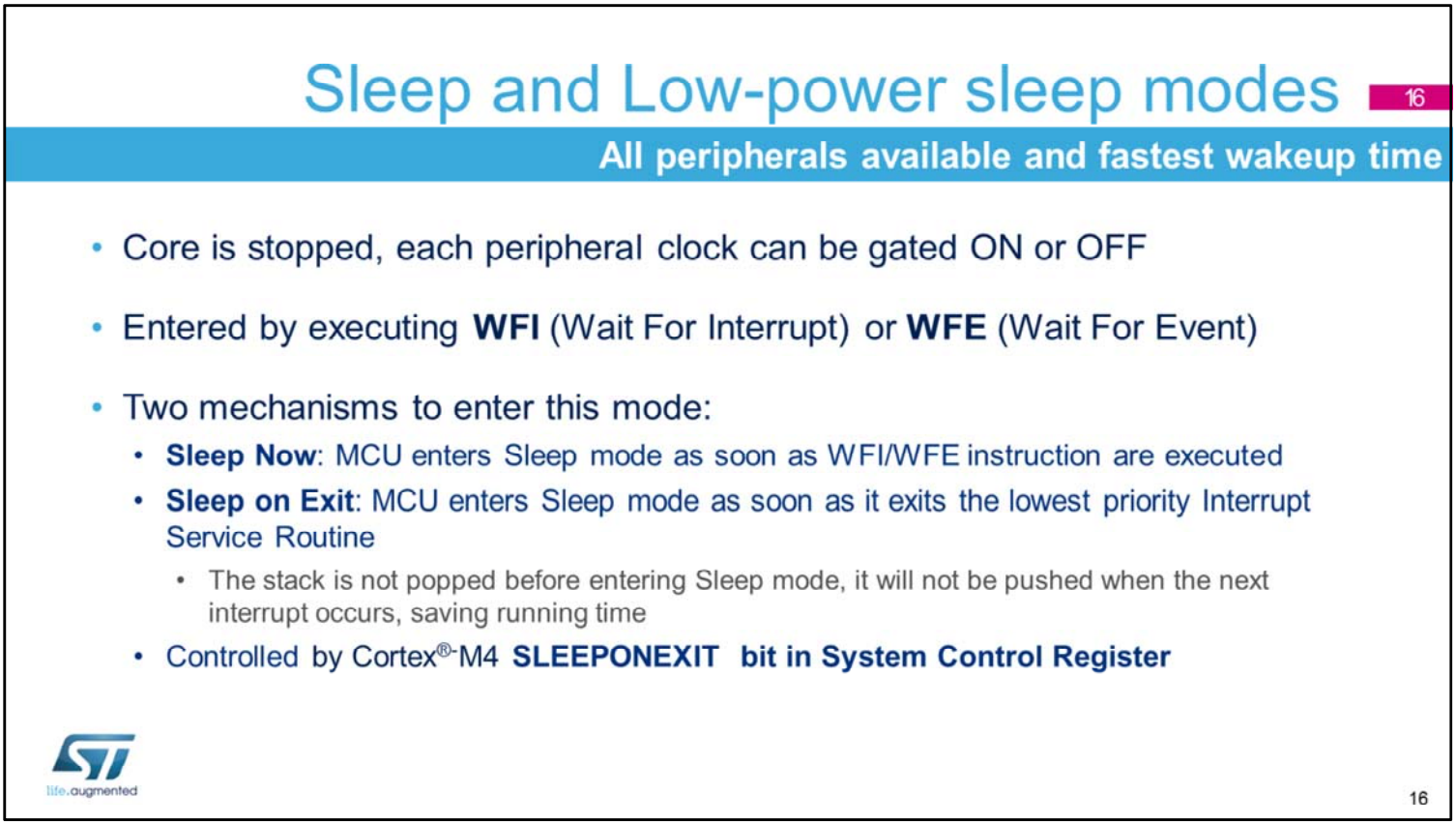
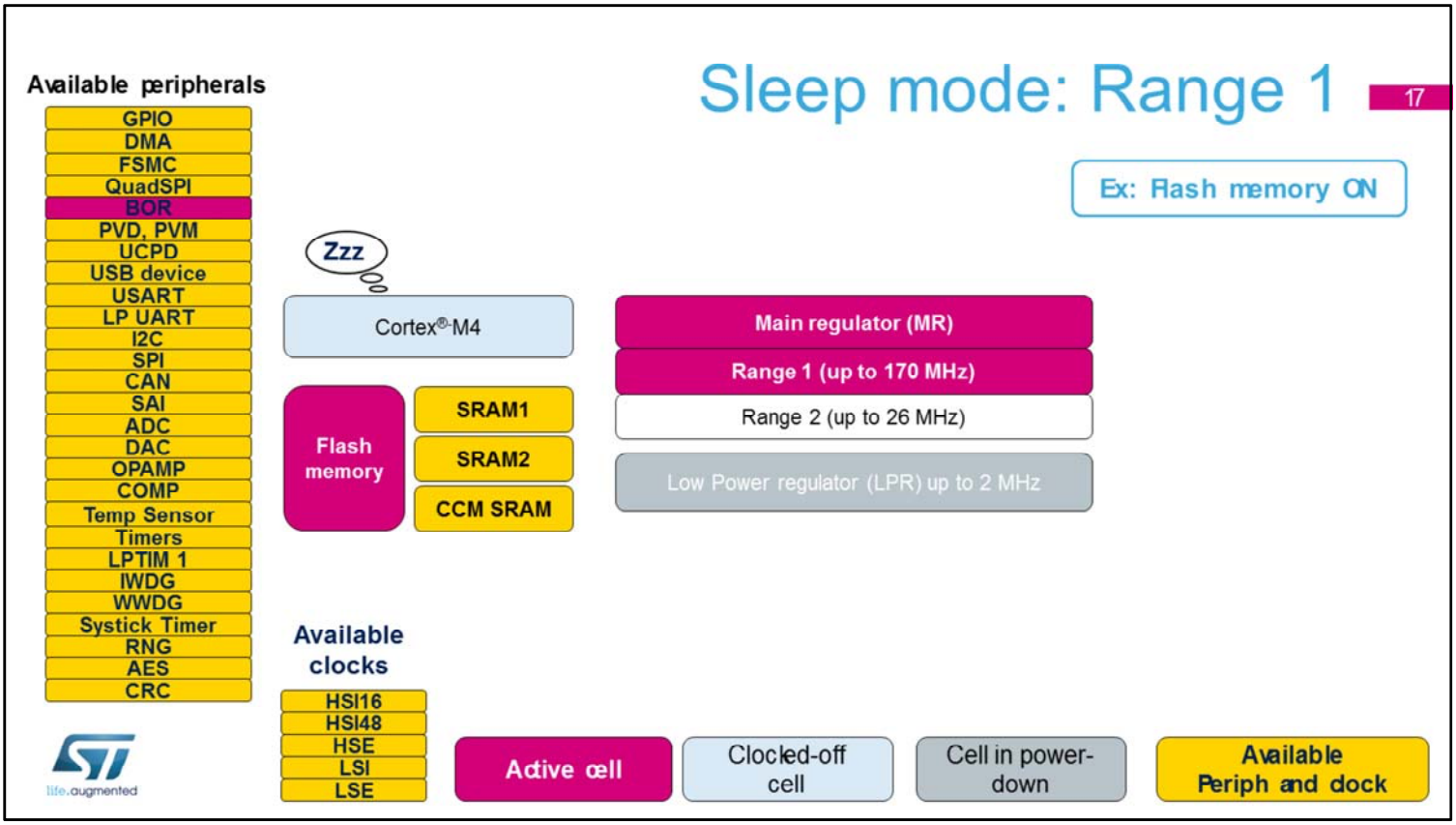
The current consumption in Run or Low-power run modes depends on several parameters: first the executed binary code, that means the program itself plus the compiler impact. Then it depends on the program location in the memory, the device software configuration, the I/O pin loading and switching rate and the temperature.
The consumption also depends on whether the code is executed from Flash memory or from SRAM. Energy efficiency is better when the Flash prefetch and the instruction cache are enabled . Executing from flash consumes more than executing from SRAM because the flash memory belongs to the VDD power domain while the SRAM belongs to the Vcore power domain.

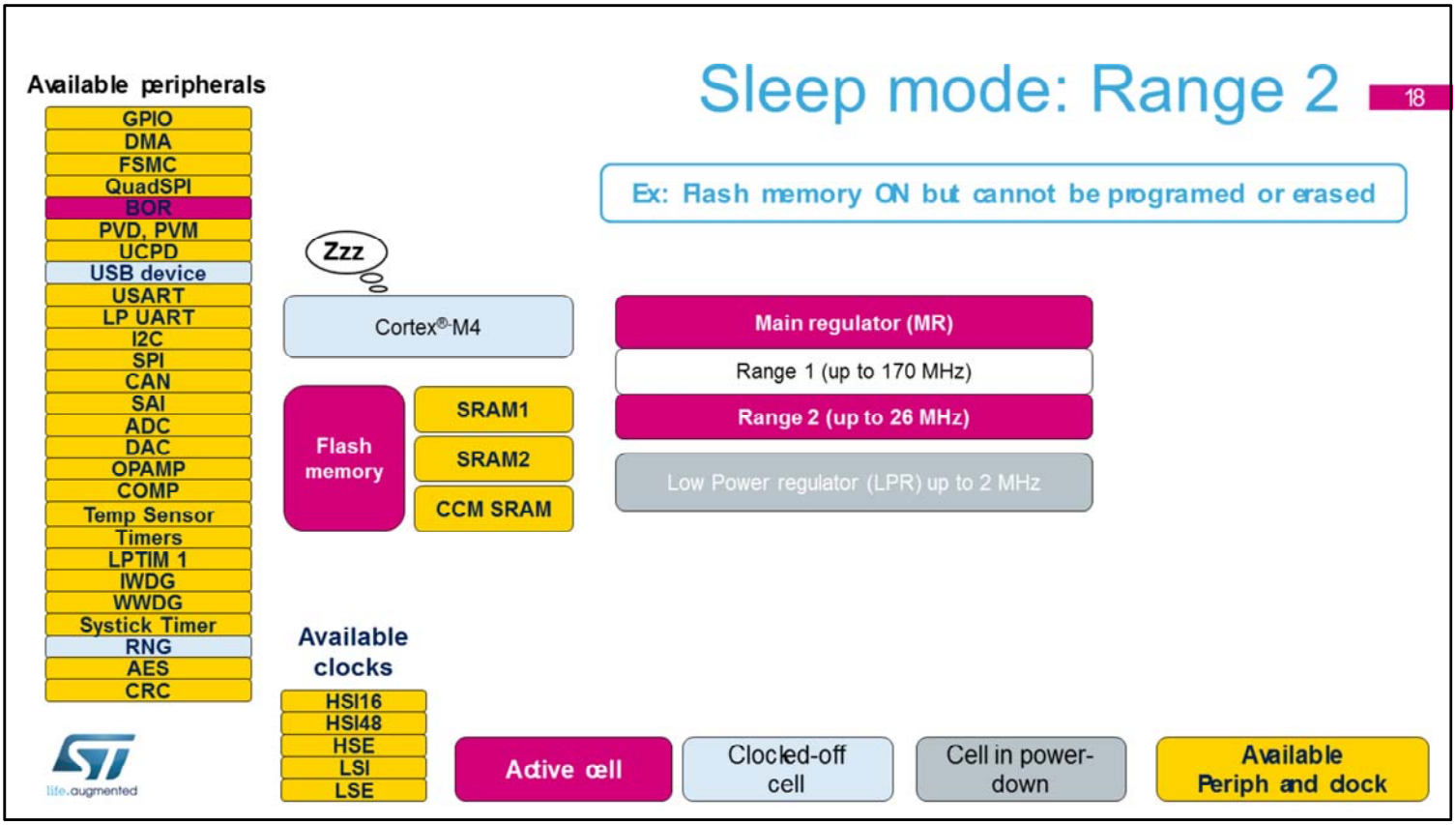


Sleep and Low-power sleep modes enable all peripherals to be used and features the fastest wakeup time.
In these modes, the CPU is stopped and each peripheral clock can be configured by software to be gated ON or OFF during the Sleep and Low-power sleep modes.
These modes are entered by executing the assembler instruction Wait for Interrupt (or WFI) or Wait for Event (or WFE). When executed in Low-power run mode, the device enters Low-power sleep mode.
Depending on the SLEEPONEXIT bit configuration in the Cortex®-M4 System Control Register, the MCU enters Sleep mode as soon as the instruction is executed, or as soon as it exits the lowest priority Interrupt Sub Routine.
This last configuration saves time and consumption by avoiding the need to pop and push the stack when exiting the low power mode. However all computations

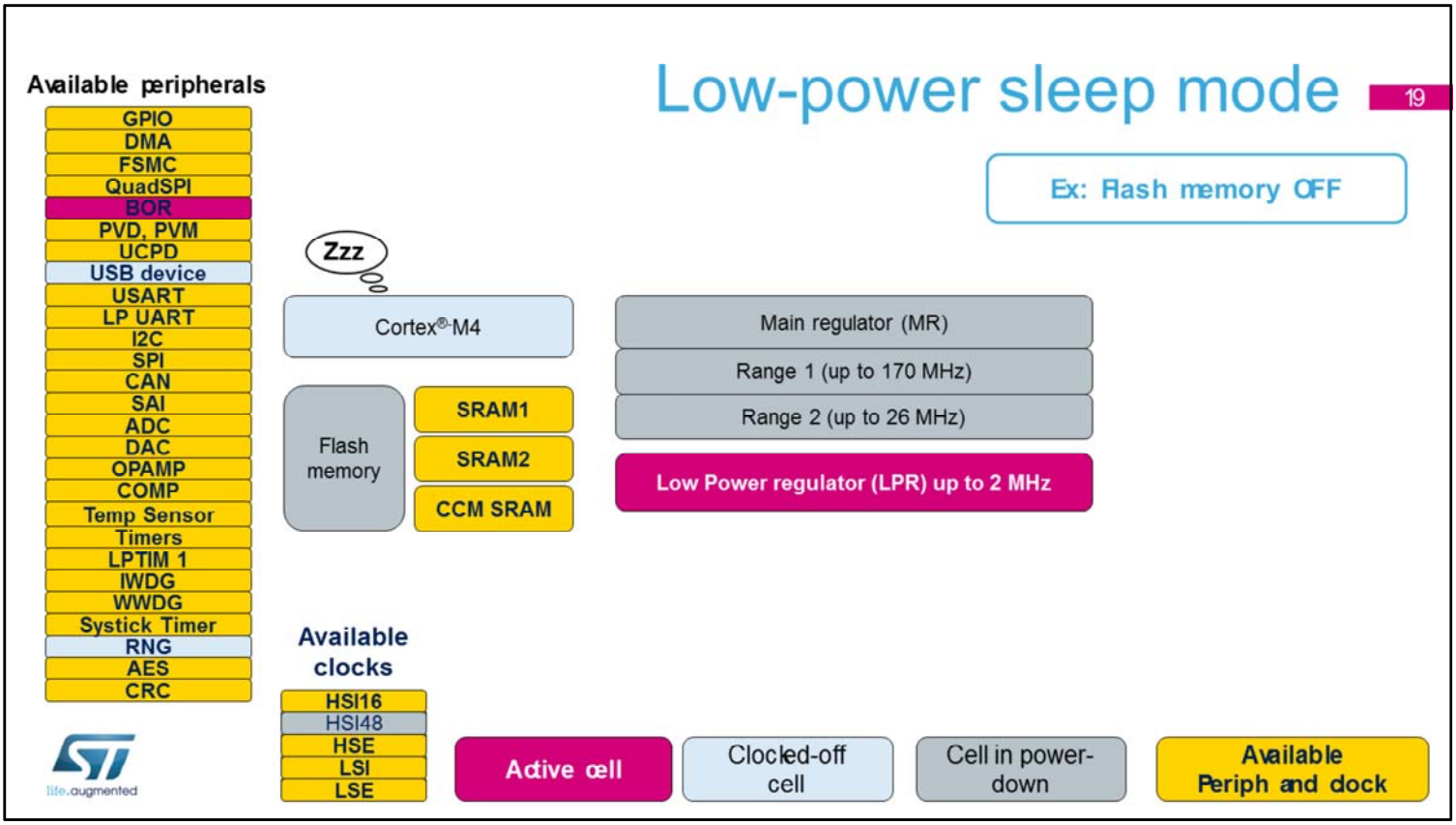
must be done in Cortex®-M4 handler mode, because the thread mode is no longer used .



In Sleep mode, the CPU clocks are OFF.
In Range 1, the system clock is up to 170 MHz, in Range 2 it is up to 26 MHz.
By default, the SRAM clocks are enabled.
They can be individually gated off during Sleep mode by software.
All peripherals can be activated in Range 1.



In Sleep mode Range 2, all peripherals can be activated except the USB device and Random Number Generator.



In Low-power sleep mode, the CPU clock is OFF and the logic is supplied by the low-power regulator. The system clock is up to 2 MHz.
Flash memory can be configured in Power down and can be gated off; SRAMs can be gated off.
All peripherals can be activated except the USB OTG and Random Number Generator.

Stop modes

Lowest power modes with full retention, 5 µs wakeup time to 16 MHz

- SRAM1, SRAM2, CCM SRAM and all peripheral registers retention
  - All high-speed clocks are stopped
  - Flash can be switched OFF
- LSE (32.768 kHz external oscillator) and LSI (32 kHz internal oscillator) can be enabled
- Several peripherals can be active and wake up from Stop modes
- System clock at wakeup is HSI16
- Stop 1 is equivalent to Stop 0 with Main Regulator off, resulting in a smaller current consumption but longer wake up time

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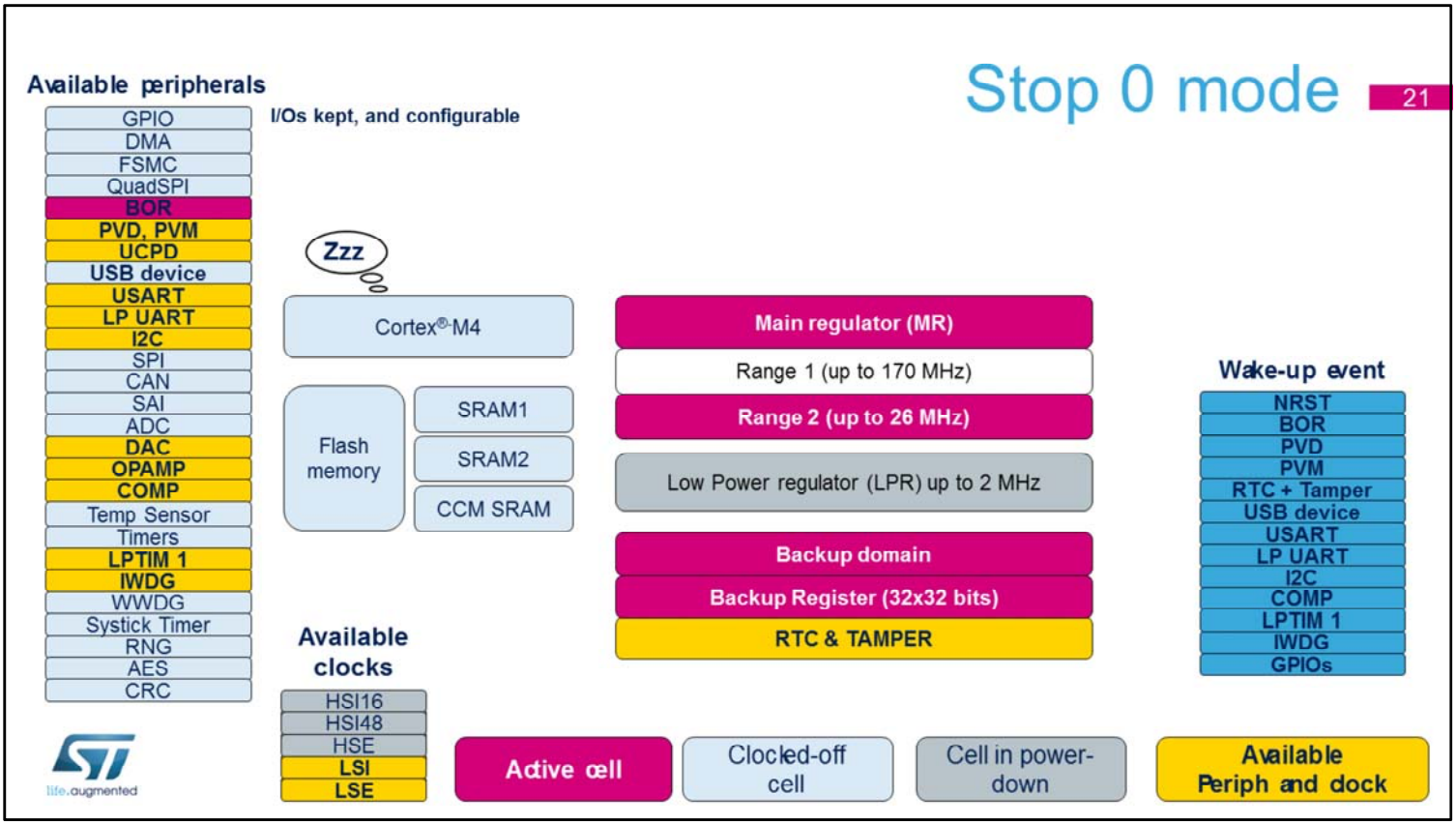
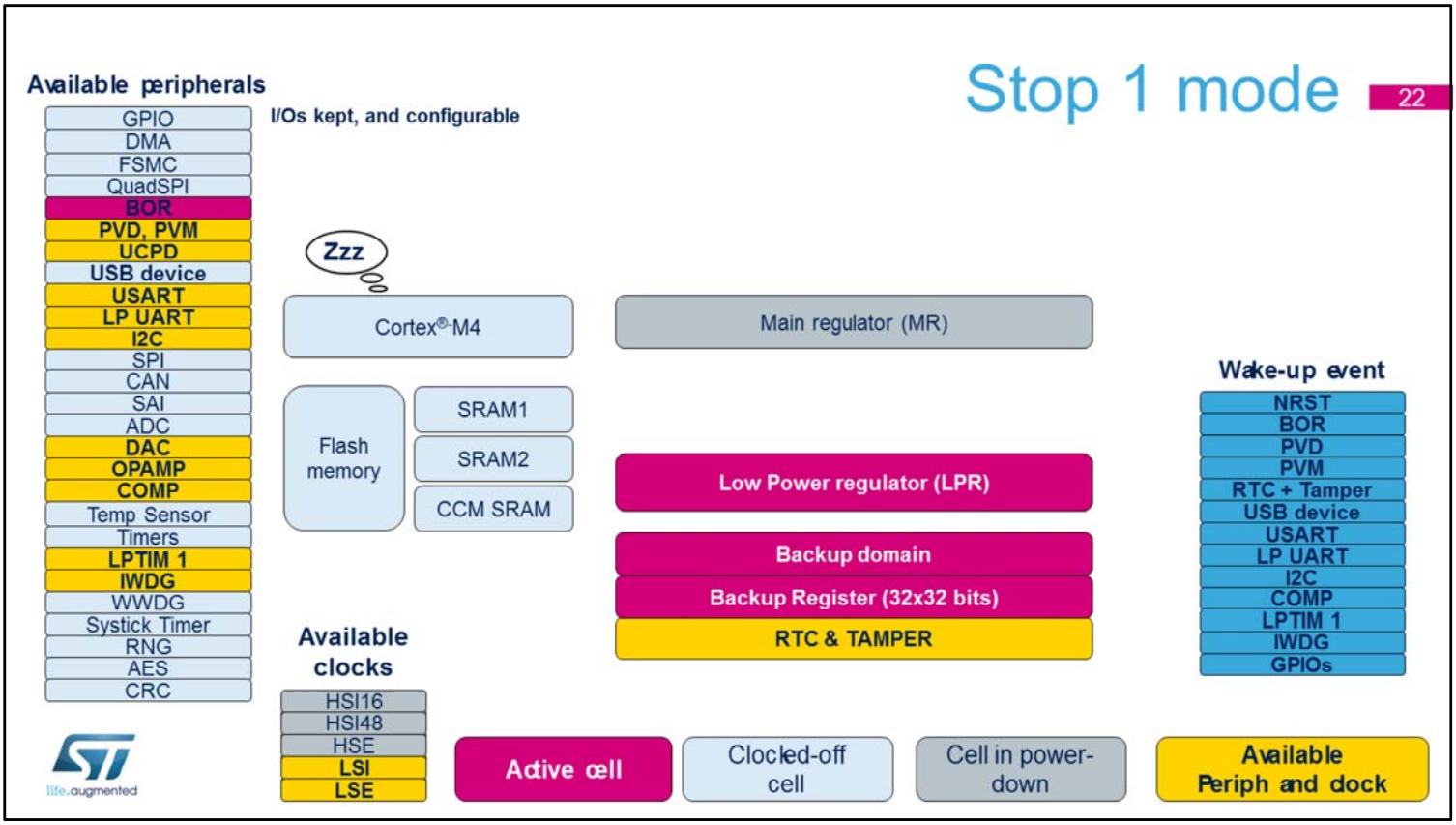
STM32G4 devices features two Stop modes: Stop 0, and 1, which are the lowest power modes with full retention and only a few µs wakeup time to Run mode at 16 MHz.
The contents of SRAM and all peripherals registers are preserved in Stop modes.
All high speed clocks are stopped.
The 32.768 kHz external oscillator and 32 kHz internal oscillator can be enabled.
Several peripherals can be active and wake up from Stop mode.
System clock on wake-up is the internal high-speed oscillator at 16 MHz.
Stop 1 is similar to Stop 0 with the Main regulator switched OFF.



The voltage regulator is configured in main regulator mode
All clocks in the VCORE domain are stopped; the PLL and the HSE oscillators are disabled.
The RTC, clocked by the internal or external low-speed oscillator, can remain active.
The brown-out reset is always enabled. Most of the peripheral clocks are gated off.
Several peripherals can be functional in Stop 0 mode: Power voltage detector, Peripheral Voltage Monitor, digital to analog converters, operational amplifiers, comparators, independent watchdog, low power timer, I2C, UART and low-power UART, and UCPD.
The events from all I/Os can wake up from Stop 0 mode, as well as the interrupt generated by the active peripherals. The I2C, UART , or LPUART can switch the HSI16 ON during the Stop mode in order to recognize

their wakeup condition and switch off the HSI16 after receiving the frame if it is not a wakeup frame. In this case, the HSI16 clock is propagated only to the peripheral requesting it.

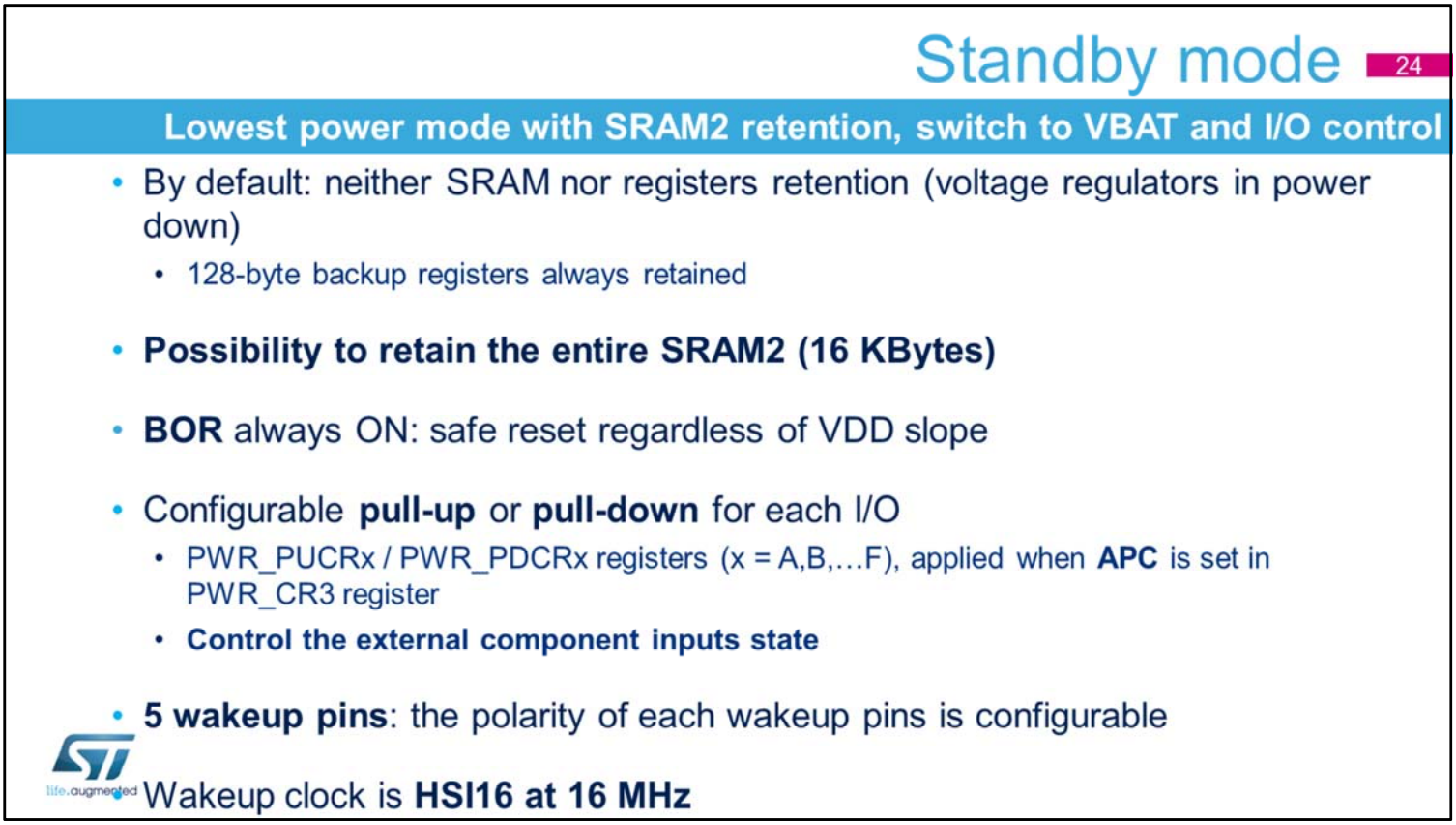


Stop 1 mode is very similar to Stop 0 except that the power figures are much lower as the main regulator is stopped and replaced by the low Power Regulator. Flash memory as well as HSI16 are configurable: they can be stopped or kept enabled.

Stop modes comparison

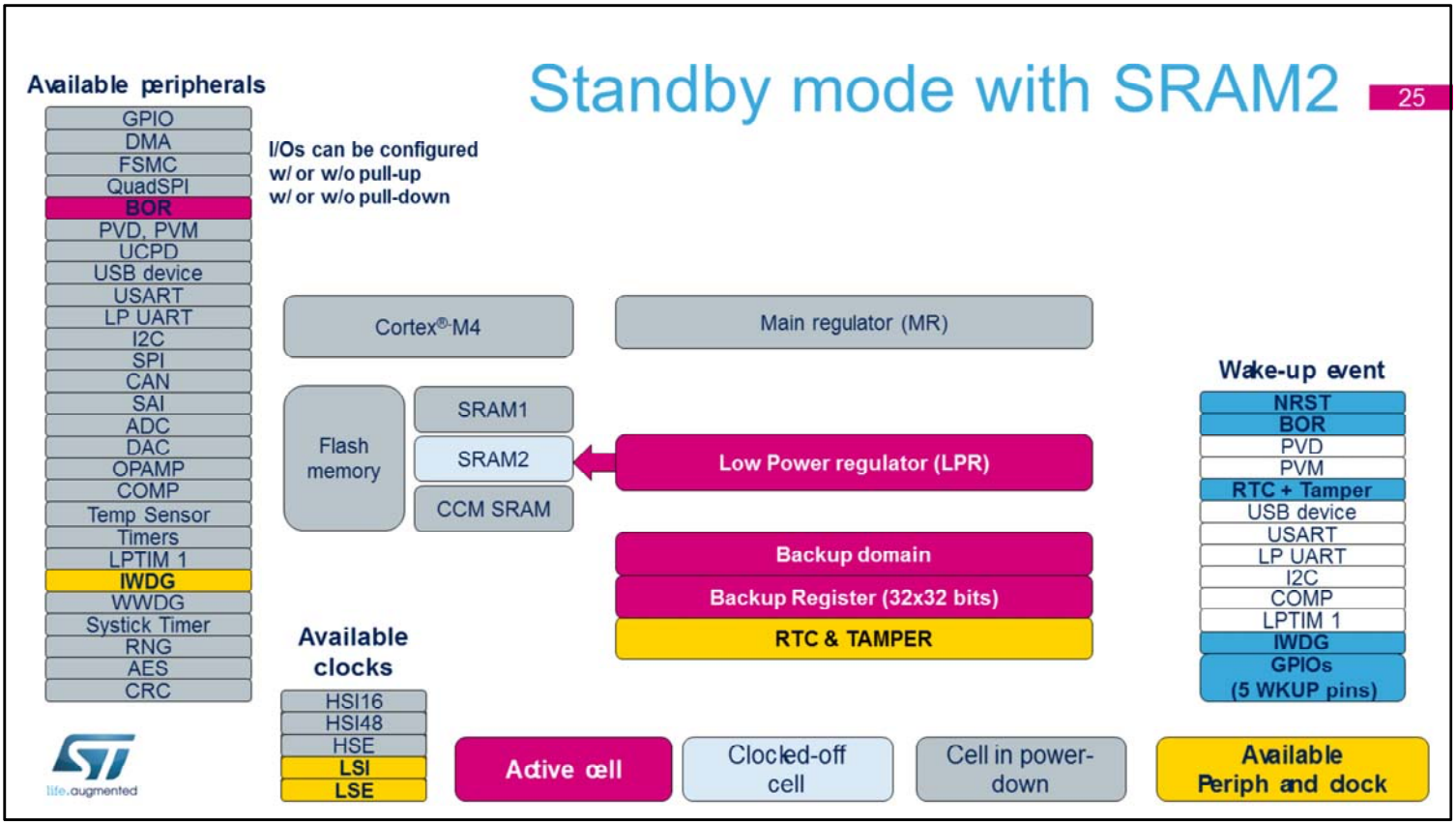
	STOP0	STOP1
Consumption (STM32G474)	25 °C, 1.8 V	
	155 µA	46 µA when RTC is disabled
Wakeup time to 16 MHz	6 µs in Flash memory initially powered down 3 µs in RAM	9.8 µs in Flash memory initially powered down 6.9 µs in RAM
Wakeup clock	HSI16 at 16 MHz	
Regulator	Main regulator	Low power regulator
Peripherals	RTC, I/Os, BOR, PVD, PVM, UCPD, DACs, OPAMPs, COMPs, IWDG 1 LP TIMER 1 LP UART (Start, address match or byte reception) 5 U(S)ART (Start, address match or byte reception) 4 I2C (address match)	

When comparing Stop modes:
Stop 0 mode consumption is higher than Stop 1 mode consumption, but the wakeup time is shorter.
Stop 0 mode keeps the Main regulator enabled, enabling a very short wake-up time of 3 µs when restarting from the RAM to the expense of a higher consumption than Stop 1.
The I2C address recognition is functional in both Stop modes, and can generate a wakeup event in case of an address match.
The UART and LPUART byte reception is functional in both Stop modes and can generate a wakeup event in case of Start detection or Byte reception or Address match event.
When clocked by the internal or external low-speed oscillator, the low-power timer can wake up the MCU with all its events.

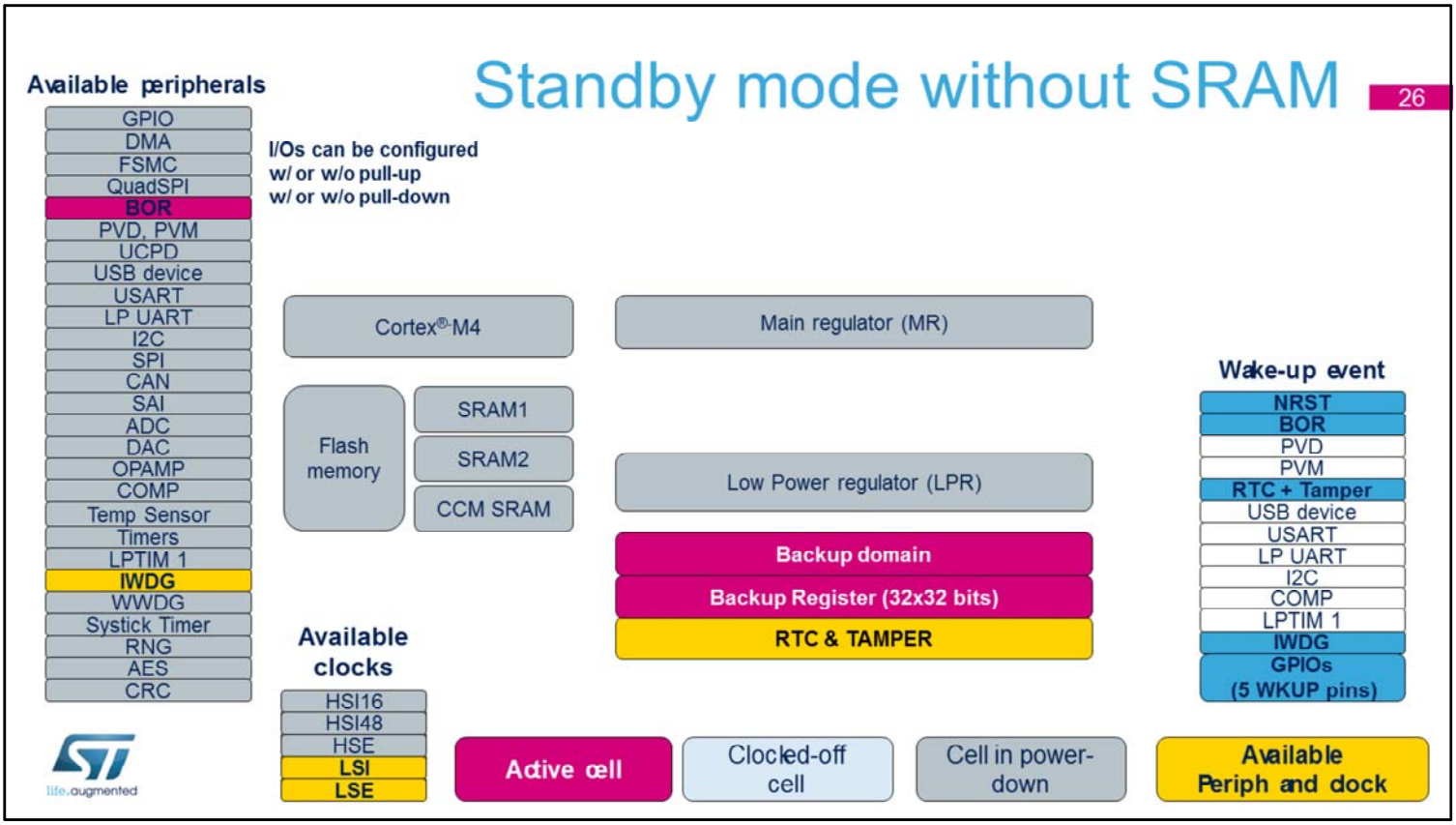


The Standby mode is the lowest power mode in which the 16 KB of SRAM2 can be retained, the automatic switch from VDD to VBAT is supported and the I/Os level can be configured by independent pull-up and pull-down circuitry.
By default, the voltage regulators are in Power down mode and the SRAM contents and peripherals registers are lost. The 128-byte backup registers are always retained.
The brown-out reset is always ON to ensure a safe reset regardless of the VDD slope.
Each I/O can be configured with or without a pull-up or pull-down, which is applied and released thanks to the APC control bit. This controls the input state of external components even during Standby mode.
5 wakeup pins are available to wake up the device from Standby mode. The polarity of each of the 5 wakeup pins

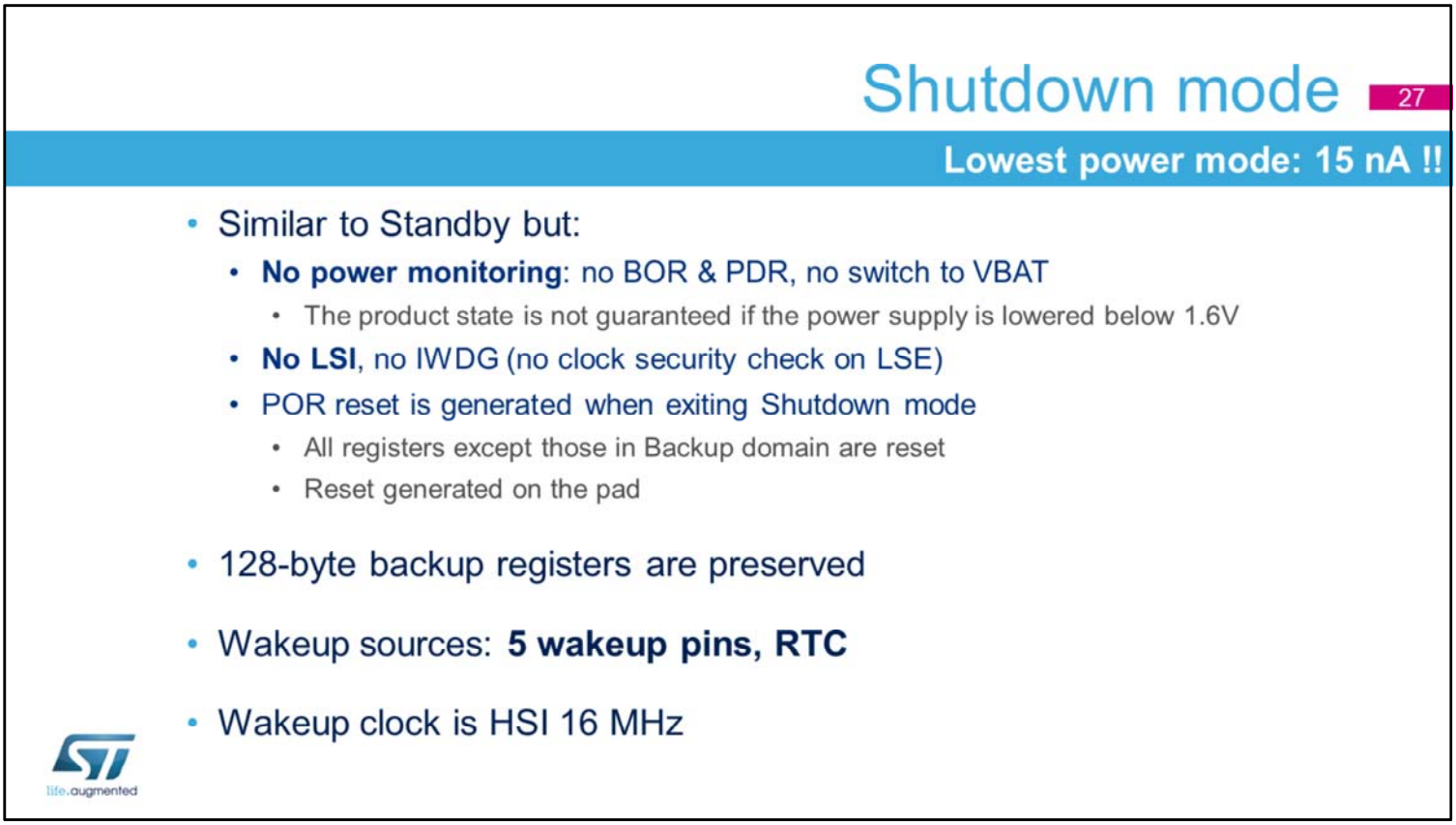
is configurable.
The wakeup clock is HSI with a frequency of 16 MHz.



In Standby mode with SRAM2, the main regulator is powered down and the low power regulator supplies the SRAM to preserve its content.
The RTC, clocked by the internal or external low-speed oscillator, may remain active .
The brown-out reset is always enabled. The independent watchdog can also be enabled in Standby mode.
Reset, brown-out reset, RTC and tamper detection, independent watchdog and any event on the 5 wakeup pins can exit the microcontroller from Standby mode.

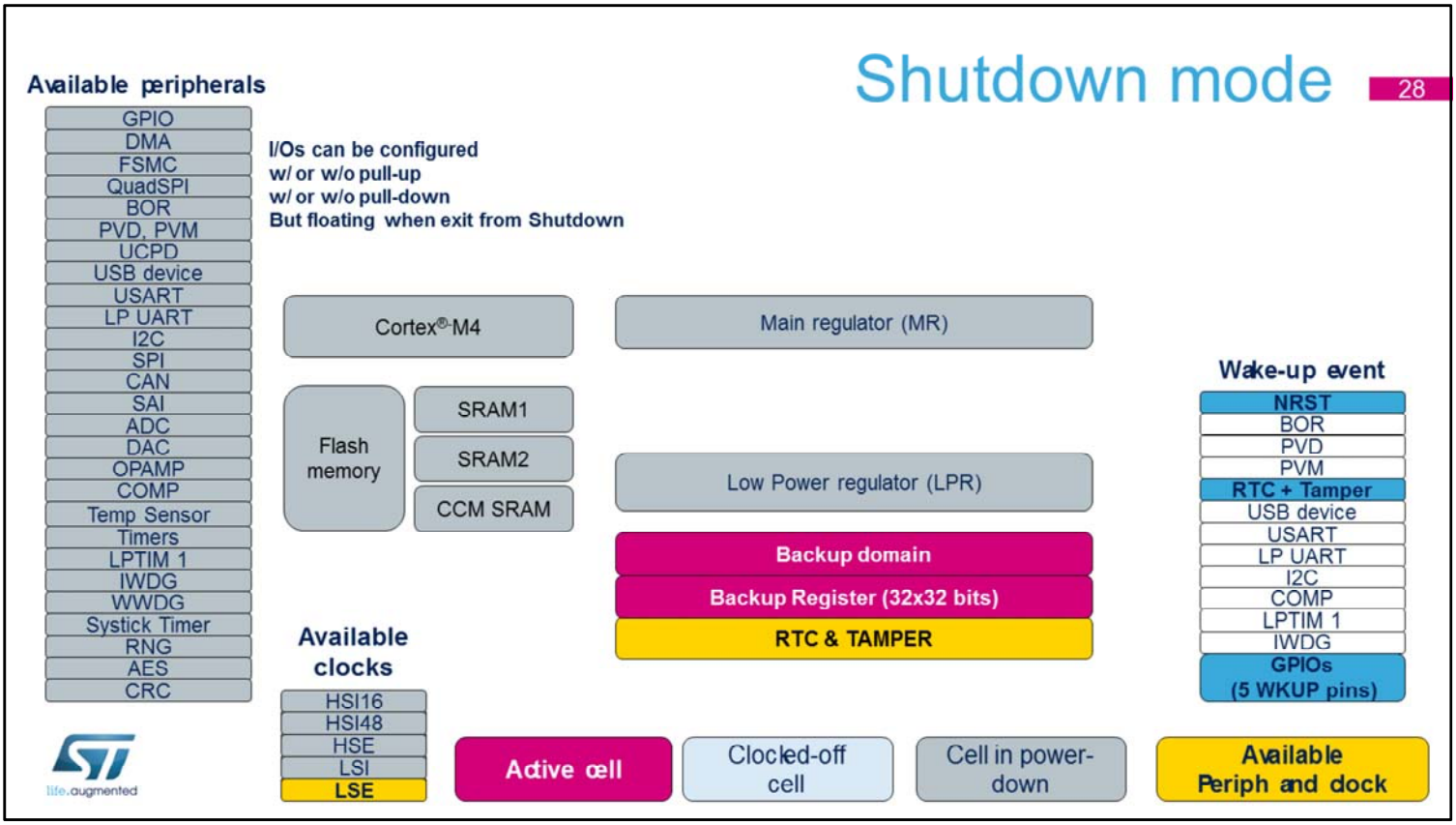


In Standby mode without SRAM retention, both main and low power regulators are powered down.
Wake-up events and available peripherals as well wake-up sources are the same as in Standby mode with SRAM.



The shutdown mode is the lowest power mode of the STM32G4, with only 15 nA at 1.8 V.
This mode is similar to Standby mode but without any power monitoring: the power down reset is disabled and the switch to VBAT is not supported in Shutdown mode. Hence the product state is not guaranteed in case the power supply is lowered below 1.6V.
The LSI is not available, and consequently the independent watchdog is also not available.
A power reset is generated when the device exits Shutdown mode: all registers are reset except those in the backup domain, and a reset signal is generated on the pad.
The 128-byte backup registers are retained in Shutdown mode.
The wakeup sources are the 5 wakeup pins and the RTC events including tampers.

When exiting Shutdown mode, the wakeup clock is HSI at 16 MHz.



In Shutdown mode, the main regulator and the low-power regulator are powered down.
The RTC, clocked by the external low-speed oscillator, can remain active.
The brown-out reset is deactivated. Only the external low-speed clock can be enabled.
The wakeup events are the RTC and tamper events, the reset and the 5 wakeup pins.

Low-power modes summary

Mode	Regulator	CPU	Flash	SRAM	Clocks	Peripherals
Run	MR Range 1	**Yes**	**ON**(1)	**ON**	Any	All
	MR Range 2					All except USB, RNG
LPRun	LPR	**Yes**	**ON**(1)	**ON**	Any except PLL	All except USB, RNG
Sleep	MR Range 1	No	**ON**(1)	**ON**(2)	Any	All Any interrupt or event
	MR Range 2					
LPSleep	LPR	No	**ON**(1)	**ON**(2)	Any except PLL	All Any interrupt or event
Stop 0	MR	No	OFF	**ON**	LSE/LSI	Reset pin, all I/Os BOR, PVD, PVM, RTC, IWDG, COMPx, DACx, OPAMPx, USARTx, LPUART, I2Cx, LPTIM1, USB, UCPD
Stop 1	LPR					
Standby	LPR	DOWN	OFF	**SRAM2 ON**	LSE/LSI	Reset pin, 5 WKUPx pins BOR, RTC, IWDG
	OFF			DOWN		
Shutdown	OFF	DOWN	OFF	DOWN	LSE	Reset pin, 5 WKUPx pins RTC

1. Can be put in power-down and clock can be gated off
2. SRAM1, SRAM2 and CCM SRAM can be gated off independently

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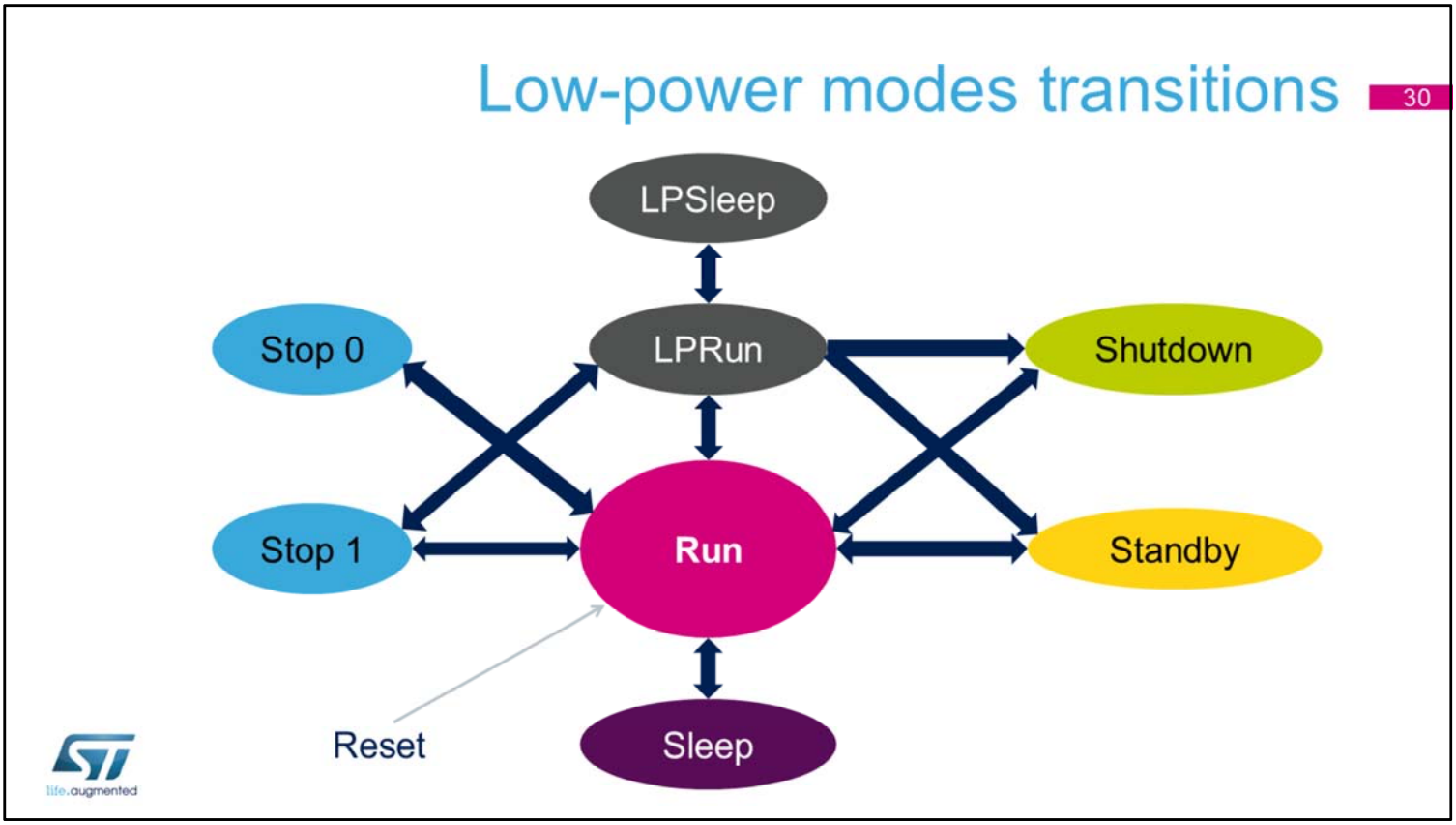
Here you can see the summary of all the STM32G4 power modes.



From Run mode, it is possible to access all low-power modes except Low-power sleep mode.
In order to enter Low-power sleep mode, it is required to move first to Low-power run mode and execute a Wait for Interrupt or Wait for Event instruction while the regulator is the low-power regulator.
On the other hand, when exiting Low-power sleep mode, the STM32G4 is in Low-power run mode.
When the device is in Low-power run mode, it is possible to transition to all low-power modes except Sleep and Stop 0 modes. Stop 0 mode can only be entered from Run mode.
If the device enters Stop 1 mode from Low-power run mode, it will exit in Low-power run mode.
If the device enters Standby or Shutdown, it will exit in Run mode.

VBAT backup domain

RTC still running and backup registers preserved in case of V_{DD} loss

- Backup domain contains:
  - RTC clocked by 32.768 kHz LSE oscillator, including **3 tamper pins**
  - **128 bytes backup registers**
  - Reset through the RCC_BDCR
- Automatic internal switch between V_{BAT} and V_{DD} when V_{DD} is powered down and powered on
- Internal connection to ADC for voltage monitoring ($V_{BAT}/3$)
- VBAT battery charging

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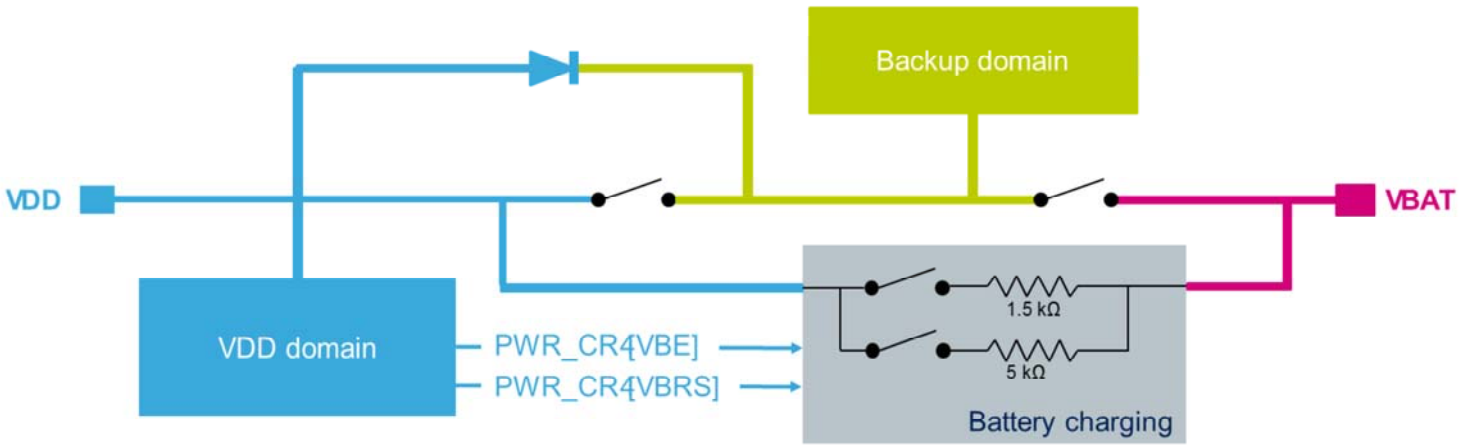
The backup domain keeps the RTC fully functional and preserve the backup registers in case the VDD supply is down, thanks to a backup battery connected to the VBAT pin.
The backup domain contains the RTC clocked by the low-speed external oscillator at 32.768 kHz.
Three tamper pins are functional in VBAT mode, and will erase the 128-byte backup registers also included in the VBAT domain, in case of intrusion detection.
The backup domain also contains the RTC clock control logic.
In case VDD drops below a certain threshold, the backup domain power supply automatically switches to VBAT.
When VDD is back to normal, the backup domain power supply automatically switches back to VDD.
The VBAT voltage is internally connected to an ADC input channel in order to monitor the backup battery

level.
When VDD is present, the battery connected to VBAT can be charged from the VDD supply.

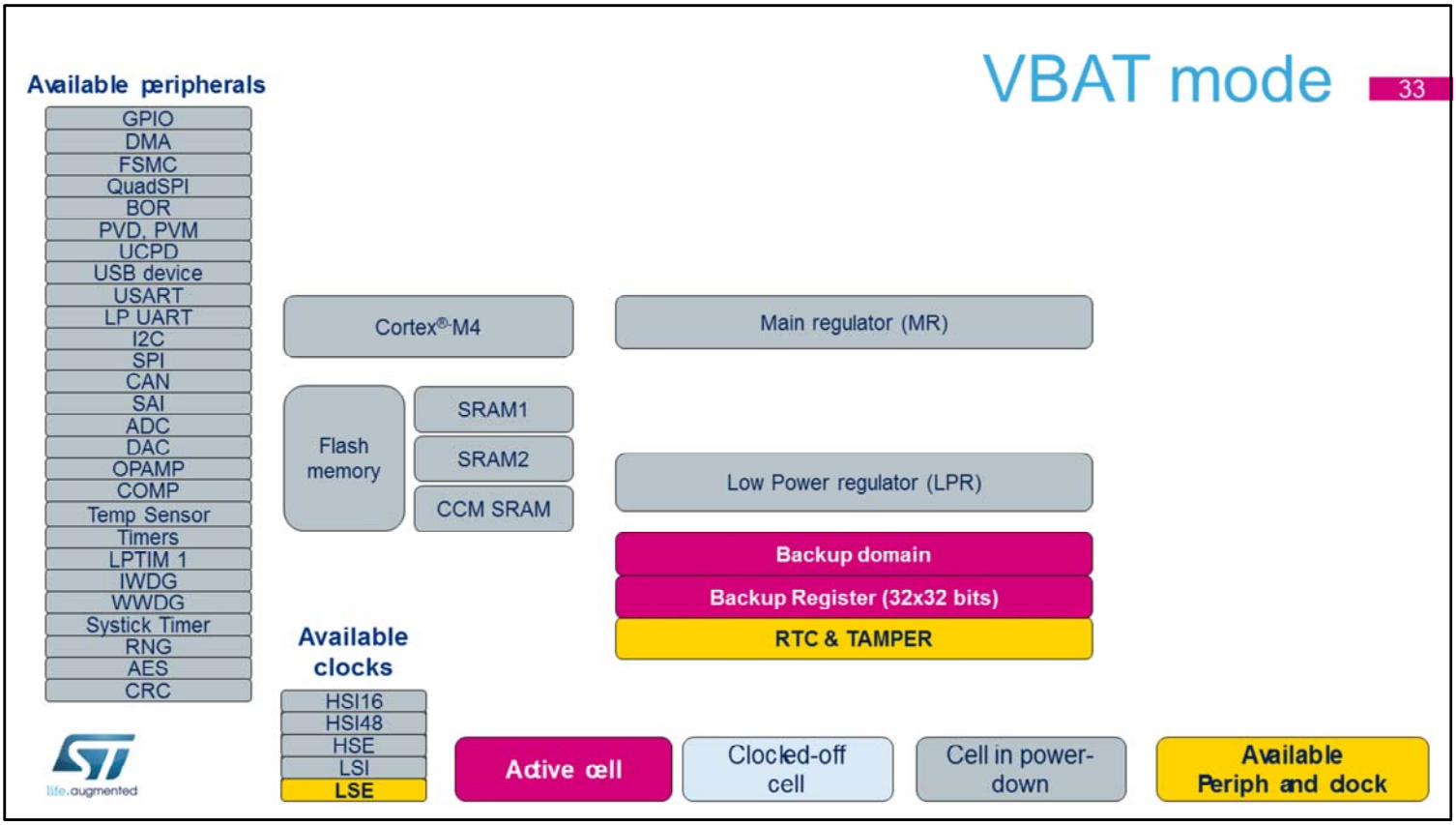
VBAT backup domain

- VBAT battery charging: enables the charging of a super-cap on VBAT through an internal resistor when V_{DD} is present.



The battery charging feature enables the charging of a super-cap connected to VBAT pin through internal resistor when VDD supply is present.
The charging is enabled by software and is done either through a 5kΩ or 1.5kΩ resistor depending on software.
Battery charging is automatically disabled in VBAT mode.
VBE bit field of the PWR_CR4 register enables battery charging.
VBRS bit field of the PWR_CR4 register selects the resistance value.
During the startup phase, if VDD is established in less than tRSTTEMPO and VDD greater than VBAT + 0.6 V, a current may be injected into VBAT through an internal diode connected between VDD and the power switch (VBAT).
If the power supply/battery connected to the VBAT pin cannot support this current injection, it is strongly

recommended to connect an external low-drop diode between this power supply and the VBAT pin



In VBAT mode, the main regulator and the low-power regulator are powered down.
The RTC and Tamper, clocked by the external low-speed oscillator, can remain active.
Only the external low-speed clock can be enabled.
The only powered block is the backup domain that includes RTC and Tampers, and the return to normal execution happens once VDD supply is provided.
The VBAT consumption with RTC is around 150 nA typical at 1.8 V.

Option bytes

- 3 option bits can be configured in Flash option bytes to prohibit a given low-power mode:
  - nRST_SHDWN: When cleared, a Reset is generated when entering Shutdown mode
  - nRST_STDBY: When cleared, a Reset is generated when entering Standby mode
  - nRST_STOP: When cleared, a Reset is generated when entering Stop modes

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Three bits are available in the Flash option bytes to prohibit a given low-power mode.
When cleared, a reset is generated instead of entering the related low-power modes.

Debug information

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- Three bits in DBGMCU_CR register enables debugging in Sleep, Stop, Standby and Shutdown modes:
  - DBG_STANDBY: When set, the digital part is not unpowered in Standby and Shutdown modes, and HCLK and FCLK remain ON, provided by internal RC
    - In addition, the MCU in under system reset during Standby/Shutdown
  - DBG_STOP: When set, HCLK and FCLK remain ON in Stop modes, provided by internal RC
  - DBG_SLEEP: When set, HCLK and FCLK remain ON in Sleep and Low-power sleep modes.
- When those bits are set, the connection with debugger is kept during the low-power mode
  - After wakeup, debug is still possible

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The microcontroller integrates special means allowing the user to debug software in low-power modes.
Three bits are available in the Debug Control Register, in order to allow debugging in Sleep, Stop, Standby and Shutdown modes. When the related bit is set, the regulator is kept ON in Standby and Shutdown modes, and the HCLK and FCLK clocks remain ON to keep the debugger active. This maintains the connection with the debugger during the low-power modes, and continues debugging after wakeup. Remember to clear these bits when the MCU is not under debug, because the consumption is higher in all low-power modes when these bits are set, due to the fact they force the clocks and the regulators to remain enabled.

Related peripherals

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- Refer to the following list of training presentations for more details of their dependencies with the power modes:
  - Reset and clock control (RCC)
  - Real-time clock (RTC)
  - STM32CubeMX, the Power consumption calculator

In addition to this training, you can refer to the following presentations:

- Reset and Clock Control
- Real-Time Clock
- STM32CubeMX, focusing on the description of the power consumption calculator.