# 1. Description

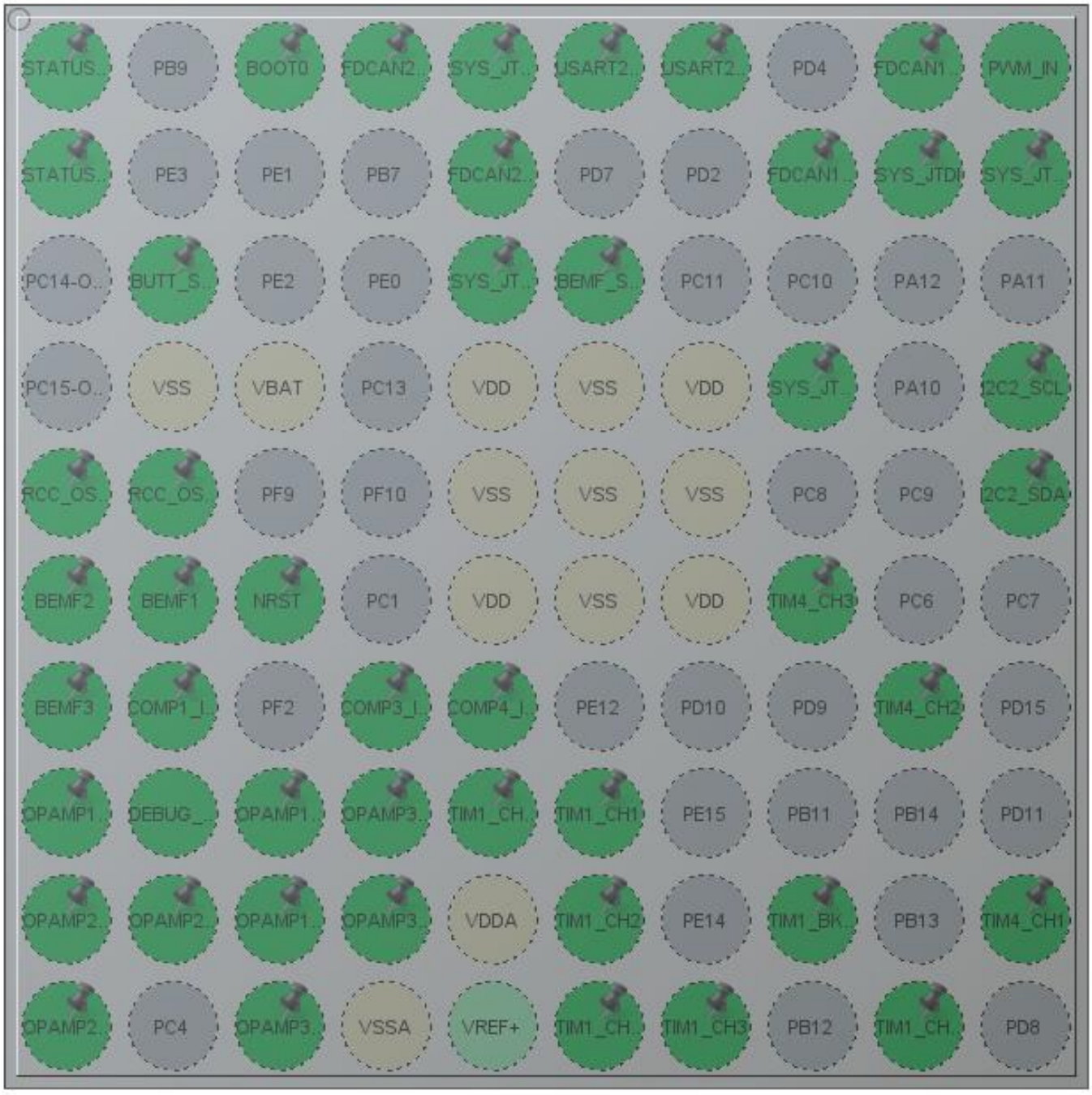
## 1.1. Project

| | |
|---|---|
| Project Name | CUBEMX_ESC |
| Board Name | custom |
| Generated with: | STM32CubeMX 5.4.0 |
| Date | 05/17/2020 |

## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32G4 |
| MCU Line | STM32G4x4 |
| MCU name | STM32G474VEHx |
| MCU Package | TFBGA100 |
| MCU Pin number | 100 |

## 2. Pinout Configuration




TFBGA100 (Top view)

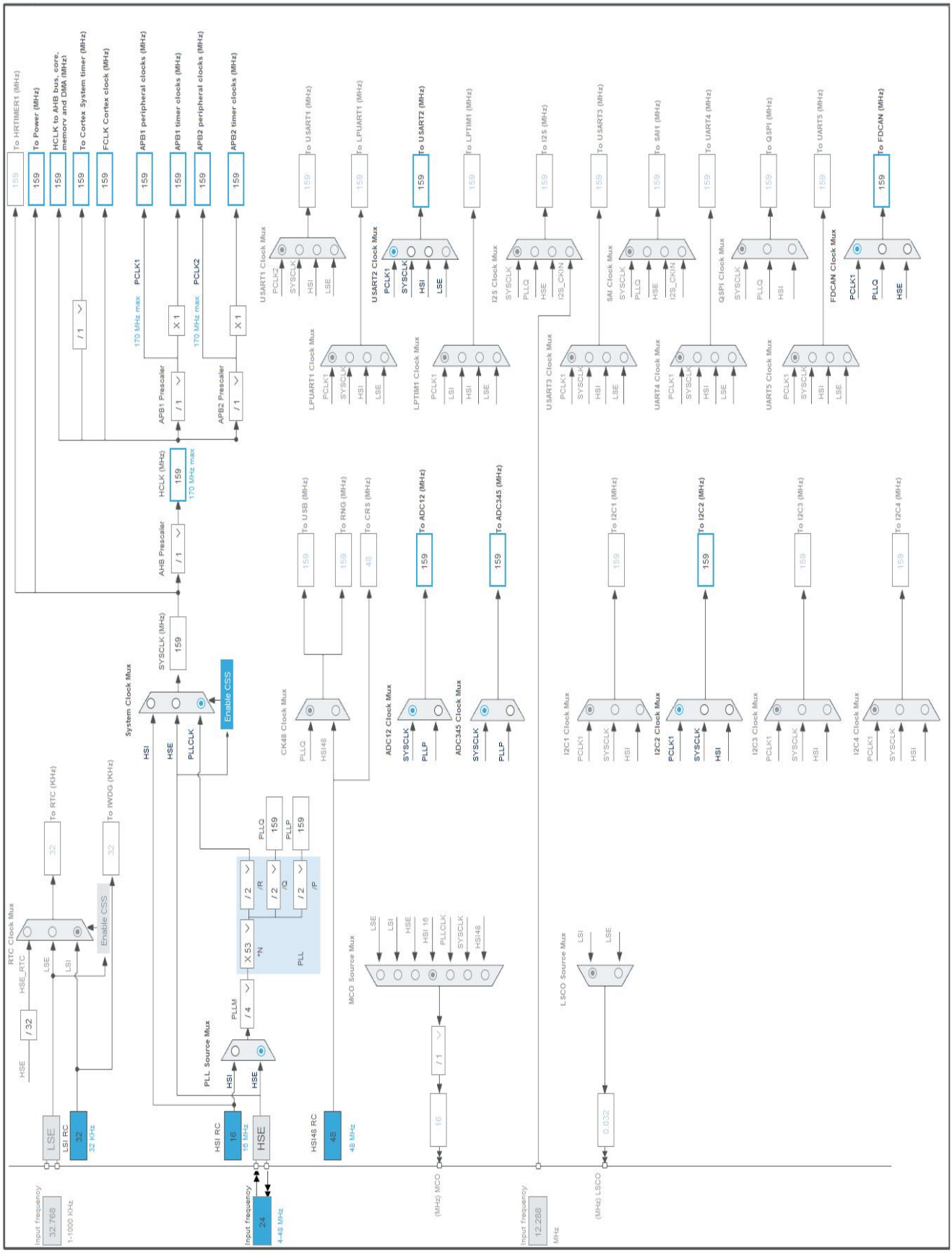
# 3. Pins Configuration

| Pin Number TFBGA100 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| A1 | PE4 | I/O | TIM3_CH3 | STATUS_1 |
| A3 | PB8-BOOT0 * | I/O | GPIO_Input | BOOT0 |
| A4 | PB6 | I/O | FDCAN2_TX | |
| A5 | PB3 | I/O | SYS_JTDO-SWO | |
| A6 | PD6 | I/O | USART2_RX | |
| A7 | PD5 | I/O | USART2_TX | |
| A9 | PD1 | I/O | FDCAN1_TX | |
| A10 | PC12 | I/O | TIM5_CH2 | PWM_IN |
| B1 | PE5 | I/O | TIM3_CH4 | STATUS_2 |
| B5 | PB5 | I/O | FDCAN2_RX | |
| B8 | PD0 | I/O | FDCAN1_RX | |
| B9 | PA15 | I/O | SYS_JTDI | |
| B10 | PA14 | I/O | SYS_JTCK-SWCLK | |
| C2 | PE6 * | I/O | GPIO_Input | BUTT_START |
| C5 | PB4 | I/O | SYS_JTRST | |
| C6 | PD3 | I/O | TIM2_CH1 | BEMF_SLCT |
| D2 | VSS | Power | | |
| D3 | VBAT | Power | | |
| D5 | VDD | Power | | |
| D6 | VSS | Power | | |
| D7 | VDD | Power | | |
| D8 | PA13 | I/O | SYS_JTMS-SWDIO | |
| D10 | PA9 | I/O | I2C2_SCL | |
| E1 | PF0-OSC_IN | I/O | RCC_OSC_IN | |
| E2 | PF1-OSC_OUT | I/O | RCC_OSC_OUT | |
| E5 | VSS | Power | | |
| E6 | VSS | Power | | |
| E7 | VSS | Power | | |
| E10 | PA8 | I/O | I2C2_SDA | |
| F1 | PC2 | I/O | ADC1_IN8 | BEMF2 |
| F2 | PC0 | I/O | ADC2_IN6 | BEMF1 |
| F3 | PG10-NRST * | I/O | GPIO_Input | NRST |
| F5 | VDD | Power | | |
| F6 | VSS | Power | | |
| F7 | VDD | Power | | |
| F8 | PD14 | I/O | TIM4_CH3 | |

| Pin Number TFBGA100 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| G1 | PC3 | I/O | ADC2_IN9 | BEMF3 |
| G2 | PA1 | I/O | COMP1_INP | |
| G4 | PA0 | I/O | COMP3_INP | |
| G5 | PE7 | I/O | COMP4_INP | |
| G9 | PD13 | I/O | TIM4_CH2 | |
| H1 | PA2 | I/O | OPAMP1_VOUT | |
| H2 | PA4 | I/O | DAC1_OUT1 | DEBUG_DAC |
| H3 | PA3 | I/O | OPAMP1_VINP | |
| H4 | PB0 | I/O | OPAMP3_VINP | |
| H5 | PE8 | I/O | TIM1_CH1N | |
| H6 | PE9 | I/O | TIM1_CH1 | |
| J1 | PA5 | I/O | OPAMP2_VINM | |
| J2 | PA6 | I/O | OPAMP2_VOUT | |
| J3 | PC5 | I/O | OPAMP1_VINM | |
| J4 | PB2 | I/O | OPAMP3_VINM | |
| J5 | VDDA | Power | | |
| J6 | PE11 | I/O | TIM1_CH2 | |
| J8 | PB10 | I/O | TIM1_BKIN | |
| J10 | PD12 | I/O | TIM4_CH1 | |
| K1 | PA7 | I/O | OPAMP2_VINP | |
| K3 | PB1 | I/O | OPAMP3_VOUT | |
| K4 | VSSA | Power | | |
| K6 | PE10 | I/O | TIM1_CH2N | |
| K7 | PE13 | I/O | TIM1_CH3 | |
| K9 | PB15 | I/O | TIM1_CH3N | |

* The pin is affected with an I/O function

# 4. Clock Tree Configuration



# 5. Software Project

## 5.1. Project Settings

| Name | Value |
|---|---|
| Project Name | CUBEMX_ESC |
| Project Folder | C:\Users\TOWER_HOME\Documents\GitHub\TRI_ESC\1-HARDWARE\2- |
| Toolchain / IDE | EWARM V8.32 |
| Firmware Package Name and Version | STM32Cube FW_G4 V1.1.0 |

## 5.2. Code Generation Settings

| Name | Value |
|---|---|
| STM32Cube MCU packages and embedded software | Copy all used libraries into the project folder |
| Generate peripheral initialization as a pair of '.c/.h' files | No |
| Backup previously generated files when re-generating | No |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |

# 6. Power Consumption Calculator report

6.1. Microcontroller Selection

| | |
|---|---|
| Series | STM32G4 |
| Line | STM32G4x4 |
| MCU | STM32G474VEHx |
| Datasheet | DS12288_Rev0 |

6.2. Parameter Selection

| | |
|---|---|
| Temperature | 25 |
| Vdd | 3.0 |

# 7. IPs and Middleware Configuration

## 7.1. ADC1

**IN8: IN8 Single-ended**

**mode: Temperature Sensor Channel**

### 7.1.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | Asynchronous clock mode divided by 1 |
| Resolution | ADC 12-bit resolution |
| Data Alignment | Right alignment |
| Gain Compensation | 0 |
| Scan Conversion Mode | Disabled |
| End Of Conversion Selection | End of single conversion |
| Low Power Auto Wait | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | Disabled |
| Overrun behaviour | Overrun data preserved |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Enable Regular Conversions | Enable |
| Enable Regular Oversampling | Disable |
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | **Channel Temperature Sensor *** |
| Sampling Time | 2.5 Cycles |
| Offset Number | No offset |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Enable Injected Conversions | Disable |

**Analog Watchdog 1:**

| | |
|---|---|
| Enable Analog WatchDog1 Mode | false |

**Analog Watchdog 2:**

| | |
|---|---|
| Enable Analog WatchDog2 Mode | false |

**Analog Watchdog 3:**

| | |
|---|---|
| Enable Analog WatchDog3 Mode | false |

## 7.2. ADC2

### IN6: IN6 Single-ended

### IN9: IN9 Single-ended

### 7.2.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | Asynchronous clock mode divided by 1 |
| Resolution | ADC 12-bit resolution |
| Data Alignment | Right alignment |
| Gain Compensation | 0 |
| Scan Conversion Mode | Disabled |
| End Of Conversion Selection | End of single conversion |
| Low Power Auto Wait | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | Disabled |
| Overrun behaviour | Overrun data preserved |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Enable Regular Conversions | Enable |
| Enable Regular Oversampling | Disable |
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | Channel 6 |
| Sampling Time | 2.5 Cycles |
| Offset Number | No offset |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Enable Injected Conversions | Disable |

**Analog Watchdog 1:**

| | |
|---|---|
| Enable Analog WatchDog1 Mode | false |

**Analog Watchdog 2:**

| | |
|---|---|
| Enable Analog WatchDog2 Mode | false |

**Analog Watchdog 3:**

| | |
|---|---|
| Enable Analog WatchDog3 Mode | false |

## 7.3. ADC5

### mode: Temperature Sensor Channel

### 7.3.1. Parameter Settings:

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | Asynchronous clock mode divided by 1 |
| Resolution | ADC 12-bit resolution |
| Data Alignment | Right alignment |
| Gain Compensation | 0 |
| Scan Conversion Mode | Disabled |
| End Of Conversion Selection | End of single conversion |
| Low Power Auto Wait | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | Disabled |
| Overrun behaviour | Overrun data preserved |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Enable Regular Conversions | Enable |
| Enable Regular Oversampling | Disable |
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | Channel Temperature Sensor |
| Sampling Time | 2.5 Cycles |
| Offset Number | No offset |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Enable Injected Conversions | Disable |

**Analog Watchdog 1:**

| | |
|---|---|
| Enable Analog WatchDog1 Mode | false |

**Analog Watchdog 2:**

| | |
|---|---|
| Enable Analog WatchDog2 Mode | false |

**Analog Watchdog 3:**

| | |
|---|---|
| Enable Analog WatchDog3 Mode | false |

## 7.4. COMP1

**mode: Input [+]**

### 7.4.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Trigger Mode | None |
| Hysteresis Level | None |

**Output Configuration:**

| | |
|---|---|
| Blanking Source | None |
| Output Pol | COMP output on GPIO isn't inverted |

## 7.5. COMP3

**mode: Input [+]**

### 7.5.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Trigger Mode | None |
| Hysteresis Level | None |

**Output Configuration:**

| | |
|---|---|
| Blanking Source | None |
| Output Pol | COMP output on GPIO isn't inverted |

## 7.6. COMP4

**mode: Input [+]**

### 7.6.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Trigger Mode | None |
| Hysteresis Level | None |

**Output Configuration:**

| | |
|---|---|
| Blanking Source | None |
| Output Pol | COMP output on GPIO isn't inverted |

## 7.7. CORDIC

**mode: Activated**

## 7.8. DAC1

**OUT1 mode: Connected to external pin and to on chip-peripherals**

### 7.8.1. Parameter Settings:

**DAC Out1 Settings:**

| | |
|---|---|
| Output Buffer | Enable |
| DAC High Frequency | Mode Automatic |
| DMA Double Data | Disable |
| Signed Format | Disable |
| Trigger | None |
| Trigger2 | None |
| User Trimming | Factory trimming |
| Sample And Hold | Sampleandhold Disable |

## 7.9. FDCAN1

**Mode: Classic Master**

### 7.9.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Clock Divider | Divide kernel clock by 1 |
| Frame Format | Classic mode |
| Mode | Normal mode |
| Auto Retransmission | Disable |
| Transmit Pause | Disable |
| Protocol Exception | Disable |
| Nominal Prescaler | 1 |
| Nominal Sync Jump Width | 1 |
| Nominal Time Seg1 | 2 |
| Nominal Time Seg2 | 2 |
| Data Prescaler | 1 |
| Data Sync Jump Width | 1 |
| Data Time Seg1 | 1 |
| Data Time Seg2 | 1 |
| Std Filters Nbr | 0 |
| Ext Filters Nbr | 0 |

| | |
|---|---|
| Tx Fifo Queue Mode | FIFO mode |

## 7.10. FDCAN2

### Mode: Classic Slave

### 7.10.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Frame Format | Classic mode |
| Mode | Normal mode |
| Auto Retransmission | Disable |
| Transmit Pause | Disable |
| Protocol Exception | Disable |
| Nominal Prescaler | 1 |
| Nominal Sync Jump Width | 1 |
| Nominal Time Seg1 | 2 |
| Nominal Time Seg2 | 2 |
| Data Prescaler | 1 |
| Data Sync Jump Width | 1 |
| Data Time Seg1 | 1 |
| Data Time Seg2 | 1 |
| Std Filters Nbr | 0 |
| Ext Filters Nbr | 0 |
| Tx Fifo Queue Mode | FIFO mode |

## 7.11. GPIO

## 7.12. I2C2

### I2C: I2C

### 7.12.1. Parameter Settings:

**Timing configuration:**

| | |
|---|---|
| Custom Timing | Disabled |
| I2C Speed Mode | Standard Mode |
| I2C Speed Frequency (KHz) | 100 |
| Rise Time (ns) | 0 |
| Fall Time (ns) | 0 |
| Coefficient of Digital Filter | 0 |

| | |
|---|---|
| Analog Filter | Enabled |
| Timing | **0x40707DBB *** |

**Slave Features:**

| | |
|---|---|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

## 7.13. OPAMP1

### Mode: PGA Connected-INVERTINGINPUT_IO0_BIAS

### 7.13.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Power Mode | Normal |
| PGA Gain | 2 or -1 |
| User Trimming | Disable |

## 7.14. OPAMP2

### Mode: PGA Connected-INVERTINGINPUT_IO0_BIAS

### 7.14.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Power Mode | Normal |
| PGA Gain | 2 or -1 |
| User Trimming | Disable |

## 7.15. OPAMP3

### Mode: PGA Connected-INVERTINGINPUT_IO0_BIAS

### 7.15.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Power Mode | Normal |
| PGA Gain | 2 or -1 |
| User Trimming | Disable |

## 7.16. RCC

### High Speed Clock (HSE): Crystal/Ceramic Resonator

### 7.16.1. Parameter Settings:

**System Parameters:**

| | |
|---|---|
| VDD voltage (V) | 3.3 |
| Instruction Cache | Enabled |
| Prefetch Buffer | Disabled |
| Data Cache | Enabled |
| Flash Latency(WS) | 7WS (7 CPU cycle) |

**RCC Parameters:**

| | |
|---|---|
| HSI Calibration Value | 64 |
| HSE Startup Timout Value (ms) | 100 |
| LSE Startup Timout Value (ms) | 5000 |

**Power Parameters:**

| | |
|---|---|
| Power Regulator Voltage Scale | Power Regulator Voltage Scale 1 boost |

**Peripherals Clock Configuration:**

| | |
|---|---|
| Generate the peripherals clock configuration | TRUE |

## 7.17. SYS

### Debug: JTAG (5 pins)

### Timebase Source: SysTick

### mode: save power of non-active UCPD - deactive Dead Battery pull-up

## 7.18. TIM1

### Channel1: PWM Generation CH1 CH1N

### Channel2: PWM Generation CH2 CH2N

### Channel3: PWM Generation CH3 CH3N

### mode: Activate-Break-Input

### 7.18.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |

| | |
|---|---|
| Dithering | Disable |
| Counter Period (AutoReload Register - 16 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 16 bits value) | 0 |
| auto-reload preload | Disable |

### Trigger Output (TRGO) Parameters:

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |
| Trigger Event Selection TRGO2 | Reset (UG bit from TIMx_EGR) |

### Break And Dead Time management - BRK Configuration:

| | |
|---|---|
| BRK State | Enable |
| BRK Polarity | High |
| BRK Filter (4 bits value) | 0 |
| BRK Sources Configuration | |
| - Digital Input | Enable |
| Break_IO mode selection | Break IO is an Input |
| Digital Input Polarity | Polarity High |
| - COMP1 | Disable |
| - COMP2 | Disable |
| - COMP3 | Disable |
| - COMP4 | Disable |
| - COMP5 | Disable |
| - COMP6 | Disable |
| - COMP7 | Disable |

### Break And Dead Time management - BRK2 Configuration:

| | |
|---|---|
| BRK2 State | Disable |
| BRK2 Polarity | High |
| BRK2 Filter (4 bits value) | 0 |
| BRK2 Sources Configuration | |
| - Digital Input | Disable |
| - COMP1 | Disable |
| - COMP2 | Disable |
| - COMP3 | Disable |
| - COMP4 | Disable |
| - COMP5 | Disable |
| - COMP6 | Disable |
| - COMP7 | Disable |

### Break And Dead Time management - Output Configuration:

| | |
|---|---|
| Automatic Output State | Disable |
| Off State Selection for Run Mode (OSSR) | Disable |
| Off State Selection for Idle Mode (OSSI) | Disable |
| Lock Configuration | Off |

| | |
|---|---|
| DeadTime Preload | Disable |
| Dead Time | 0 |
| Asymmetrical DeadTime | Disable |
| Falling Dead Time | 0 |

**Clear Input:**

| | |
|---|---|
| Clear Input Source | Disable |

**Pulse On Compare ( Common for Channel 3 and 4 ):**

| | |
|---|---|
| Pulse Width Prescaler | 0 |
| Pulse Width | 0 |

**PWM Generation Channel 1 and 1N:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |
| CHN Polarity | High |
| CH Idle State | Reset |
| CHN Idle State | Reset |

**PWM Generation Channel 2 and 2N:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |
| CHN Polarity | High |
| CH Idle State | Reset |
| CHN Idle State | Reset |

**PWM Generation Channel 3 and 3N:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |
| CHN Polarity | High |
| CH Idle State | Reset |
| CHN Idle State | Reset |

## *7.19. TIM2*

### Channel1: PWM Generation CH1

### 7.19.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Dithering | Disable |
| Counter Period (AutoReload Register - 32 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

**Clear Input:**

| | |
|---|---|
| Clear Input Source | Disable |

**Pulse On Compare ( Common for Channel 3 and 4 ):**

| | |
|---|---|
| Pulse Width Prescaler | 0 |
| Pulse Width | 0 |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

## *7.20. TIM3*

### Channel3: PWM Generation CH3

### Channel4: PWM Generation CH4

### 7.20.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Dithering | Disable |
| Counter Period (AutoReload Register - 16 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

**Clear Input:**

| | |
|---|---|
| Clear Input Source | Disable |

**Pulse On Compare ( Common for Channel 3 and 4 ):**

| | |
|---|---|
| Pulse Width Prescaler | 0 |
| Pulse Width | 0 |

**PWM Generation Channel 3:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 4:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

## *7.21. TIM4*

### Combined Channels: XOR ON / Hall Sensor Mode

### 7.21.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Dithering | Disable |
| Counter Period (AutoReload Register - 16 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Trigger Event Selection TRGO | Output Compare (OC2REF) |

**Pulse On Compare ( Common for Channel 3 and 4 ):**

| | |
|---|---|
| Pulse Width Prescaler | 0 |
| Pulse Width | 0 |

**Hall Sensor:**

| | |
|---|---|
| Prescaler Division Ratio | No division |
| Polarity | Rising Edge |

| | |
|---|---|
| Input Filter | 0 |
| Commutation Delay | 0 |

## 7.22. TIM5

### Channel2: Input Capture direct mode

### 7.22.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Dithering | Disable |
| Counter Period (AutoReload Register - 32 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

**Pulse On Compare ( Common for Channel 3 and 4 ):**

| | |
|---|---|
| Pulse Width Prescaler | 0 |
| Pulse Width | 0 |

**Input Capture Channel 2:**

| | |
|---|---|
| Polarity Selection | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter (4 bits value) | 0 |

## 7.23. USART2

### Mode: Asynchronous

### 7.23.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |

| | |
|---|---|
| Over Sampling | 16 Samples |
| Single Sample | Disable |
| ClockPrescaler | clock /1 |
| Fifo Mode | Disable |
| Txfifo Threshold | 1 eighth full configuration |
| Rxfifo Threshold | 1 eighth full configuration |

### Advanced Features:

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

*** User modified value**

# 8. System Configuration

## 8.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| ADC1 | PC2 | ADC1_IN8 | Analog mode | No pull-up and no pull-down | n/a | BEMF2 |
| ADC2 | PC0 | ADC2_IN6 | Analog mode | No pull-up and no pull-down | n/a | BEMF1 |
| | PC3 | ADC2_IN9 | Analog mode | No pull-up and no pull-down | n/a | BEMF3 |
| COMP1 | PA1 | COMP1_INP | Analog mode | No pull-up and no pull-down | n/a | |
| COMP3 | PA0 | COMP3_INP | Analog mode | No pull-up and no pull-down | n/a | |
| COMP4 | PE7 | COMP4_INP | Analog mode | No pull-up and no pull-down | n/a | |
| DAC1 | PA4 | DAC1_OUT1 | Analog mode | No pull-up and no pull-down | n/a | DEBUG_DAC |
| FDCAN1 | PD1 | FDCAN1_TX | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD0 | FDCAN1_RX | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| FDCAN2 | PB6 | FDCAN2_TX | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PB5 | FDCAN2_RX | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| I2C2 | PA9 | I2C2_SCL | Alternate Function Open Drain | Pull-up | Low | |
| | PA8 | I2C2_SDA | Alternate Function Open Drain | Pull-up | Low | |
| OPAMP1 | PA2 | OPAMP1_VOUT | Analog mode | No pull-up and no pull-down | n/a | |
| | PA3 | OPAMP1_VINP | Analog mode | No pull-up and no pull-down | n/a | |
| | PC5 | OPAMP1_VINM | Analog mode | No pull-up and no pull-down | n/a | |
| OPAMP2 | PA5 | OPAMP2_VINM | Analog mode | No pull-up and no pull-down | n/a | |
| | PA6 | OPAMP2_VOUT | Analog mode | No pull-up and no pull-down | n/a | |
| | PA7 | OPAMP2_VINP | Analog mode | No pull-up and no pull-down | n/a | |
| OPAMP3 | PB0 | OPAMP3_VINP | Analog mode | No pull-up and no pull-down | n/a | |
| | PB2 | OPAMP3_VINM | Analog mode | No pull-up and no pull-down | n/a | |
| | PB1 | OPAMP3_VOUT | Analog mode | No pull-up and no pull-down | n/a | |
| RCC | PF0-OSC_IN | RCC_OSC_IN | n/a | n/a | n/a | |
| | PF1-OSC_OUT | RCC_OSC_OUT | n/a | n/a | n/a | |
| SYS | PB3 | SYS_JTDO-SWO | n/a | n/a | n/a | |
| | PA15 | SYS_JTDI | n/a | n/a | n/a | |
| | PA14 | SYS_JTCK-SWCLK | n/a | n/a | n/a | |
| | PB4 | SYS_JTRST | n/a | n/a | n/a | |
| | PA13 | SYS_JTMS-SWDIO | n/a | n/a | n/a | |
| TIM1 | PE8 | TIM1_CH1N | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE9 | TIM1_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | PE11 | TIM1_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PB10 | TIM1_BKIN | Alternate Function Open Drain | No pull-up and no pull-down | Low | |
| | PE10 | TIM1_CH2N | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE13 | TIM1_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PB15 | TIM1_CH3N | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| TIM2 | PD3 | TIM2_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | BEMF_SLCT |
| TIM3 | PE4 | TIM3_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | STATUS_1 |
| | PE5 | TIM3_CH4 | Alternate Function Push Pull | No pull-up and no pull-down | Low | STATUS_2 |
| TIM4 | PD14 | TIM4_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD13 | TIM4_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD12 | TIM4_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| TIM5 | PC12 | TIM5_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | PWM_IN |
| USART2 | PD6 | USART2_RX | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD5 | USART2_TX | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| GPIO | PB8-BOOT0 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | BOOT0 |
| | PE6 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | BUTT_START |
| | PG10-NRST | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | NRST |

## *8.2. DMA configuration*

nothing configured in DMA service

## 8.3. NVIC configuration

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Prefetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 0 | 0 |
| System tick timer | true | 0 | 0 |
| PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| ADC1 and ADC2 global interrupt | unused | | |
| FDCAN1 interrupt 0 | unused | | |
| FDCAN1 interrupt 1 | unused | | |
| TIM1 break interrupt and TIM15 global interrupt | unused | | |
| TIM1 update interrupt and TIM16 global interrupt | unused | | |
| TIM1 trigger and commutation interrupts and TIM17 global interrupt | unused | | |
| TIM1 capture compare interrupt | unused | | |
| TIM2 global interrupt | unused | | |
| TIM3 global interrupt | unused | | |
| TIM4 global interrupt | unused | | |
| I2C2 event interrupt / I2C2 wake-up interrupt through EXTI line 24 | unused | | |
| I2C2 error interrupt | unused | | |
| USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26 | unused | | |
| TIM5 global interrupt | unused | | |
| TIM6 global interrupt, DAC1 and DAC3 channel underrun error interrupts | unused | | |
| ADC5 global interrupt | unused | | |
| COMP1, COMP2 and COMP3 interrupts through EXTI lines 21, 22 and 29 | unused | | |
| COMP4, COMP5 and COMP6 interrupts through EXTI lines 30, 31 and 32 | unused | | |
| FPU global interrupt | unused | | |
| FDCAN2 interrupt 0 | unused | | |
| | | | |

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| FDCAN2 interrupt 1 | unused | | |
| CORDIC interrupt | unused | | |

*** User modified value**

# 9. Software Pack Report