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Webpage

RESEARCH INTEREST

- Computer Vision, Spiking Neural Networks, Neural Radiance Fields (NeRF), Generative AI, 3D Stable Diffusion, Self-supervised Learning (SSL), Nano-GPT, Pruning, Quantization and Neural Architecture Search, AI-based Software/Hardware design, Neuromorphic Computing, Machine Learning for Virtual and Augmented Reality.

LANGUAGES AND TOOLS

- **Technical Languages:** C, C++, Python-based Object-Oriented Programming, Python (PyTorch, Tensorflow, JAX, Keras, Mxnet, Sklearn, CV2), OpenGL, Verilog, System Verilog, TCL Scripting, AsciiDoc, HTML, and R Language.
- **Tools:** VS Code, PyCharm, Google Colab, Linux, CUDA, Fast-AI, ML-Flow, GPU programming, MATLAB, Git, Cadence (Virtuoso, Innovus), Calibre (DRC, LVS, PEX), Synopsys, Modelsim, Quartus and GDS II Reader/Writer.

EDUCATION

Cornell University (Tech) **NYC, New York** **Aug 2023 – Aug 2025**
- Ph.D. in Electrical Engineering CGPA: 3.70

Arizona State University **Tempe, AZ** **Aug 2020 – Aug 2023**
- Ph.D. in Electrical Engineering CGPA: 3.72

Government College University **Lahore, Pakistan** **Oct 2017 – Sep 2019**
- MS in Electrical Engineering CGPA: 3.75

COMSATS University **Islamabad, Pakistan** **Feb 2011 – Mar 2015**
- BS in Electrical Engineering CGPA: 3.37

Relevant Courses
- Advanced Applied ASIC Design, VLSI Design, Neuromorphic Computing Hardware Design, EffecientML.ai (Han Lab, MIT),ML Hardware and Systems, Computer Vision and Pattern Recog, Machine Learning: Bayesian Perspective.

EMPLOYMENT

Graduate Research Assistant **Cornell Tech (Cornell University), NY** **Aug 2023 – Present**
- **Computer Vision Generative Models (3D Stable Diffusion)**
  - Single-shot 3D scene generation using stable diffusion and NeRF backbone on edge devices.
- **Self-supervised Learning with Vision Transformers (SSL-ViT)**
  - Implemented mainstream vision transformer architectures for better feature learning on unlabeled data.
- **Low-precision and Memory Efficient Neural Radiance Fields (NeRF) with Hardware Accelerator Design**
  - Developed NeRF with low-precision 3D Gaussian-based conical frustums for high-quality 3D scene rendering.
  - Implemented fixed-grid-based quantization scheme for 3D Gaussian, statistically aware quantizationfor MLP activations, and adaptively rounded quantization for weights to make the complete NeRF flow low-precision.
  - Replaced the compute inefficient positional encoding with the fixed-precision (8-bit and 3-bit) look-uptables for software/hardware level efficiency. Achieved high PSNR and SSIM with very low rendering time.
- **Low-compute Spiking Neural Network (LC-SNN) Architecture for DVS-based Computer Vision**
  - Designed a 3-bit precision integer-only quantization scheme for membrane potential for SNN architecture.
  - Proposed fully quantized SNN with spatial-channel pruning for efficient edge computation.
  - Benchmarked LC-QESNN on complex datasets with >3X memory, >5X FLOPs reduction, and <1% accuracy drop.

Design Technology Enablement Intern **Intel Corporations, Hillsboro, OR** **May 2022 – March 2023**
- **Estimation of Local Layout Effect (LLEs) using Machine Readable Specs (MRS)**
  - Using LLE rules from the QA team, designed machine-readable specs to estimate the LLEs' presence in the layouts.
  - Translated MRS into Python utility and validated automated LLE estimation using different layouts.
  - Provided prototype version of python-based utility to QA and TTR team for small and large-scale layout testing.
- **Python-Based Automated Layout Generation for Different Cell Types**
  - Developed Python algorithm to generate automatic and DRC clean layouts.
  - Generated and delivered layouts using a designed algorithm for LLE test cases, standard cells, and memory cells.
- **Pre-production Automated Verification and Completion of Design Run-sets**
  - Implemented an algorithm to identify the key requirements and discrepancies of run-sets for auto-correction.

Research Associate **Seo Lab, Arizona State University, AZ** **Aug 2021 – Aug 2023**
- **DARPA Project: Low Precision Autoencoder Design for Information Processing from Event-based Camera**
  - Designed low-precision sparse autoencoder architecture for Event (Prophesee-Gen1) data compression.

- Designed log of two-based quantization module to covert weights and activations to 4-bit and 2-bit precision.
- Achieved high accuracy of >91% and mean average precision of 0.30 with >10X image data compression ratio.

- **Hardware-efficient Spiking Neural Network (SNN) for DVS-based Computer Vision Applications**
  - Implemented learnable potential threshold-based efficient SNN algorithm (LT-SNN) for edge AI applications.
  - Trained & tested LT-SNN networks for different event-based datasets (N-Caltech, DVS-CIFAR10 & Prophesee Gen1).Implemented low-precision of weights, membrane potential, and activations (2-bit,4-bit, and 8-bit).
  - Improved state-of-the-art accuracy by more than 2.8% and mAP 0.11 with 10.68× less SNN model size.

Research Associate **Optoelectronics Lab, ASU, AZ** **Aug 2020 – July 2021**

- **DOE Funded Project** worth **$2 million: Polarization Camera based Drone Imaging System for Concentrated SolarPower Plants' Defects Detection**
  - Formulated polarization camera-based imaging setup using Nvidia Jetson Tx2 and Sony Imaging sensors.
  - Finished 90% of integration and testing of imaging setup with AltaX Freefly Drone.
- **DARPA Funded Project: Underwater Housing for the Object Localization in the Deep Sea**
  - Developed a polarimetric imaging system with Nvidia Jetson Xavier for robust imaging.

Research Officer **Computer Vision Lab, KICS LHR, PK** **Mar 2020 – Oct 2020**

- **Local Industry Project: Deep Leaning-based Face attendance system, Jetson Tx2 and PYNQ (XILINX)**
  - I worked on the algorithm design and customization of the YoloV3 model for inference on Jetson Tx2.

Lab Engineer **Sharif College of Engineering LHR, PK** **May 2015 – Feb 2020**

- **Lab Instructor in the Department of Electrical and Computer Engineering**

PUBLICATIONS

- Memory-Efficient SNN with Low-Precision Membrane Potential and Weights, ***DAC 2024***, Submitted.
- Efficient-NeRF Accelerator with Low Precision 3D Gaussian Representation and In-memory Computing Design, ***DAC 2024****, Submitted.*
- 3D-ISC: A 65nm 3D Compatible In-Sensor Computing Accelerator with Reconfigurable Tile Architecture for Real-time DVS Data Compression., Gokul Krishnan, Gopikrishnan Raveendran Nair, Jonghyun Oh, Anupreetham Anupreetham, Pragnya Sudershan Nalla, Ahmed Hassan, Injune Yeo et al. ***IEEE ASSCC 2023***, Accepted.
- Field Deployable Mirror Soiling Detection Based on Polarimetric Imaging, Md Zubair Ebne Rafique, Hossain Mansur Resalat Faruque, Ahmad Hassan, Mo Tian, Nabasindhu Das, Yu Yao, ***SolarPaces 2023****.*
- Self-Adaptive Low-precision Spiking Neural Networks for Event-based Object Recognition and Detection, Ahmed Hasssan, Jian Meng, and Jae-sun Seo, ***ICLR 2023****, submitted.*
- Advances in Digital vs. Analog AI Accelerators, Jae-sun Seo, Jyotishman Saikia, Jian Meng, WangxinHe, Han-sok Suh, Anupreetham, Yuan Liao, Ahmed Hasssan, and Injune Yeo, ***IEEE Solid-State Circuits Magazine, 2022.***
- Spatial-temporal Data Compression of Dynamic Vision Sensor Output with High Pixel-level Saliency using Low-precision Sparse Autoencoder, Ahmed Hasssan, Jian Meng, Yu Cao and Jae-sun Seo, ***Asilomar Conference on Signals, Systems, and Computers 2022.***
- LT-SNN: Self-adaptive Spiking Neural Network with Learnable Threshold, Jian Meng, Ahmed Hasssan,and Jae-sun Seo, ***Techcon, Semiconductor Research Corporation 2022****.*
- Smart Tunnel Farming Model: An Inculcation of Cloud Computing with Cortex for Reliable Agricultural Production, Syed Muhammad Alam, Ahmed Hasssan, Abeer Bashir and Mazhar Iqbal, ***International Journal of Sensor Networks and Data Communication 2018****.*
- A comparative review of China, India, and Pakistan renewable energy sectors and sharing opportunities, Saeed Ahmed, Anzar Mahmood, Ahmad Hasan, Guftaar Ahmad Sardar Sidhu, and Muhammad Fasih Uddin Buttl, ***Renewable and Sustainable Energy Reviews 2016****.*

ACADEMIC PROJECTS

- **Low-Precision Convolution Neural Network-Based Processing Engine Design for Classification of MNIST Dataset**
  - Designed shallow (1 Conv and 1 Linear layer) low precision (2-bit weights and 2-bit activations) CNN architecture.
  - Designed and implemented log2-based quantization of weights and activations for better hardware efficiency.
  - Wrote RTL and developed a pipelined design for MAC units to optimize latency and synthesized design.
- **Distance and Sort Engine Design using 7nm ASAP7 PDK**
  - Wrote RTL for Distance and Sort module and verified their functionality using Test Bench.
  - Synthesized the design using Design Compiler, validated synthesized netlist, and achieved frequency 10Ghz.
  - Exported GDS-II file after post-APR and Imported GDS into Virtuoso to run DRC and LVS checks. Confirmed post layoutfunctionality and timing with PEX netlist in Caliber xACT.
- **UNet-based Image Segmentation Architecture Design**
  - Designed shallow UNet Architecture with low-precision weights and activations for image segmentation. Extractedconvex hull to compute the object polygon area. Achieved 0.99 IOU for the custom object dataset.