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**Digital System**

Experiment 5

Combinational Circuit Design: Seven Segments Display using K-Maps

Truth Table

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| a | b | c | d | A | B | C | D | E | F | G |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| x | y | z | AN0 | AN1 | AN2 | AN3 | AN4 | AN5 | AN6 | AN7 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

K-Maps

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| K-map for AN0 | | |  | K-map for AN1 | | |
|  | 0 | 1 |  |  | 0 | 1 |
| 00 | 0 | 1 |  | 00 | 1 | 0 |
| 01 | 1 | 1 |  | 01 | 1 | 1 |
| 11 | 1 | 1 |  | 11 | 1 | 1 |
| 10 | 1 | 1 |  | 10 | 1 | 1 |

|  |  |  |
| --- | --- | --- |
| K-map for AN2 | | |
|  | 0 | 1 |
| 0o | 1 | 1 |
| o1 | 0 | 1 |
| 11 | 1 | 1 |
| 10 | 1 | 1 |

|  |  |  |
| --- | --- | --- |
| K-map for AN3 | | |
|  | 0 | 1 |
| 0o | 1 | 1 |
| o1 | 1 | 0 |
| 11 | 1 | 1 |
| 10 | 1 | 1 |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| K-map for AN4 | | |  | K-map for AN5 | | |
|  | 0 | 1 |  |  | 0 | 1 | |
| 0o | 1 | 1 |  | 0o | 1 | 1 | |
| o1 | 1 | 1 |  | o1 | 1 | 1 | |
| 11 | 1 | 1 |  | 11 | 1 | 1 | |
| 10 | 0 | 1 |  | 10 | 1 | 0 | |

|  |  |  |
| --- | --- | --- |
| K-map for AN6 | | |
|  | 0 | 1 |
| 0o | 1 | 1 |
| o1 | 1 | 1 |
| 11 | 0 | 1 |
| 10 | 1 | 1 |

|  |  |  |
| --- | --- | --- |
|  |  |  |
| K-map for AN7 | | |
|  | 0 | 1 |
| 0o | 1 | 1 |
| o1 | 1 | 1 |
| 11 | 1 | 0 |
| 10 | 1 | 1 |
|  |  |  |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| K-map for Seg-A | | | | | | |
|  | oo | o1 | 11 | 10 |  |  |
| oo | 0 | 1 | 0 | 0 |  |  |
| o1 | 1 | 0 | 0 | 0 |  |  |
| 10 | 0 | 1 | 0 | 0 |  |  |
| 11 | 0 | 0 | 1 | 0 |  |  |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| K-map for Seg-B | | | | | | |
|  | oo | o1 | 11 | 10 |  |  |
| oo | 0 | 0 | 0 | 0 |  |  |
| o1 | 0 | 1 | 0 | 1 |  |  |
| 10 | 1 | 0 | 1 | 1 |  |  |
| 11 | 0 | 0 | 1 | 0 |  |  |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| K-map for Seg-C | | | | | | |
|  | oo | o1 | 11 | 10 |  |  |
| oo | 0 | 0 | 0 | 1 |  |  |
| o1 | 0 | 0 | 0 | 0 |  |  |
| 10 | 1 | 0 | 1 | 1 |  |  |
| 11 | 0 | 0 | 0 | 0 |  |  |
|  |  |  |  |  |  |  |

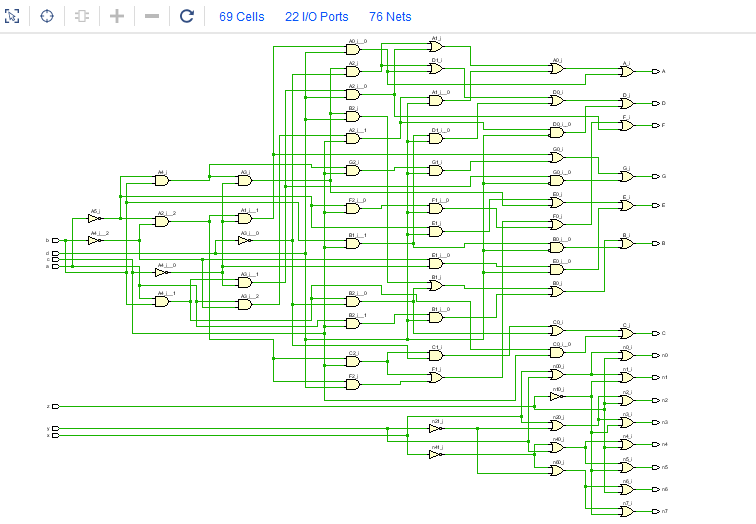
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| K-map for Seg-D | | | | | | |
|  | oo | o1 | 11 | 10 |  |  |
| oo | 0 | 1 | 0 | 0 |  |  |
| o1 | 1 | 0 | 1 | 0 |  |  |
| 10 | 0 | 0 | 1 | 0 |  |  |
| 11 | 0 | 0 | 0 | 1 |  |  |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| K-map for Seg-E | | | | | | |
|  | oo | o1 | 11 | 10 |  |  |
| oo | 0 | 1 | 1 | 0 |  |  |
| o1 | 1 | 1 | 1 | 0 |  |  |
| 10 | 0 | 0 | 0 | 0 |  |  |
| 11 | 0 | 1 | 0 | 0 |  |  |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| K-map for Seg-F | | | | | | |
|  | oo | o1 | 11 | 10 |  |  |
| oo | 0 | 1 | 1 | 1 |  |  |
| o1 | 0 | 0 | 1 | 0 |  |  |
| 10 | 0 | 1 | 0 | 0 |  |  |
| 11 | 0 | 0 | 0 | 0 |  |  |

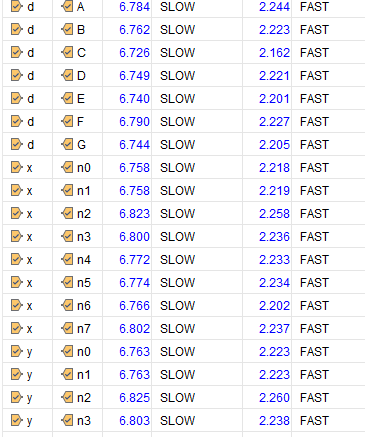
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| K-map for Seg-G | | | | | | |
|  | oo | o1 | 11 | 10 |  |  |
| oo | 1 | 1 | 0 | 0 |  |  |
| o1 | 0 | 0 | 1 | 0 |  |  |
| 10 | 1 | 0 | 0 | 0 |  |  |
| 11 | 0 | 0 | 0 | 0 |  |  |

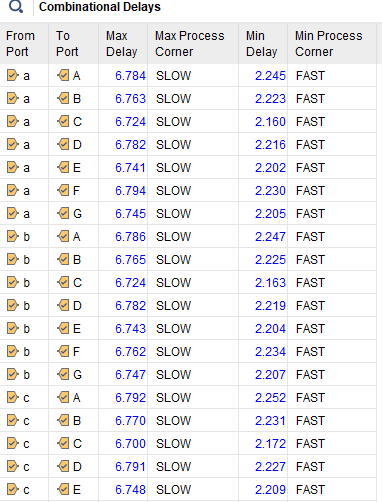
Circuit Diagram



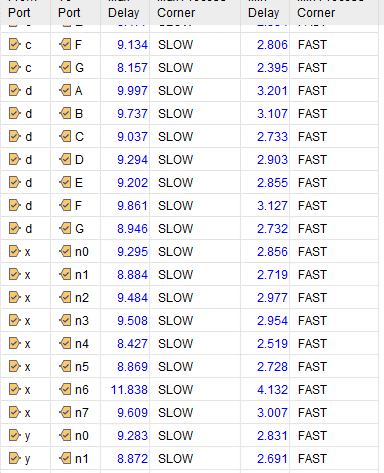
Combinational Delay

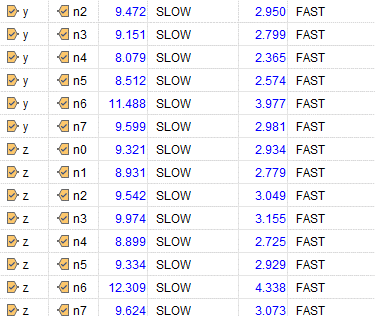


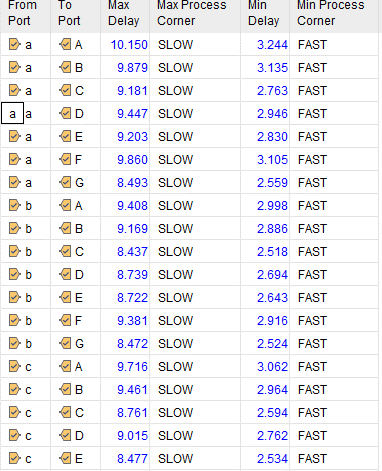




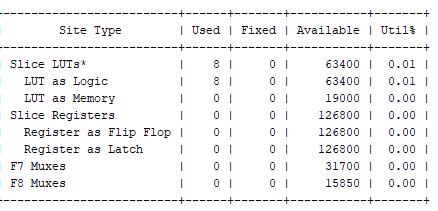
R







Resource Utilization



System Verilog code

module lab5 (input logic a,b,c,d,x,y,z,

output logic n0,n1,n2,n3,n4,n5,n6,n7,A,B,C,D,E,F,G

);

assign A = (~a && b && ~c && ~d) || (a && b && ~c && d) || (a && ~b && c && d) || (~a && ~b && ~c && d) ;

assign B = (~a && b && ~c && d) || (a && b && ~d) || (a && c && d) || (b && c && ~d) ;

assign C = (~a && ~b && c && ~d) || (a && b && ~d) || (a && b && c) ;

assign D = (~a && b && ~c && ~d) || (~a && ~b && ~c && d) || (b && c && d) || (a && ~b && c && ~d) ;

assign E = (~a && d) || (~a && b && ~c ) || (~b && ~c && d) ;

assign F = (~a && ~b && c) || (~a && ~b && d ) || (~a && c && d) || (a && b && ~c && d) ;

assign G = (~a && ~b && ~c ) || (~a && b && c && d) || (a && b && ~c && ~d) ;

assign n0 = x||y||z;

assign n1 = x||y||(~z);

assign n2 = x||(~y)||z;

assign n3 = x||(~y)||(~z);

assign n4 = ~x||(y)||(z);

assign n5 = ~x||(y)||(~z);

assign n6 =~x||(~y)||(z);

assign n7 = ~x||(~y)||(~z);

endmodule

module lab5\_tb;

logic a, b, c, d, x, y, z;

logic n0, n1, n2, n3, n4, n5, n6, n7, A, B, C, D, E, F, G;

lab5 uut (

initial begin

for (int i = 0; i < 8; i++) begin

x = i[2];

y = i[1];

z = i[0];

// Loop through all possible combinations for d, x, y, z

for (int j = 0; j < 16; j++) begin

a = j[3];

b = j[2];

c = j[1];

d = j[0];

#10;

end

end

$finish;

end

endmodule

.a(a),

.b(b),

.c(c),

.d(d),

.x(x),

.y(y),

.z(z),

.n0(n0),

.n1(n1),

.n2(n2),

.n3(n3),

.n4(n4),

.n5(n5),

.n6(n6),

.n7(n7),

.A(A),

.B(B),

.C(C),

.D(D),

.E(E),

.F(F),

.G(G)

);