SPI Slave with Single Port RAM

by Ahmed Khalaf Mohamed Ali

Under the guidance of **Eng. Kareem Waseem**

1 Projects specifications:

1.1 Input-Output Ports

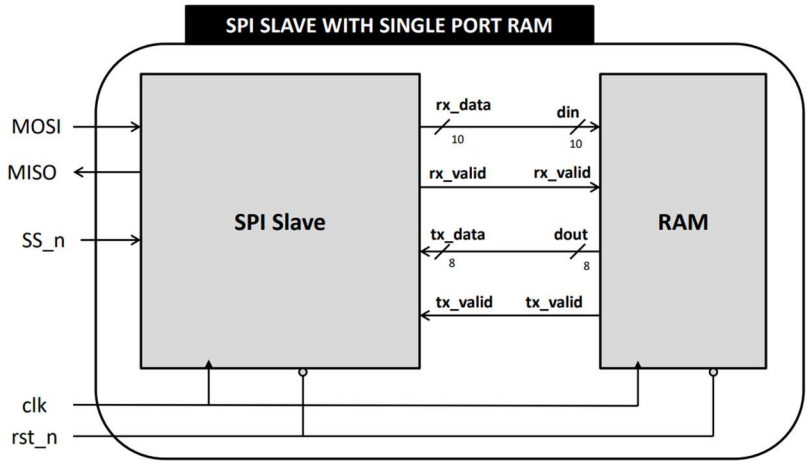


Figure 1:SPI SLAVE INTERFACE WITH SINGLE RAM

1.2 SPI SLAVE INTERFACE

1.2.1 Ports

Name	Type	Size	Description
clk	Input	1 bit	Clock signal
rst_n	Input	1 bit	Active low reset signal
SS_n	Input	1 bit	Slave Select signal
MOSI	Input	1 bit	Master-Out-Slave-In data signal
tx_data	Input	10 bit	Transfer data output signal, Takes MOSI for 10 clock cycles and stores it in tx_data to send it to the RAM
tx_valid	Input	1 bit	Indicates when tx_data is valid
MISO	Output	1 bit	Master-In-Slave-Out data signal
rx_data	Output	10 bit	Received data from the memory
rx_valid	Output	1 bit	Indicates when rx_data is valid

1.3 Single Port sync RAM Module

1.3.1 Parameters

MEM_DEPTH, Default: 256
ADDR_SIZE, Default: 8

1.3.2 Ports

Name	Type	Size	Description
clk	Input	1 bit	**Clock Signal**
a_rst_n		1 bit	**Active low synchronous reset signal**
din		10 bits	**Data Input**
rx_valid		1 bit	**HIGH only accept din[7:0] to save the write/read address internally or write a memory word depending on the most significant 2 bits din[9:8]**
dout	Output	8 bits	**Data Output**
tx_valid		**1 bit**	**Whenever the command is memory read the tx_valid should be HIGH**

1.4 SPI Slave FSM Transitions

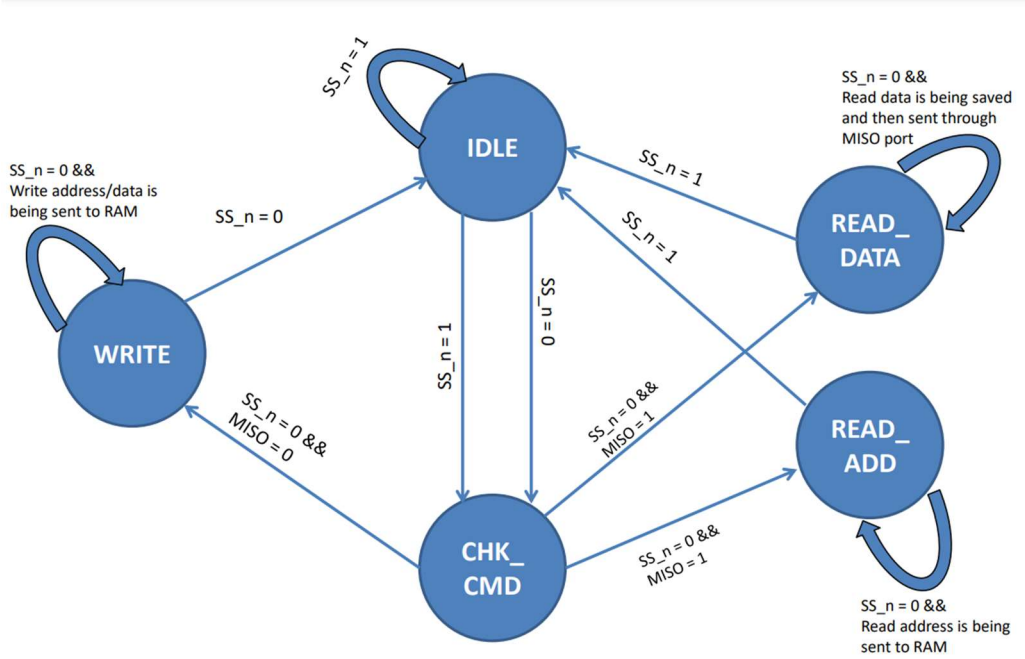


Figure 2: SPI Slave State Transitions

2 READ-WRITE

Din[9:8] selects the mode for Read/ Write on the single port synchronous RAM

din[9:8]	Command	Description
00	Write	**Hold din[7:0] internally as write address**
01		**Write din[7:0] in the memory with write address held previously**
10	Read	**Hold din[7:0] internally as read address**
11		**Read the memory with read address held previously, tx_valid should be HIGH, dout holds the word read from the memory, ignore din[7:0].**

3 WAVEFORMS

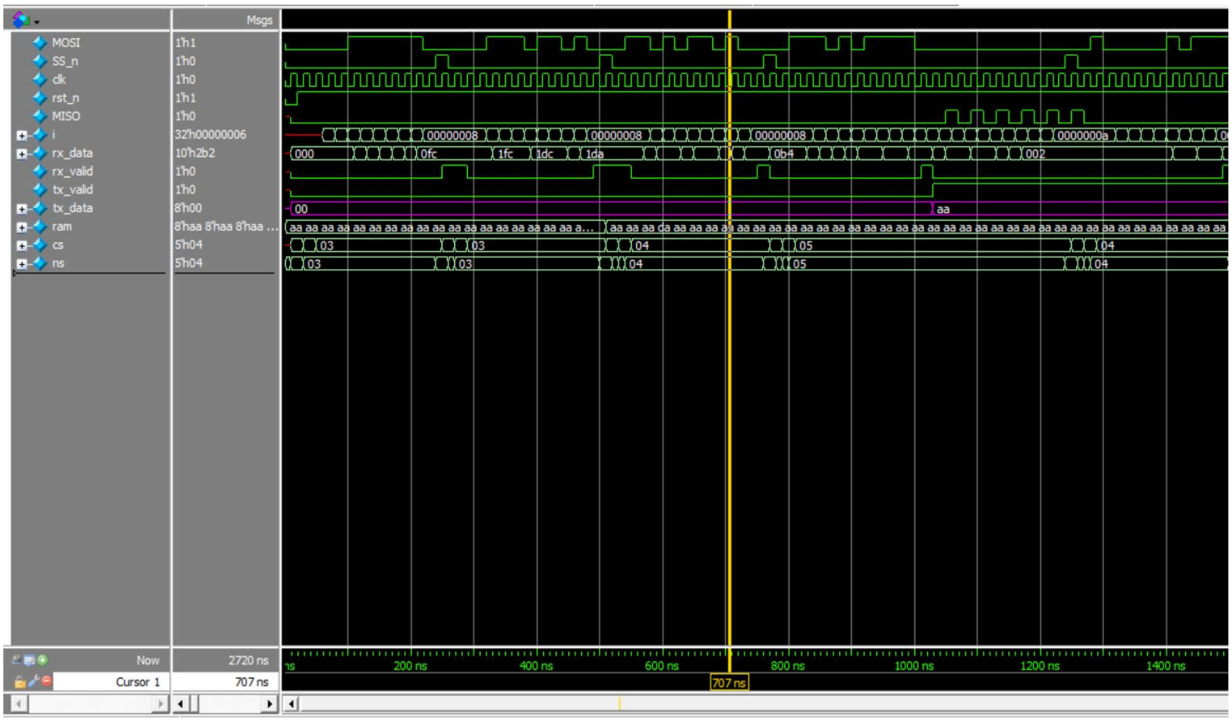


Figure 3:initialization Ram

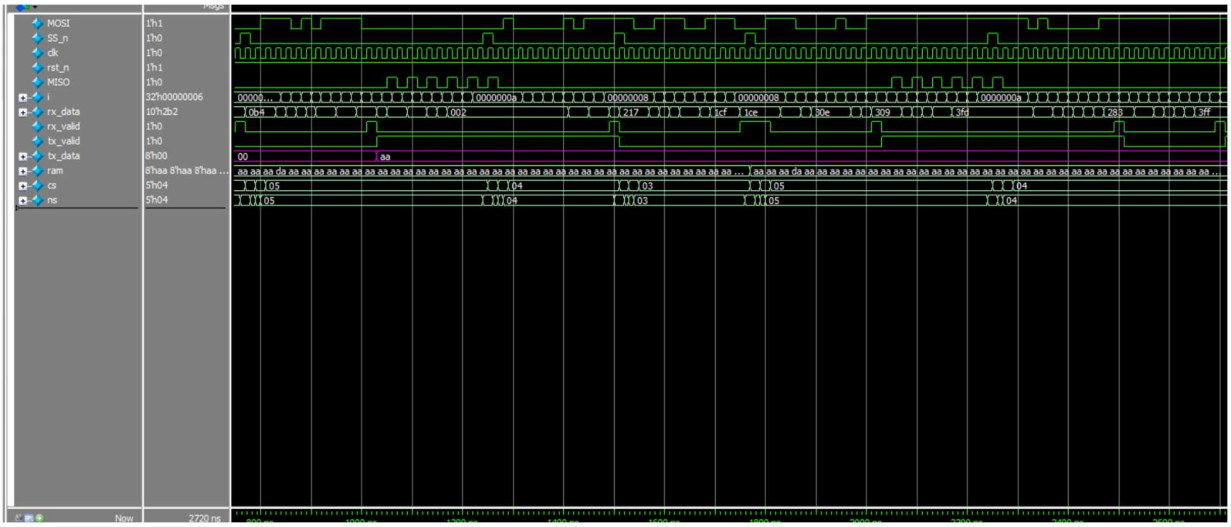


Figure 4: Write AND READ DATA AND ADDRESS

4 Synthesis snippets-One hot encoding:

4.1 Schematic after the elaboration

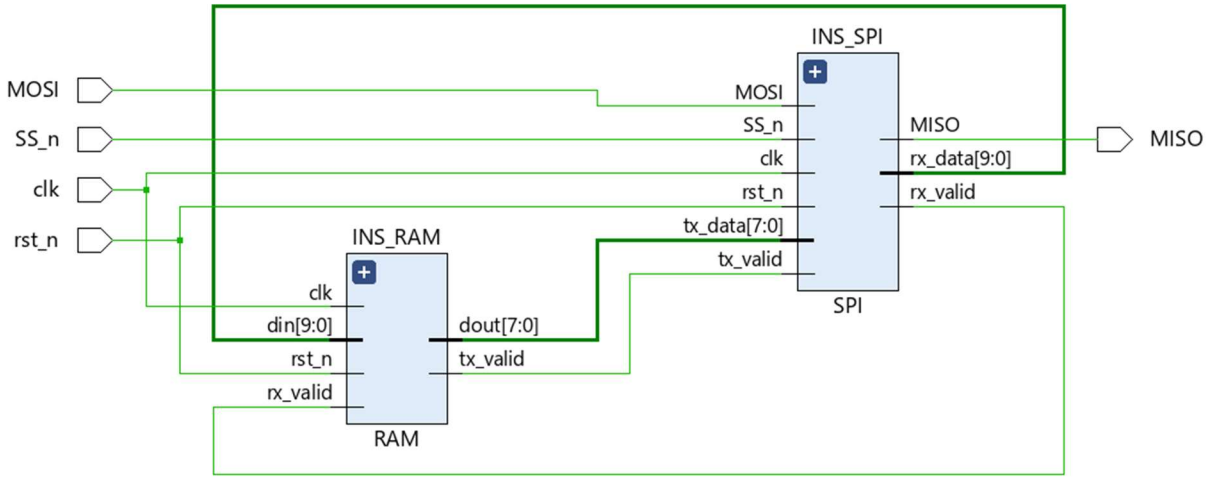


Figure 5:Schematic after the elaboration

4.2 Schematic after the Synthesis

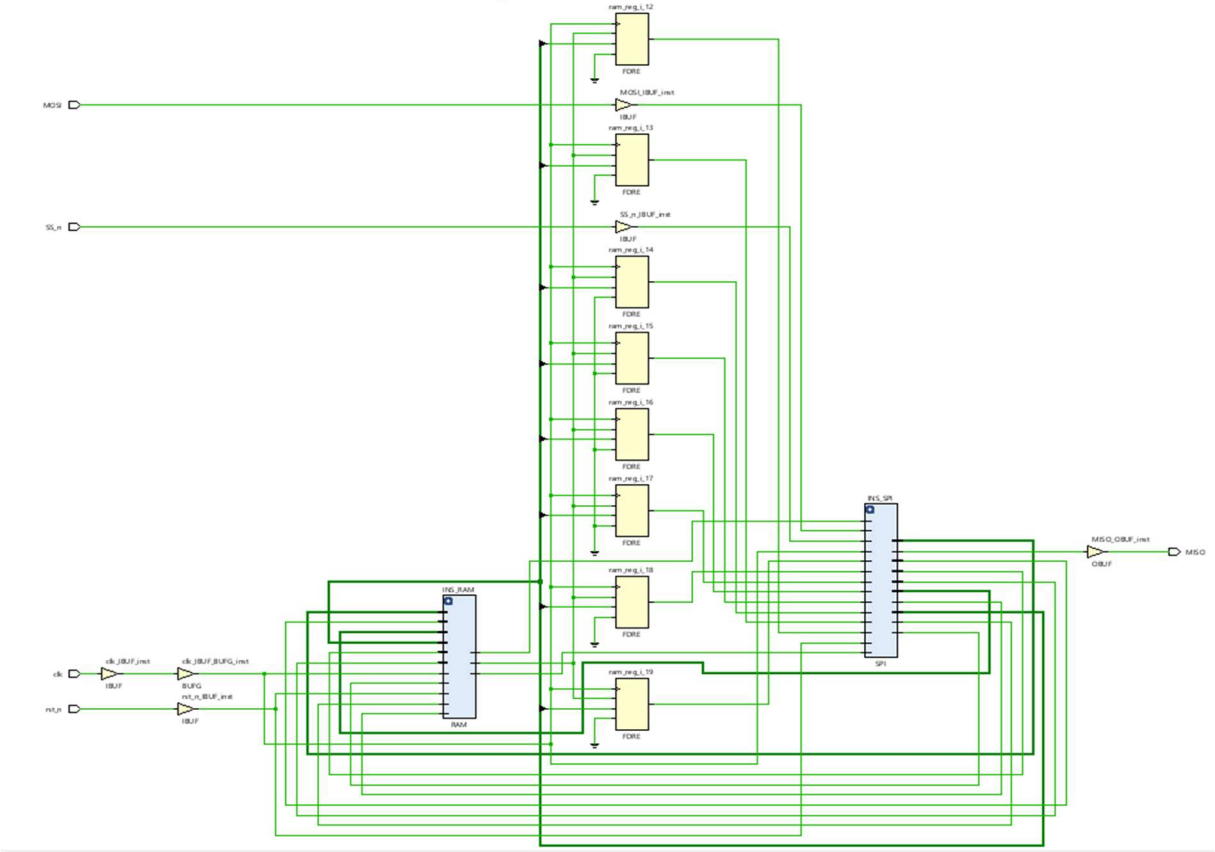
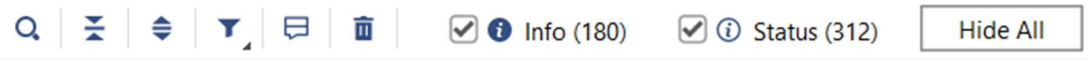


Figure 6:Schematic after the Synthesis



4.3 Synthesis report showing the encoding used

```
INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI'
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |               Previous Encoding
---------------------------------------------------------------------------------------------------
*
                    IDLE |                            00001 |                            00001
                 CHK_CMD |                            00010 |                            00010
                   WRITE |                            00100 |                            00100
               READ_DATA |                            10000 |                            10000
                READ_ADD |                            01000 |                            01000
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3898] No Re-encoding of one hot register 'cs_reg' in module 'SPI'
```

Figure 7:Synthesis report showing the encoding used

4.4 Design Timing summary

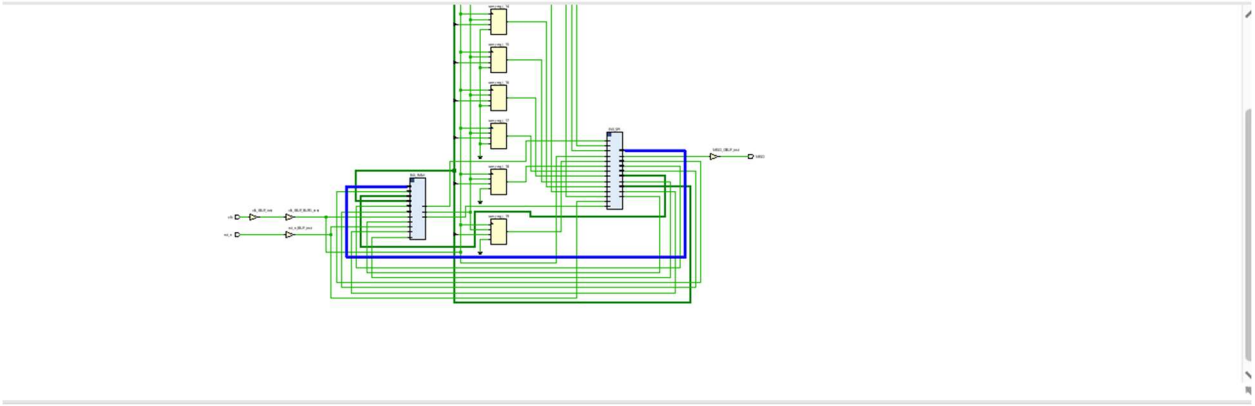
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.714 ns	Worst Hold Slack (WHS):	0.142 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	87	Total Number of Endpoints:	87	Total Number of Endpoints:	42

All user specified timing constraints are met.

Figure 8:Design Timing summary

4.5 Critical path



Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	6.714	1	4	INS_SPI/rx_data_reg[6]/C	INS_RAM/ra...RADDR[10]	2.540	0.751	1.789	10.000	sys_clk_pin
Path 2	6.714	1	4	INS_SPI/rx_data_reg[7]/C	INS_RAM/ra...RADDR[11]	2.540	0.751	1.789	10.000	sys_clk_pin
Path 3	6.714	1	4	INS_SPI/rx_data_reg[0]/C	INS_RAM/ra...BWRADDR[4]	2.540	0.751	1.789	10.000	sys_clk_pin
Path 4	6.714	1	4	INS_SPI/rx_data_reg[1]/C	INS_RAM/ra...BWRADDR[5]	2.540	0.751	1.789	10.000	sys_clk_pin
Path 5	6.714	1	4	INS_SPI/rx_data_reg[2]/C	INS_RAM/ra...BWRADDR[6]	2.540	0.751	1.789	10.000	sys_clk_pin

Figure 9:Critical path

5 Implementation-One hot encoding:

5.1 Utilization report

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_SLAVE_WITH_SINGLE_PORT_RAM	36	39	21	36	0.5	5	1
INS_RAM (RAM)	5	9	7	5	0.5	0	0
INS_SPI (SPI)	32	22	19	32	0	0	0

Figure 10:Utilization report

5.2 Timing report

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.912 ns	Worst Hold Slack (WHS):	0.044 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	88	Total Number of Endpoints:	88	Total Number of Endpoints:	42

All user specified timing constraints are met.

Figure 11:Timing report

5.3 FPGA device

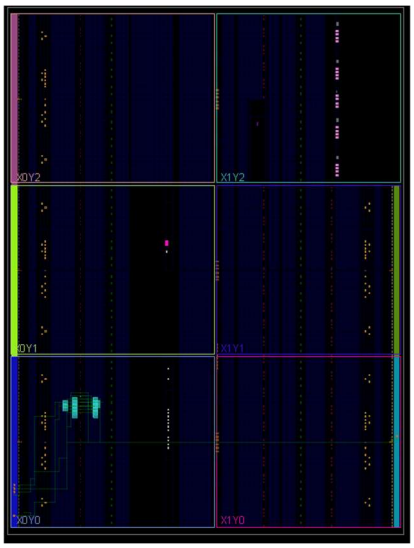


Figure 12:FPGA device

5.4 Bitstream generate

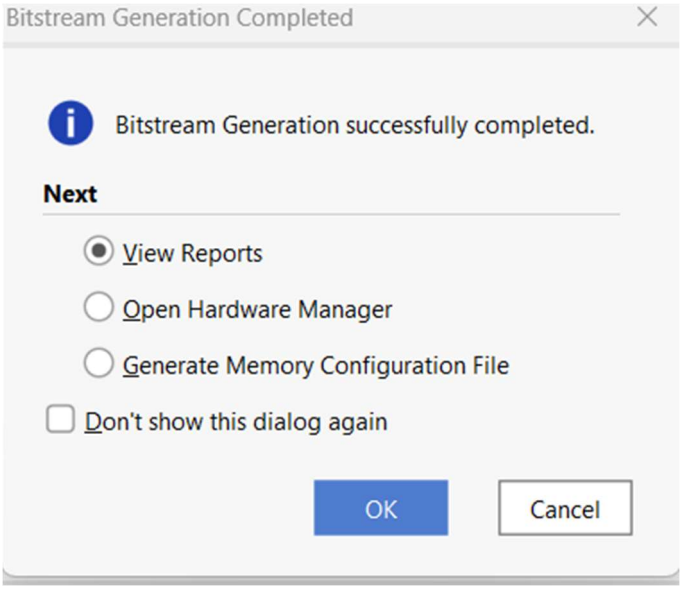


Figure 13:Bitstream generate

6 Synthesis snippets-gray encoding:

6.1 Schematic after the elaboration

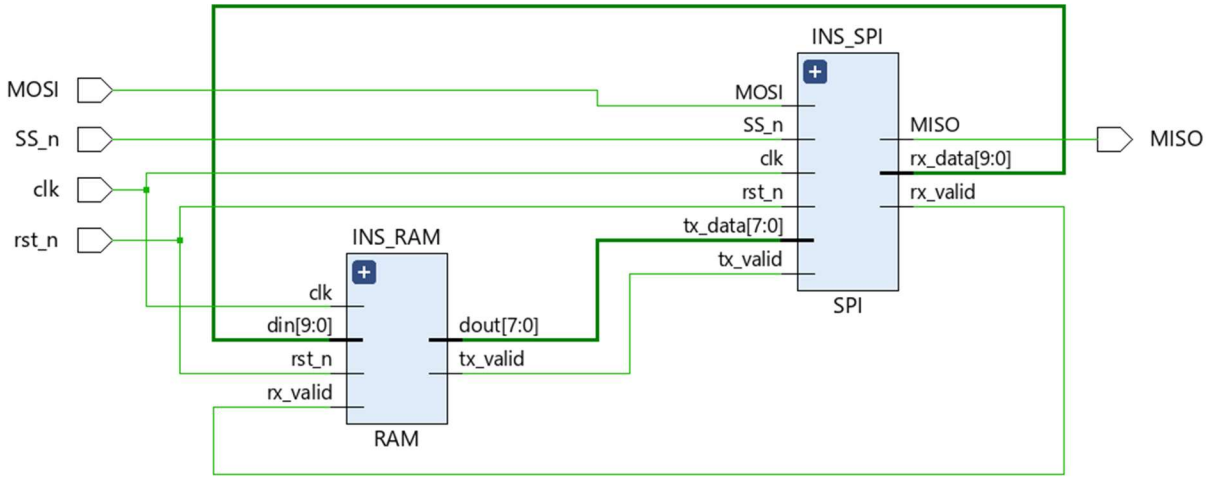


Figure 14:schematic after the elaboration

6.2 Schematic after the Synthesis

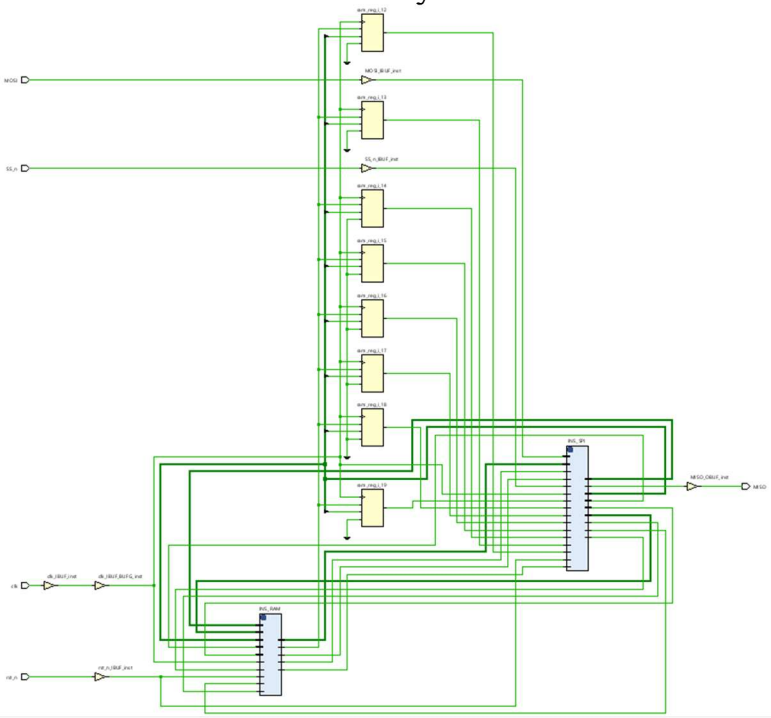
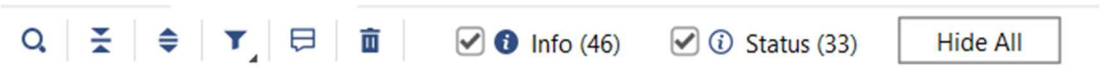


Figure 15:Schematic after the Synthesis



6.3 Synthesis report showing the encoding used

```
INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI'
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |               Previous Encoding
---------------------------------------------------------------------------------------------------
                    IDLE |                              000 |                            00001
                 CHK_CMD |                              001 |                            00010
                   WRITE |                              011 |                            00100
               READ_DATA |                              010 |                            10000
                READ_ADD |                              111 |                            01000
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI'
```

Figure 16:Synthesis report showing the encoding used

6.4 Design Timing summary

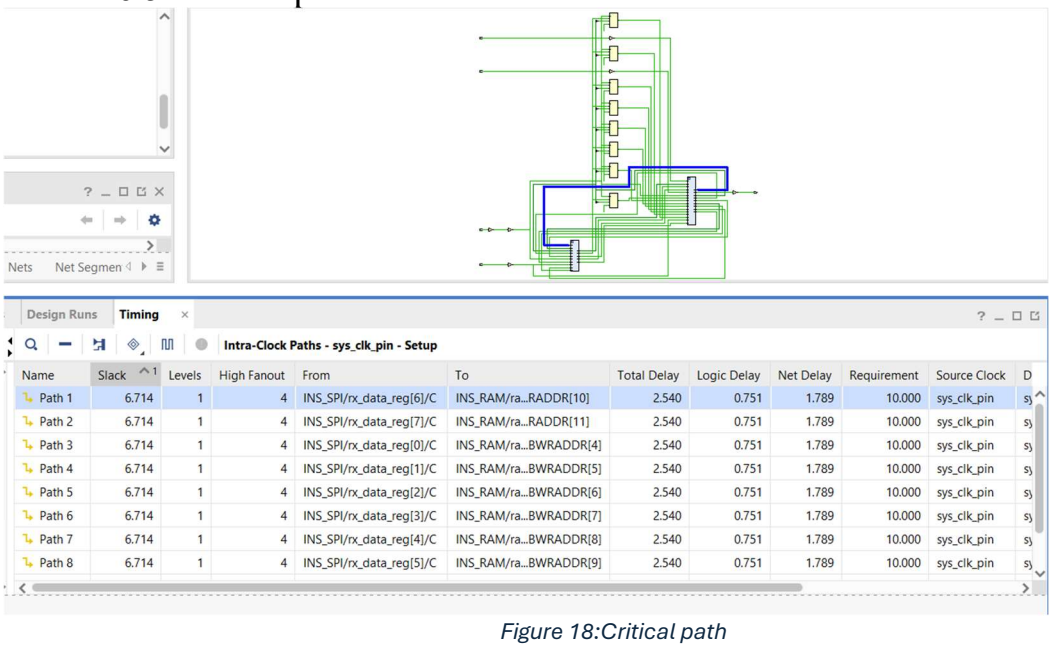
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.714 ns	Worst Hold Slack (WHS):	0.142 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	85	Total Number of Endpoints:	85	Total Number of Endpoints:	40

All user specified timing constraints are met.

Figure 17:Design Timing summary

6.5 Critical path



Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	D
Path 1	6.714	1	4	INS_SPI/rx_data_reg[6]/C	INS_RAM/ra...RADDR[10]	2.540	0.751	1.789	10.000	sys_clk_pin	s
Path 2	6.714	1	4	INS_SPI/rx_data_reg[7]/C	INS_RAM/ra...RADDR[11]	2.540	0.751	1.789	10.000	sys_clk_pin	s
Path 3	6.714	1	4	INS_SPI/rx_data_reg[0]/C	INS_RAM/ra...BWRADDR[4]	2.540	0.751	1.789	10.000	sys_clk_pin	s
Path 4	6.714	1	4	INS_SPI/rx_data_reg[1]/C	INS_RAM/ra...BWRADDR[5]	2.540	0.751	1.789	10.000	sys_clk_pin	s
Path 5	6.714	1	4	INS_SPI/rx_data_reg[2]/C	INS_RAM/ra...BWRADDR[6]	2.540	0.751	1.789	10.000	sys_clk_pin	s
Path 6	6.714	1	4	INS_SPI/rx_data_reg[3]/C	INS_RAM/ra...BWRADDR[7]	2.540	0.751	1.789	10.000	sys_clk_pin	s
Path 7	6.714	1	4	INS_SPI/rx_data_reg[4]/C	INS_RAM/ra...BWRADDR[8]	2.540	0.751	1.789	10.000	sys_clk_pin	s
Path 8	6.714	1	4	INS_SPI/rx_data_reg[5]/C	INS_RAM/ra...BWRADDR[9]	2.540	0.751	1.789	10.000	sys_clk_pin	s

Figure 18:Critical path

7 Implementation-gray encoding:

7.1 Utilization report

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_SLAVE_WITH_SINGLE_PORT_RAM	43	39	20	43	0.5	5	1
INS_RAM (RAM)	13	17	5	13	0.5	0	0
INS_SPI (SPI)	30	22	17	30	0	0	0

Figure 19:Utilization report

7.2 Timing report

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.023 ns	Worst Hold Slack (WHS):	0.118 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	87	Total Number of Endpoints:	87	Total Number of Endpoints:	42

All user specified timing constraints are met.

Figure 20:Timing report

7.3 FPGA device

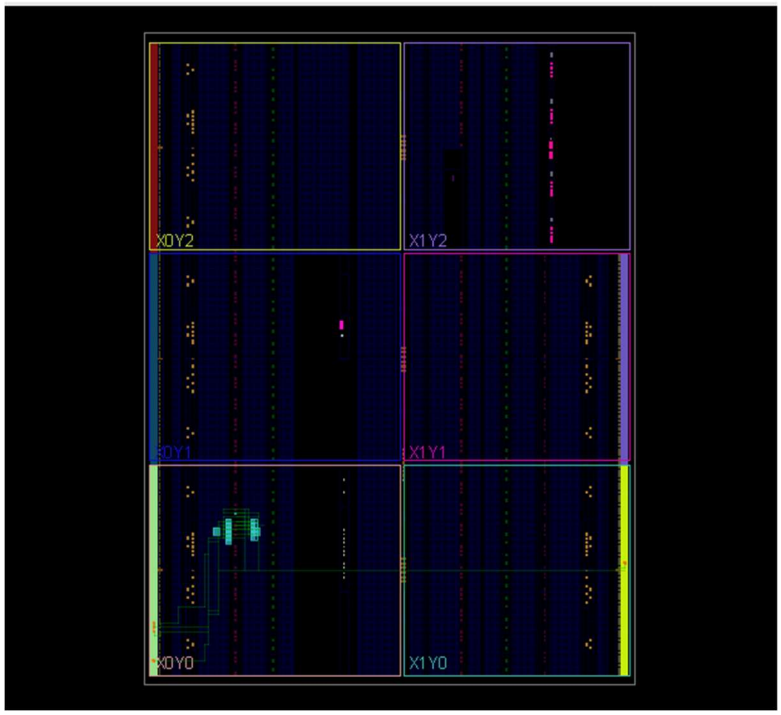


Figure 21:FPGA device

7.4 Bitstream generate

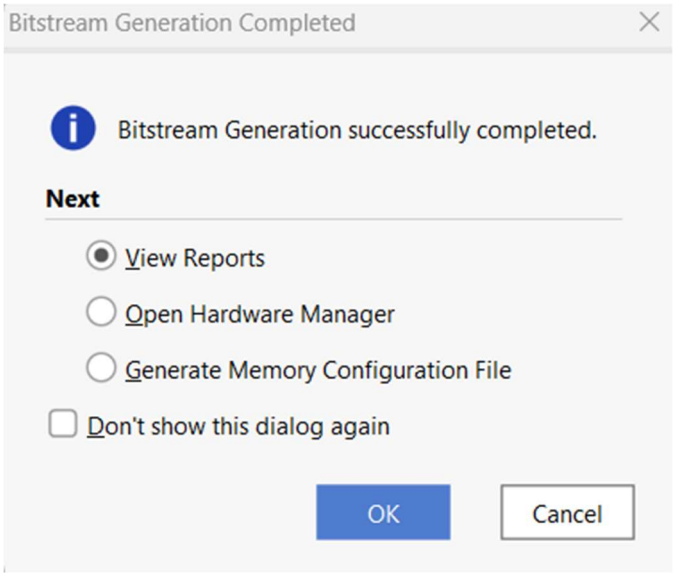


Figure 22:Bitstream generate

8 Synthesis snippets- sequential encoding:

8.1 Schematic after the elaboration

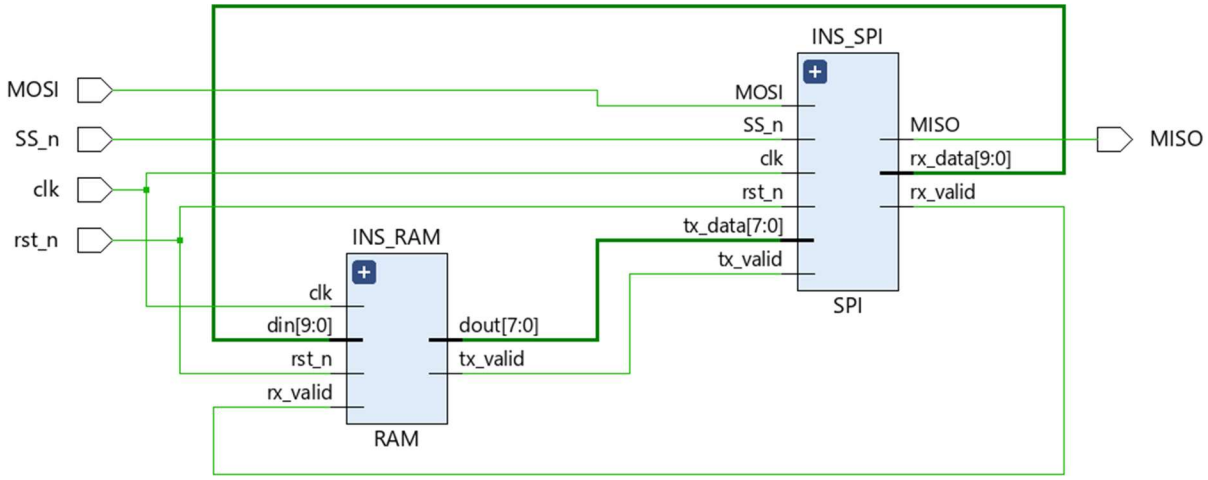


Figure 23:Schematic after the elaboration

8.2 Schematic after the Synthesis

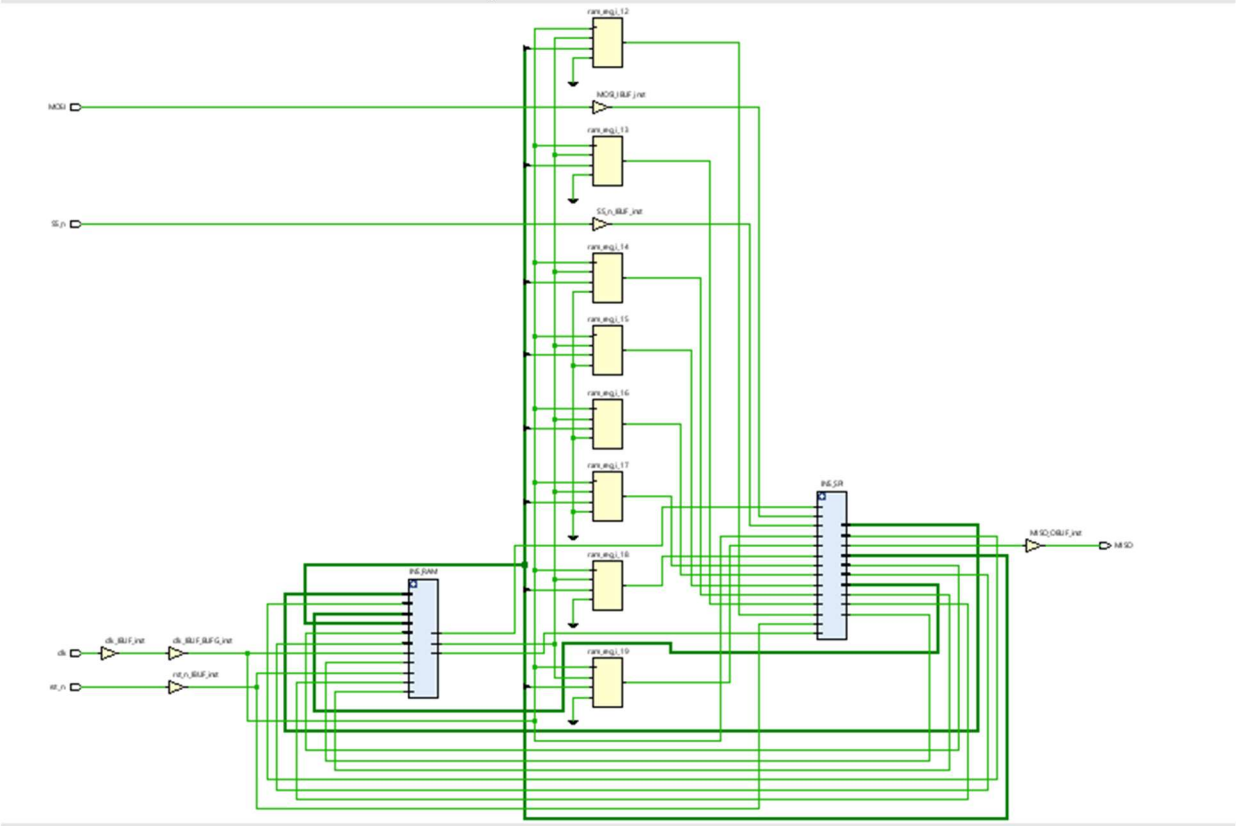


Figure 24:Schematic after the Synthesis

8.3 Synthesis report showing the encoding used

```
INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI'
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |               Previous Encoding
---------------------------------------------------------------------------------------------------
                    IDLE |                              000 |                            00001
                 CHK_CMD |                              001 |                            00010
                   WRITE |                              010 |                            00011
               READ_DATA |                              011 |                            00101
                READ_ADD |                              100 |                            00100
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI'
```

Figure 25:Synthesis report showing the encoding used

8.4 Design Timing summary

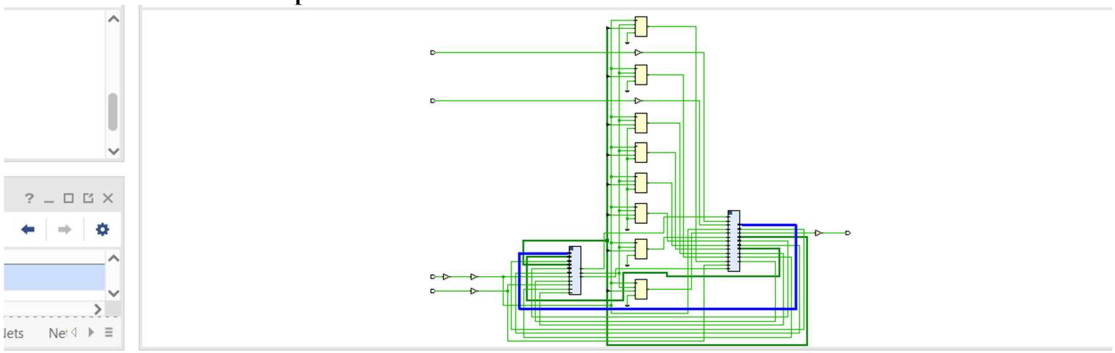
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.714 ns	Worst Hold Slack (WHS):	0.142 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	85	Total Number of Endpoints:	85	Total Number of Endpoints:	40

All user specified timing constraints are met.

Figure 26:Design Timing summary

8.5 Critical path



Design Runs | Timing | Debug

Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	6.714	1	4	INS_SPI/rx_data_reg[6]/C	INS_RAM/ra...RADDR[10]	2.540	0.751	1.789	10.000	sys_clk_pin
Path 2	6.714	1	4	INS_SPI/rx_data_reg[7]/C	INS_RAM/ra...RADDR[11]	2.540	0.751	1.789	10.000	sys_clk_pin
Path 3	6.714	1	4	INS_SPI/rx_data_reg[0]/C	INS_RAM/ra...BWRADDR[4]	2.540	0.751	1.789	10.000	sys_clk_pin
Path 4	6.714	1	4	INS_SPI/rx_data_reg[1]/C	INS_RAM/ra...BWRADDR[5]	2.540	0.751	1.789	10.000	sys_clk_pin
Path 5	6.714	1	4	INS_SPI/rx_data_reg[2]/C	INS_RAM/ra...BWRADDR[6]	2.540	0.751	1.789	10.000	sys_clk_pin
Path 6	6.714	1	4	INS_SPI/rx_data_reg[3]/C	INS_RAM/ra...BWRADDR[7]	2.540	0.751	1.789	10.000	sys_clk_pin
Path 7	6.714	1	4	INS_SPI/rx_data_reg[4]/C	INS_RAM/ra...BWRADDR[8]	2.540	0.751	1.789	10.000	sys_clk_pin

Figure 27:Critical path

9 Implementation- sequential encoding:

9.1 Utilization report

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_SLAVE_WITH_SINGLE_PORT_RAM	31	37	20	31	0.5	5	1
INS_RAM (RAM)	6	9	7	6	0.5	0	0
INS_SPI (SPI)	28	20	19	28	0	0	0

Figure 28:Utilization report

9.2 Timing report

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.979 ns	Worst Hold Slack (WHS):	0.076 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	86	Total Number of Endpoints:	86	Total Number of Endpoints:	40

All user specified timing constraints are met.

Figure 29:Timing report

9.3 FPGA device

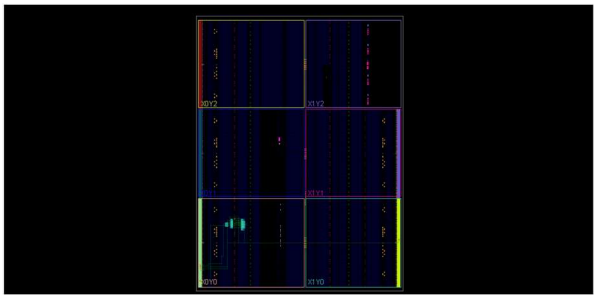


Figure 30:FPGA device

9.4 Bitstream generate

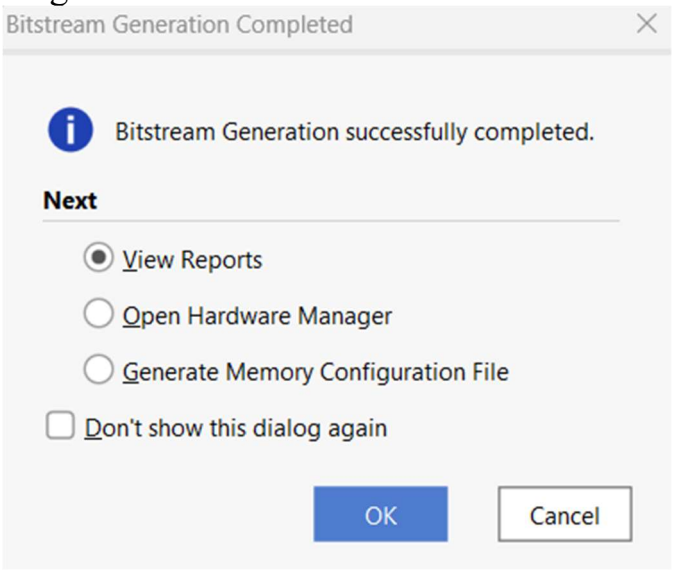


Figure 31:Bitstream generate

10 BEST ENCODING:

In previous simulations we test “gray” and “sequential” ,”One_hot” encoding and will choose the highest implementation slack to make debug core .

In this situation the best encoding is sequential encoding with high frequency 500Mhz:

Sequential encoding with debug core :

10.1 Utilization report

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
N SPI_SLAVE_WITH_SINGLE_PORT_RAM	1221	1967	3	642	1113	108	1	5	2	1
dbg_hub (dbg_hub)	453	741	0	236	429	24	0	0	1	1
INS_RAM (RAM)	4	9	0	5	4	0	0.5	0	0	0
INS_SPI (SPI)	27	20	0	17	27	0	0	0	0	0
u_ila_0 (u_ila_0)	737	1189	3	397	653	84	0.5	0	0	0

Figure 32:Utilization report

10.2 Timing report

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.097 ns	Worst Hold Slack (WHS):	0.022 ns	Worst Pulse Width Slack (WPWS):	1.250 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	3890	Total Number of Endpoints:	3874	Total Number of Endpoints:	2154

All user specified timing constraints are met.

Figure 33:Timing report

10.3 FPGA device

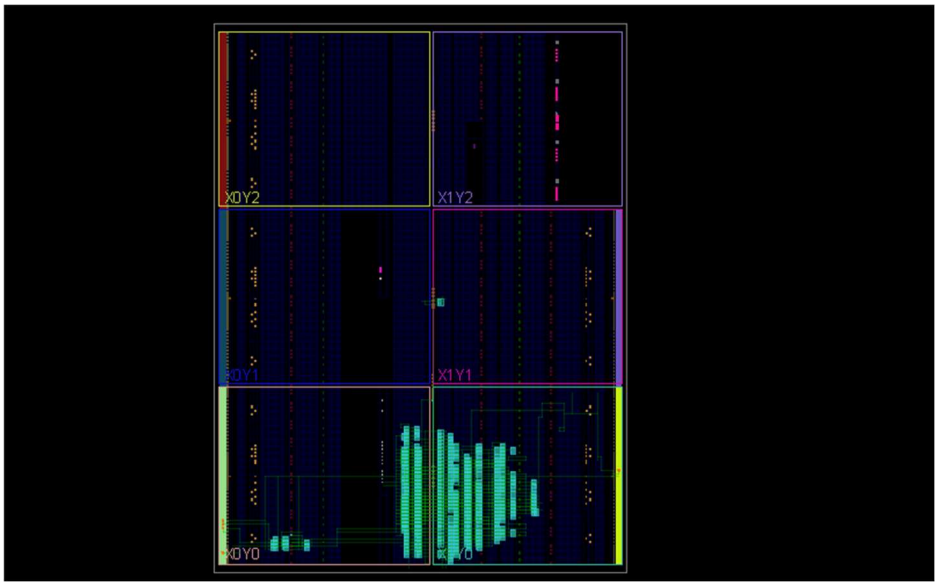


Figure 34:FPGA device

10.4 Bitstream generate

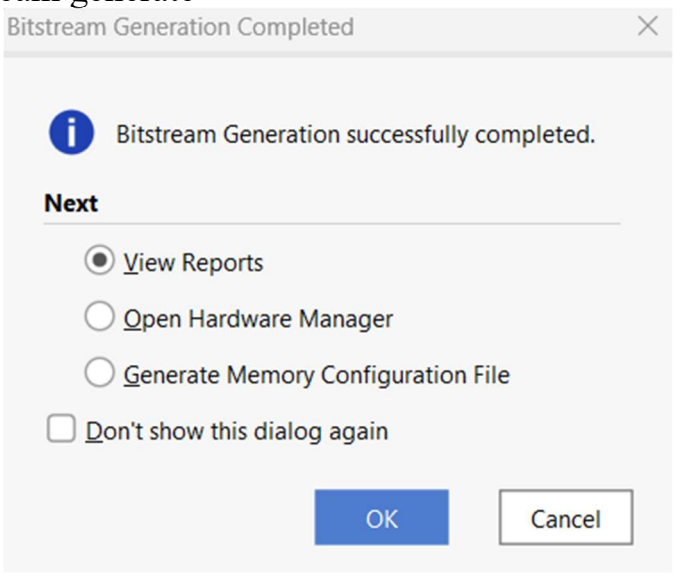


Figure 35:Bitstream generate