"Digital IC Design Diploma"

Data Synchronizer

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Submitted by:

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The following snippets are some of the testing scenarios of the functionality of the Data Synchronizer:

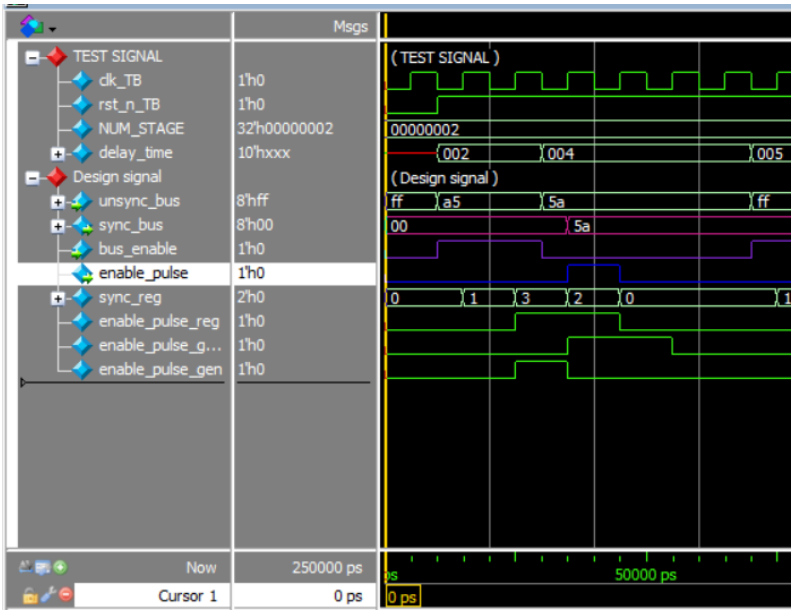

Figure 1: The start of the simulation, reset asserts and deasserts as shown by the yellow pointer

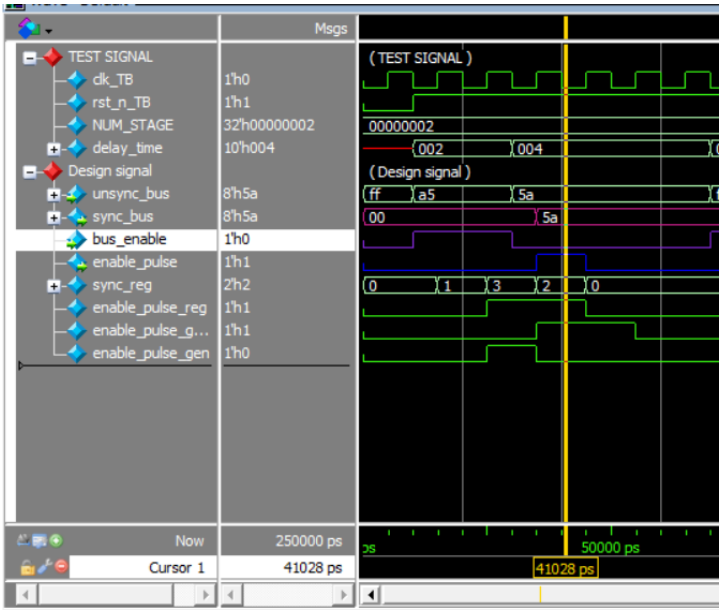

Figure 2: insert a5 on a bus and not wait enough time, and another data 5a is gone.

Note: this must be taken into mind, and the speed of the sender must be slower than the receiver's speed

At least three times, or take into account the routing delay.

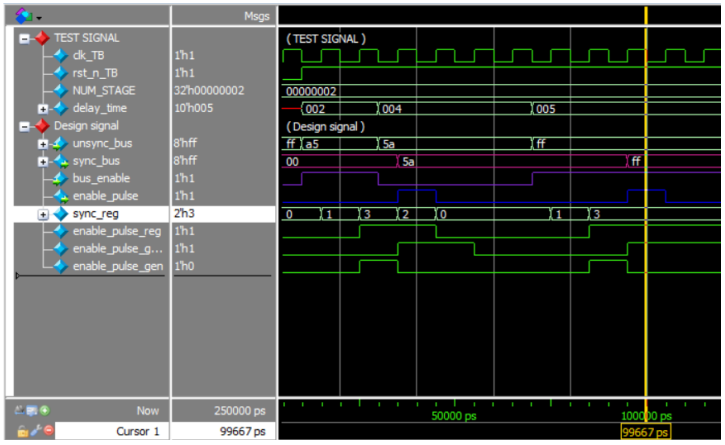

Figure 3: Insert FF on a bus and enable the bus too much, and the data is transmitted correctly after three cycles.

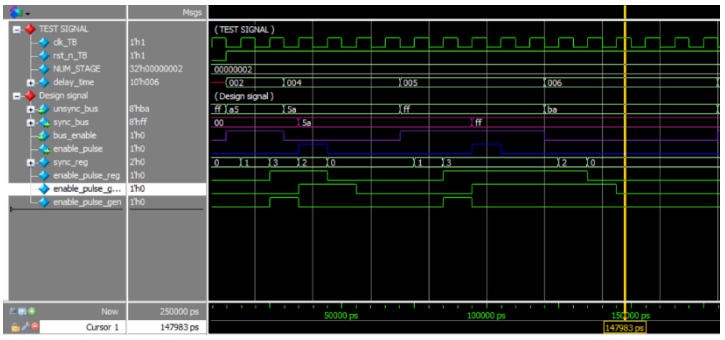

Figure 4: Insert BA on a bus and do not enable the bus too much; the data is not transmitted.