"Digital IC Design Diploma"

Clock Divider Assignment

Under supervision of:

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Submitted by:

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The following snippets are some of the testing scenarios of the functionality of the Clock Divider block:

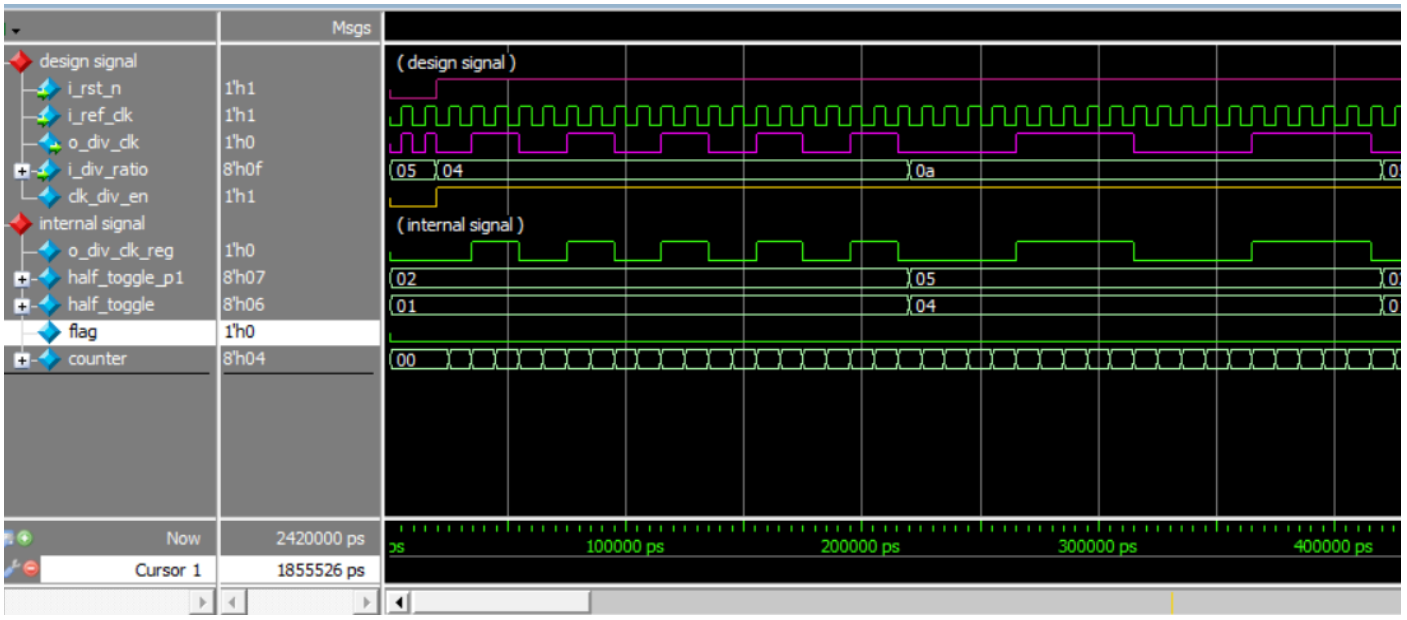

Figure 1: The start of the simulation, reset is asserted and the cases of driving the division by even value.

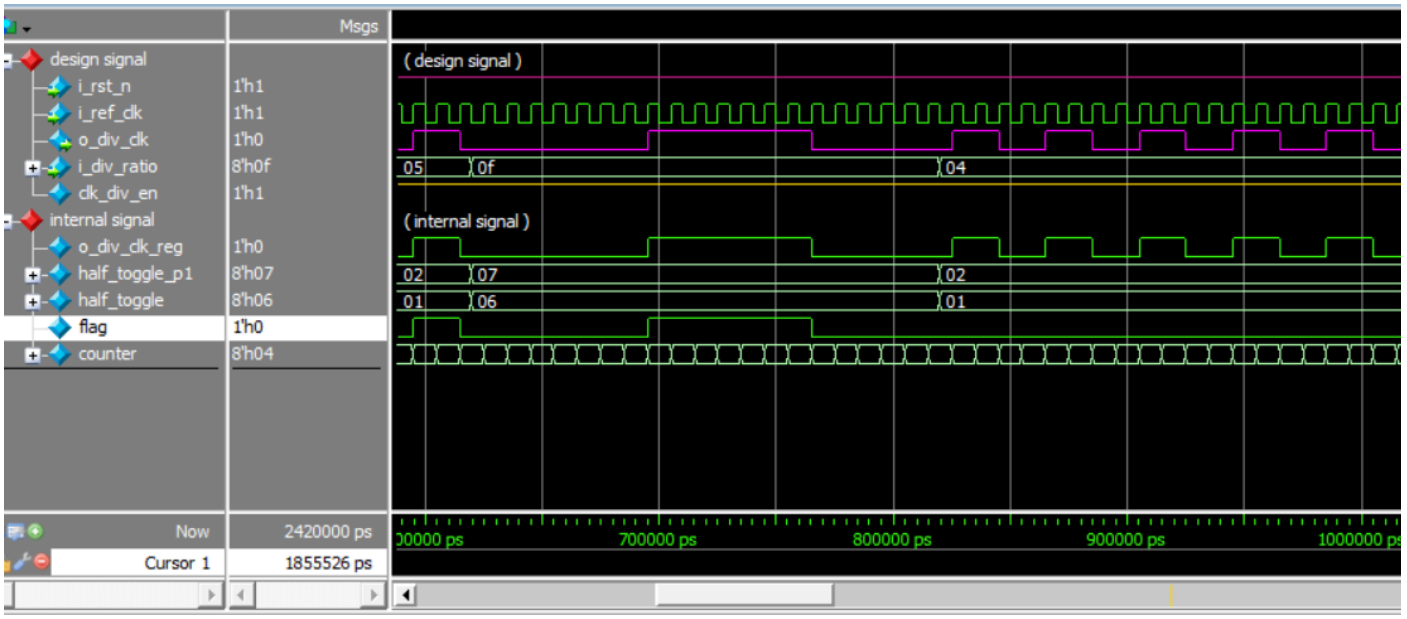

Figure 2: The generated clock when the division ratio is 15 then 4.

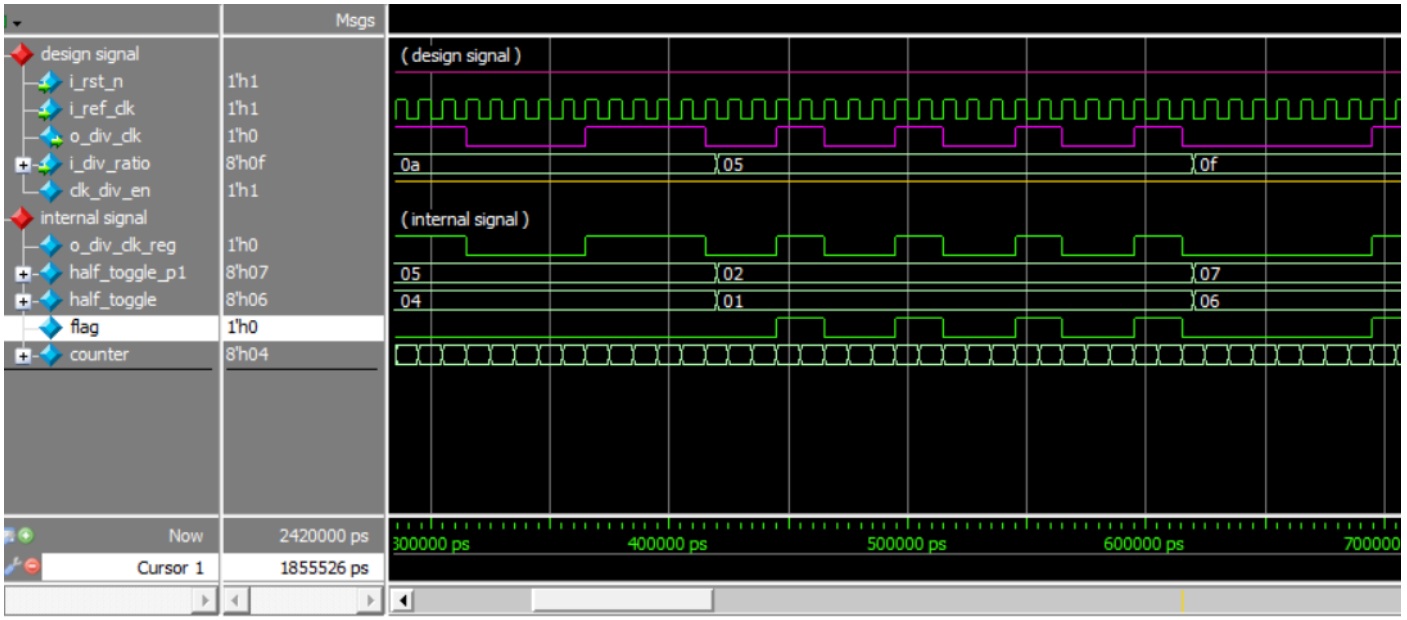

Figure 3: The generated clock when the division ratio is 5 and show valid duty cycle.

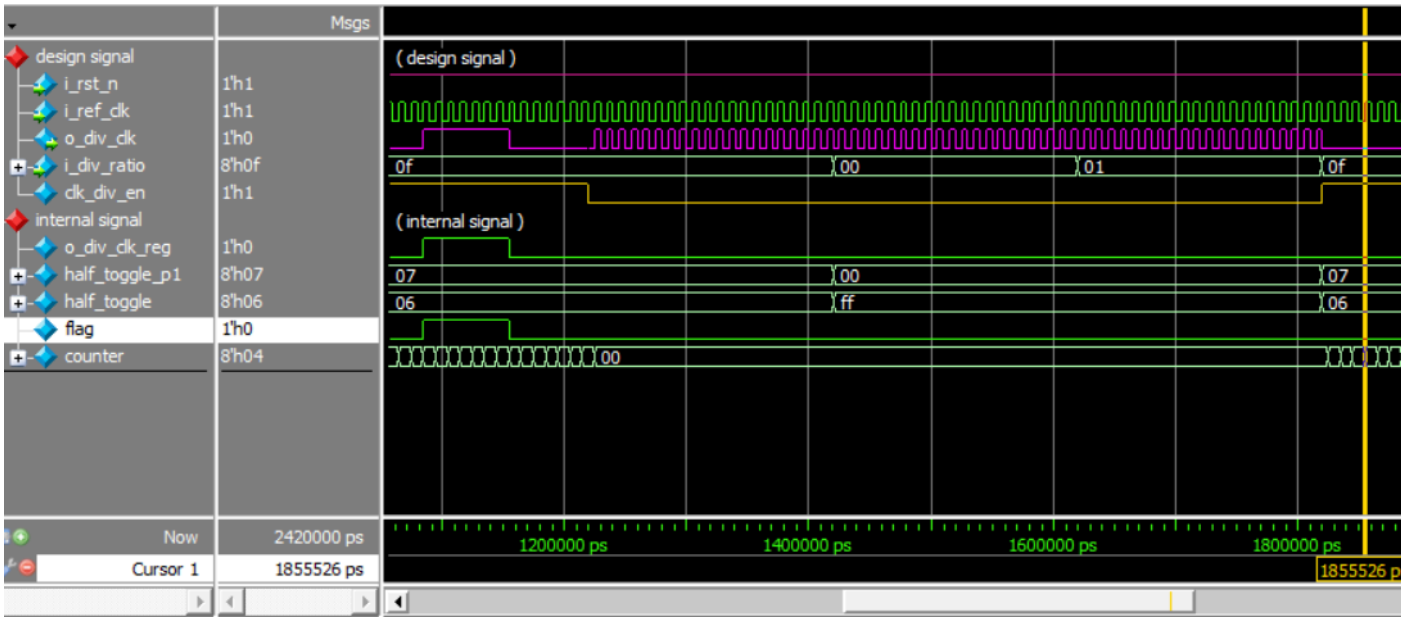

Figure 4: The generated clock when the division ratio is 0 and 1 and enable off.

NOTE: the generated clock in this case is the same as the reference clock.

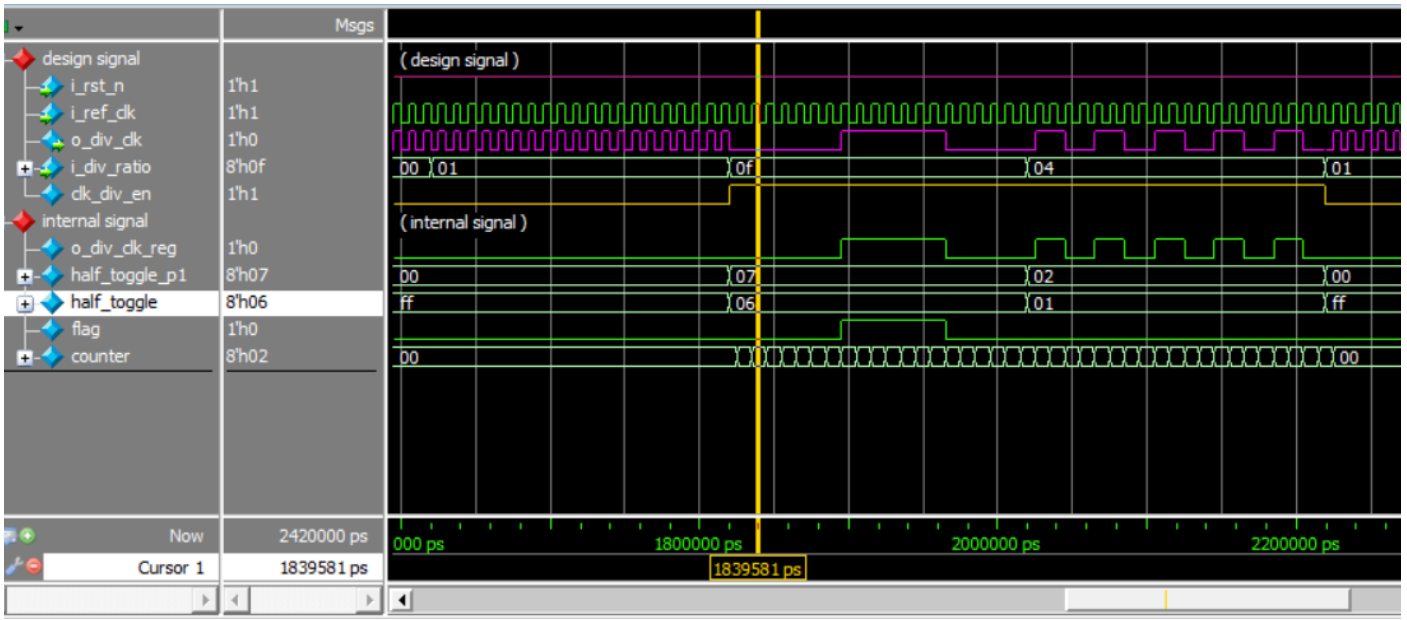

Figure 5: The generated clock when the clock divider enable is active and show valid division after division invalid in previous case.