"Digital IC Design Diploma"

RESET Synchronizer

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The following snippets are some of the testing scenarios of the functionality of the reset Synchronizer:

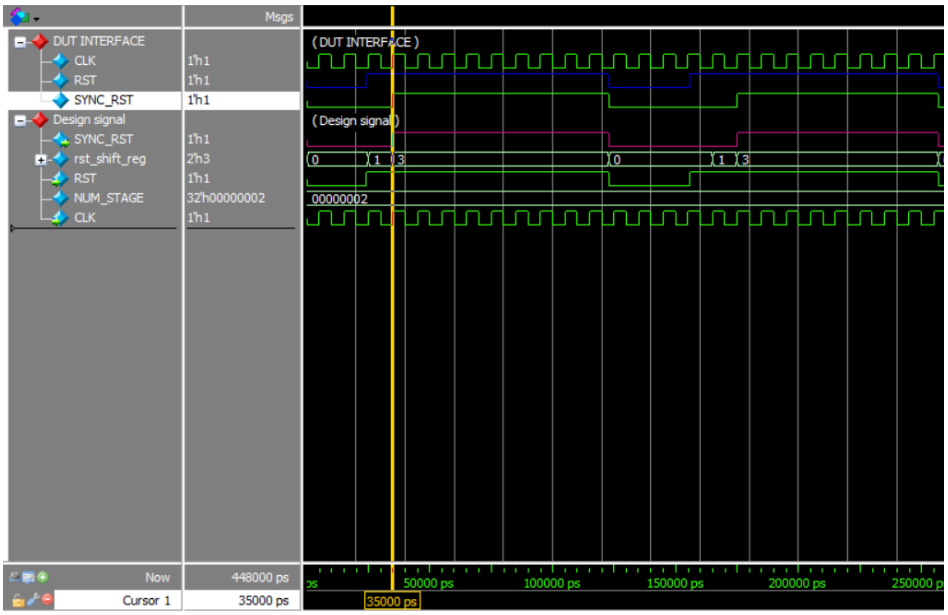

Figure 1: The start of the simulation, reset asserts and deasserts two times in the violation region

***NOTE:** The reset deassert signal has a delay of two cycles*

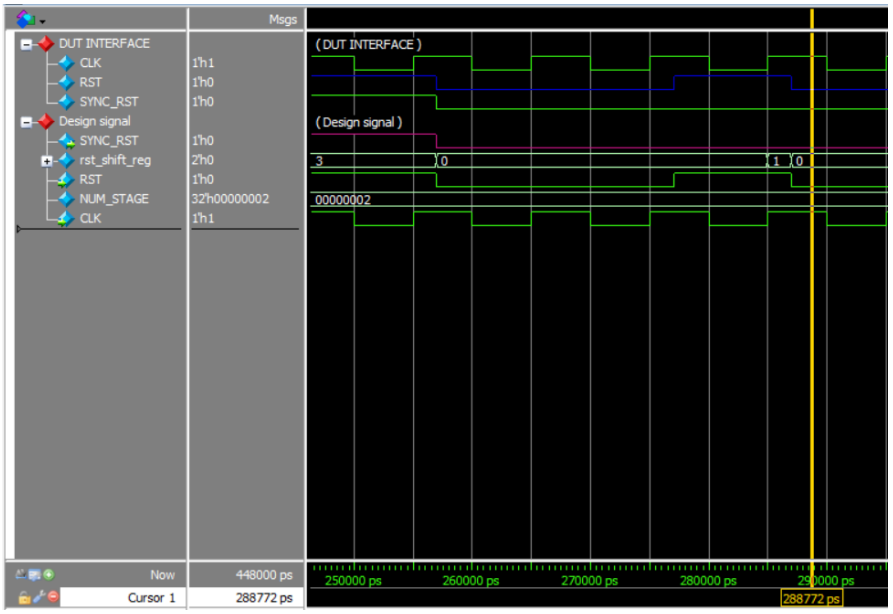

Figure 2: Assert and deassert the reset signal for not enough time.

Note: The deassert reset has not enough time to capture