"Digital IC Design Diploma"

Asynchronous FIFO

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Submitted by:

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The following snippets are some of the testing scenarios of the functionality of the Asynchronous FIFO

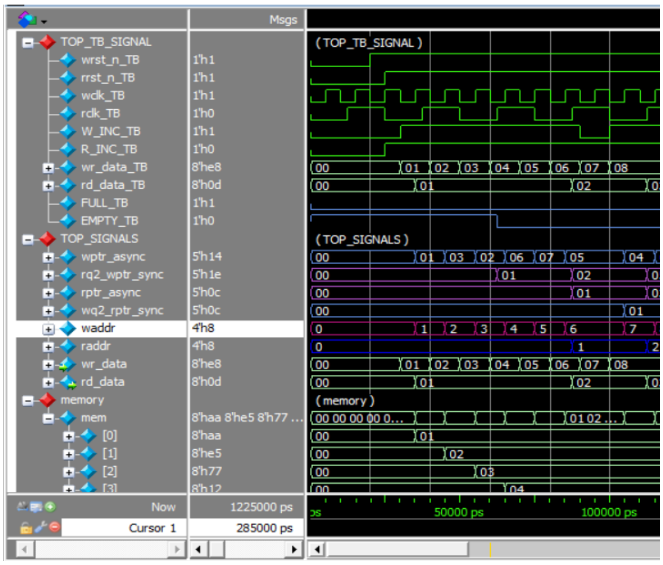

Figure 1: The start of the simulation, reset asserts and deasserts as shown, and shows the empty flag and full flag

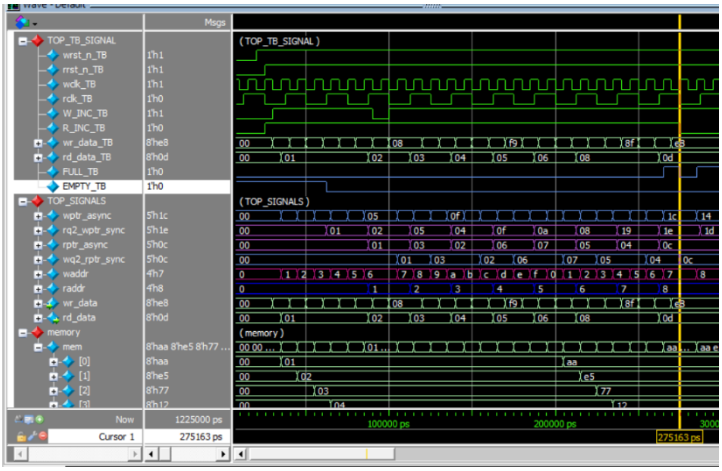

Figure 2: assert read and write enable, and show the data read and the flags behavioral.

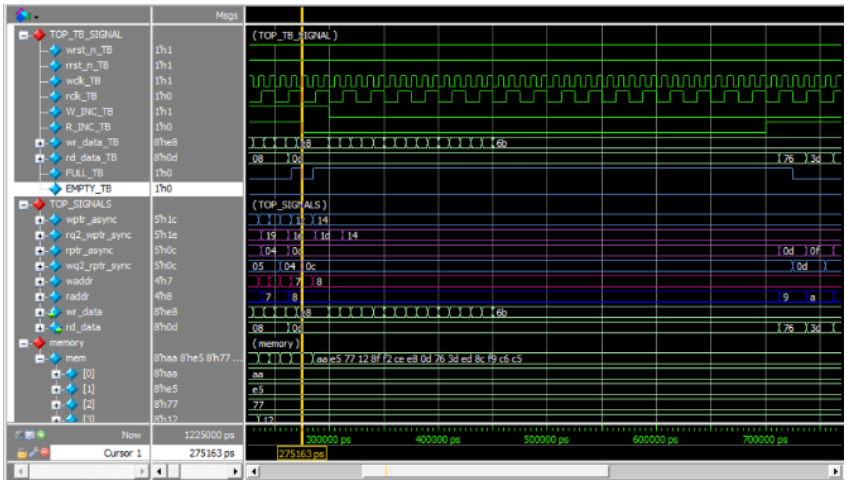

Figure 3: deassert the read and write that do not read the next data and do not change the pointer_reg.

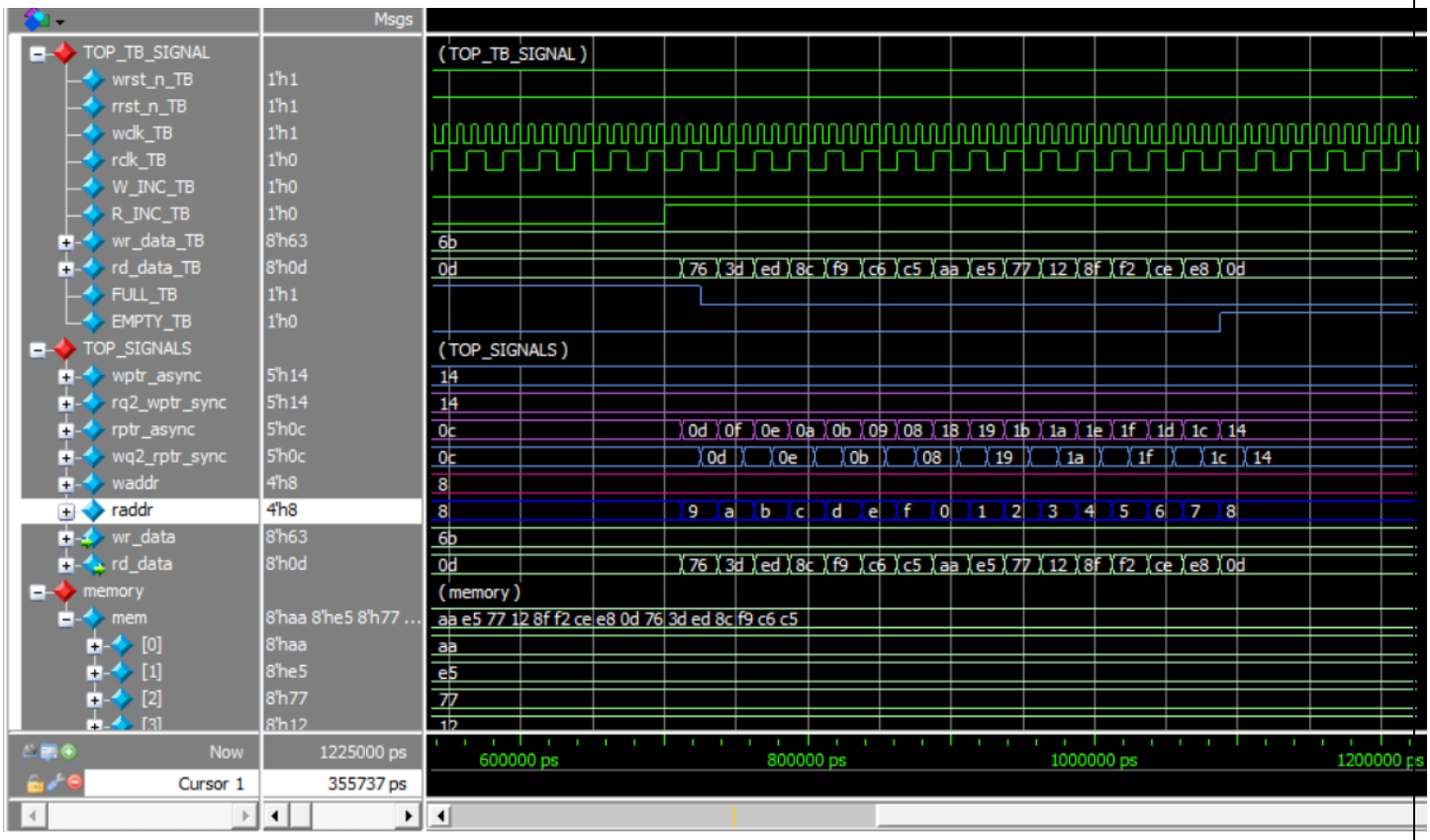

Figure 4: Insert read enable, and after reading, the empty flag should be high.

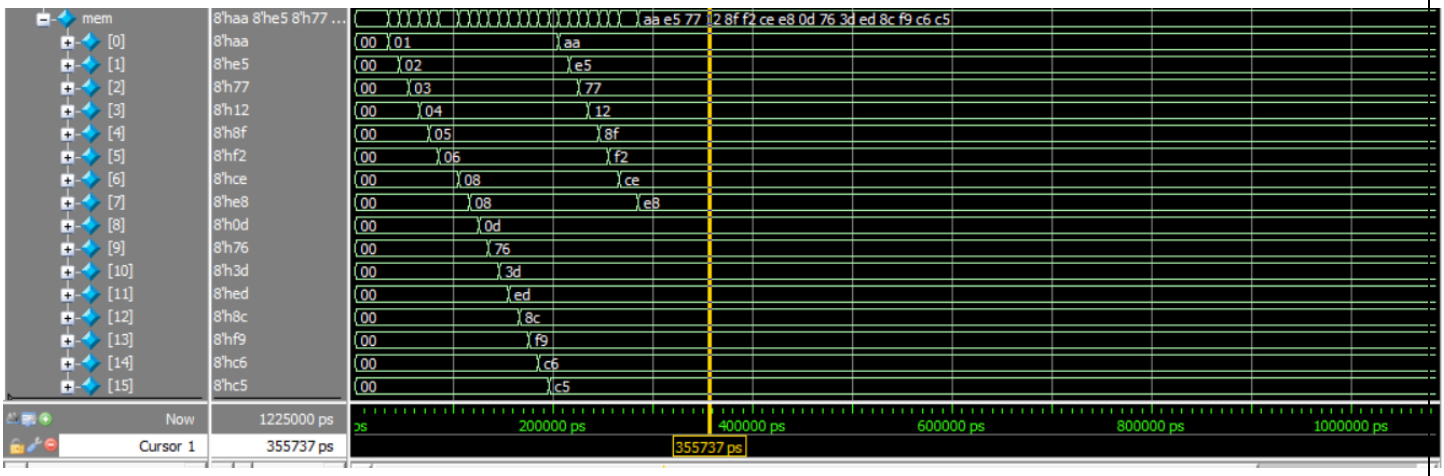

Figure 4: memory values.

```
#    Time: 0 ps  Iteration: 0  Process: /ASYNC_FIFO_TB/#INITIAL#49 File: ASYNC_FIFO_TB.v Line: 50
# success: FIFO is Full as expected
# success: FIFO is empty as expected
```

Figure 4: memory values.