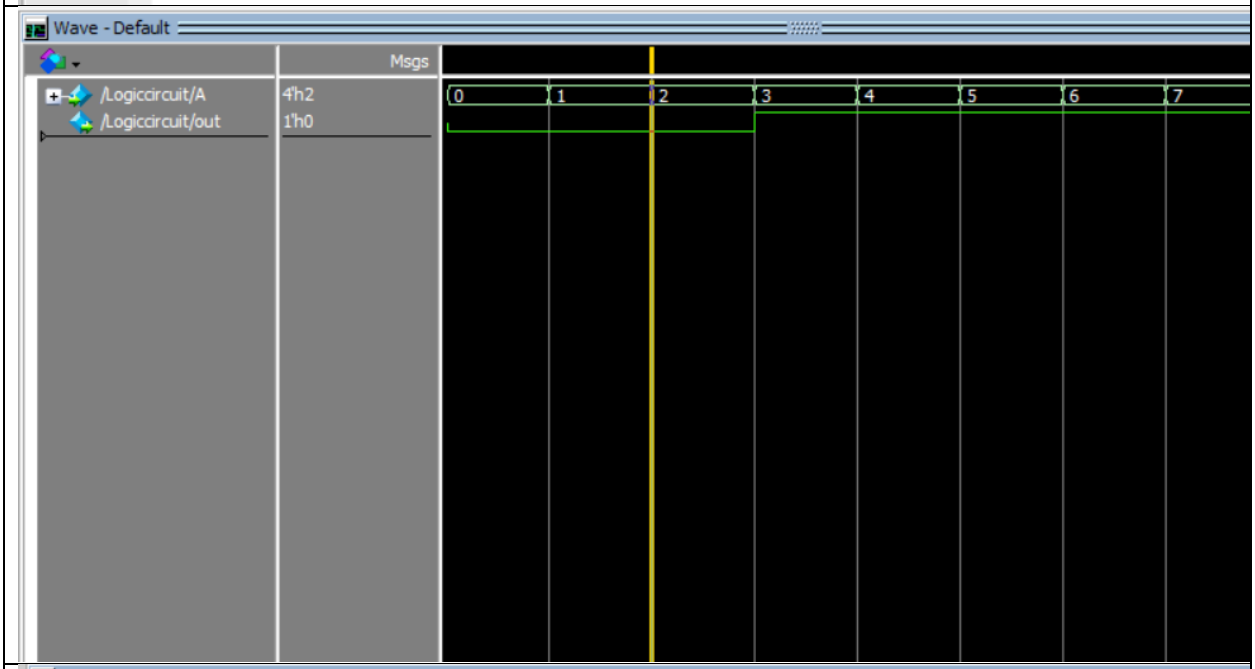
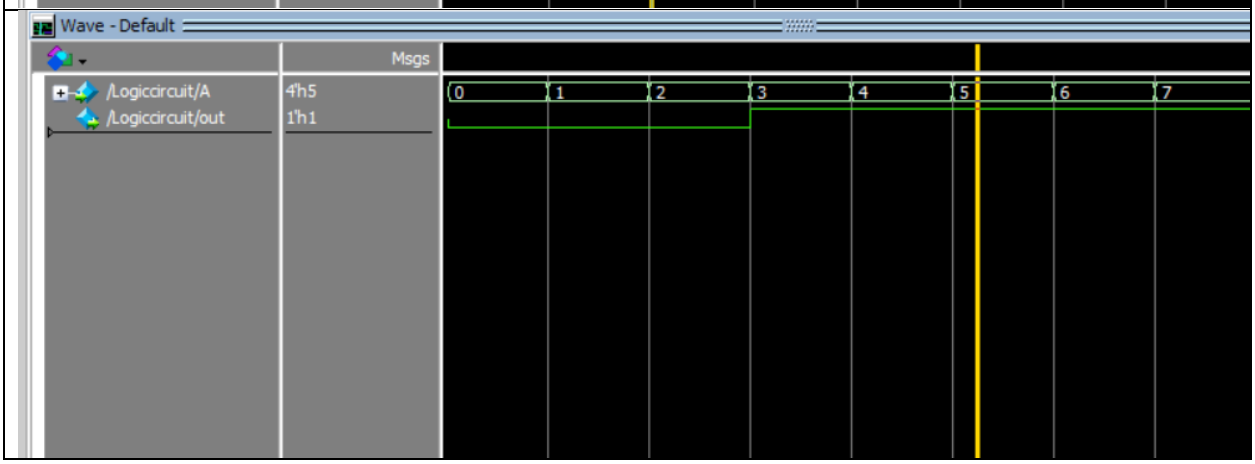
1)

C:/questasim64_2021.1/examples/LOGICCIRCUIT.v (/Logiccircuit) - Default

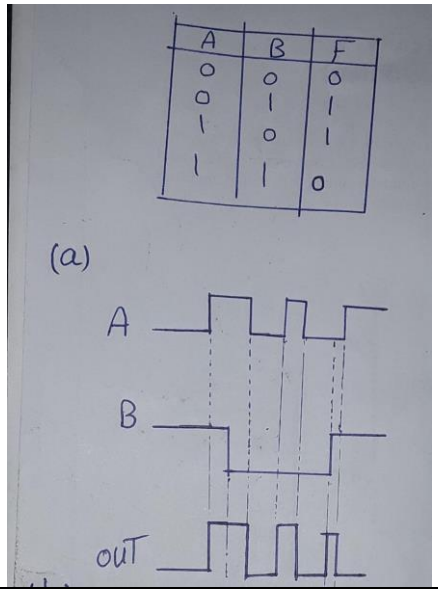
```
Ln#
1  module Logiccircuit(A,out);
2  input [3:0]A;
3  output out;
4  assign out =(A[2]&(!A[3]))|(A[0]&A[1]&(!A[3]));
5  endmodule
6
```

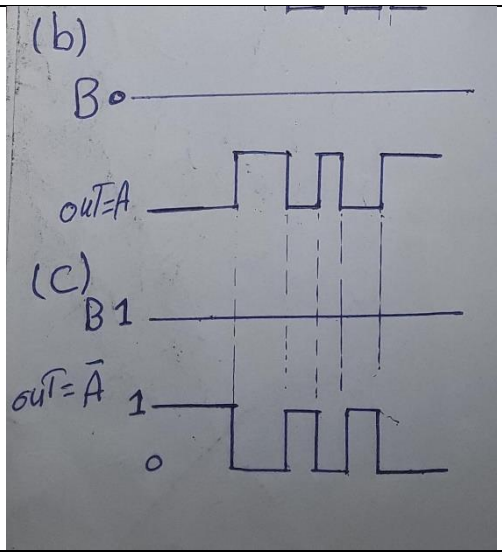





Wave - Default
Msgs
/Logiccircuit/A
/Logiccircuit/out
4'hb
1'h0
6
7
8
9
a
b
c
d
e
f

2)


A
B
F
0 0 0
0 1 1
1 0 1
1 1 0
(a)
A
B
OUT

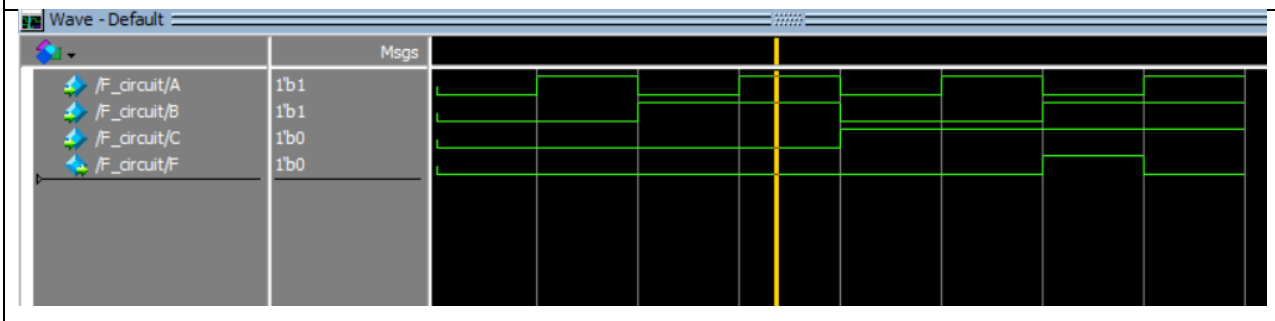


3)

C:/questasim64_2021.1/examples/eight_CODE.v (/F_circuit) - Default

Ln#

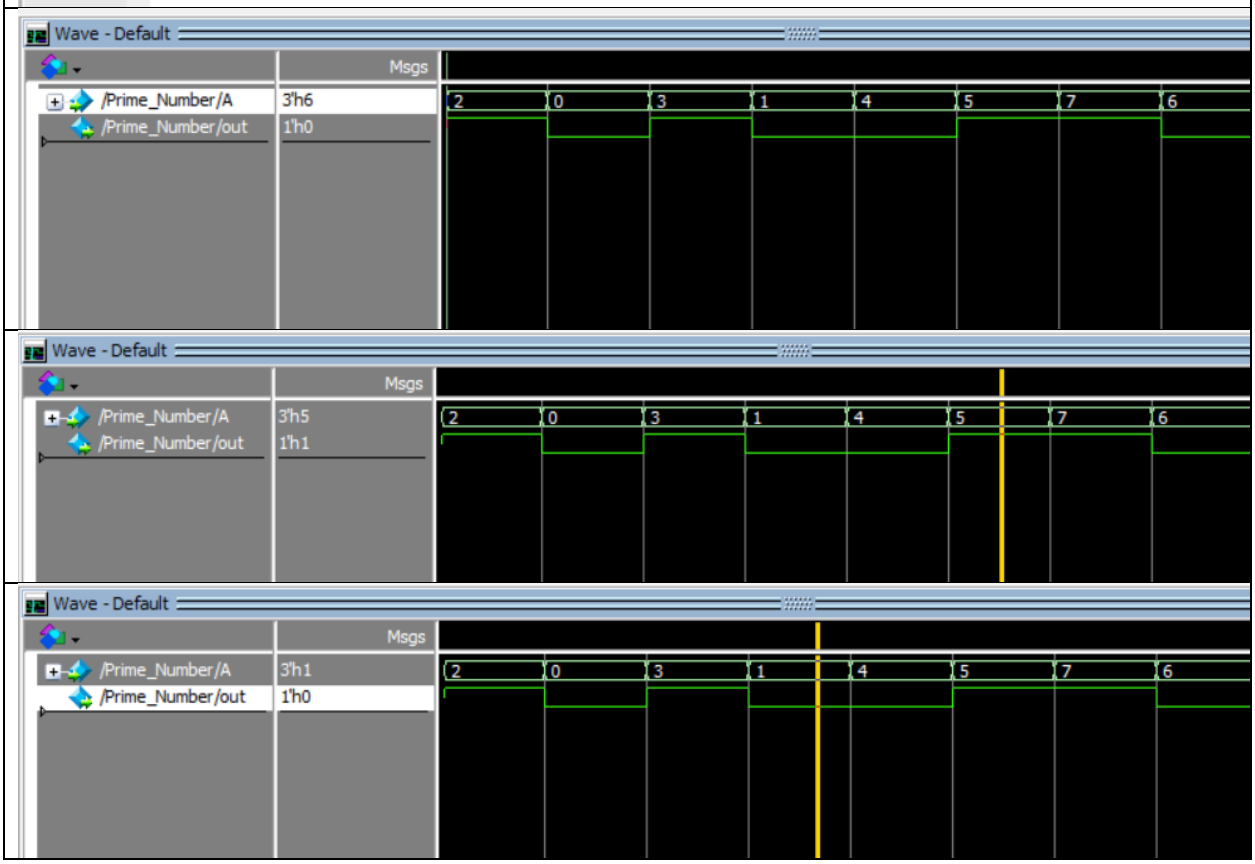
```
1  module F_circuit(A,B,C,F);
2  input A,B,C;
3  output F;
4  assign F=(C==1)?((B==1)?((A==0)?1'b1:1'b0):1'b0):1'b0;
5  endmodule
6
```



4)

C:/questasim64_2021.1/examples/Prime_Number.v (/Prime_Number) - Default

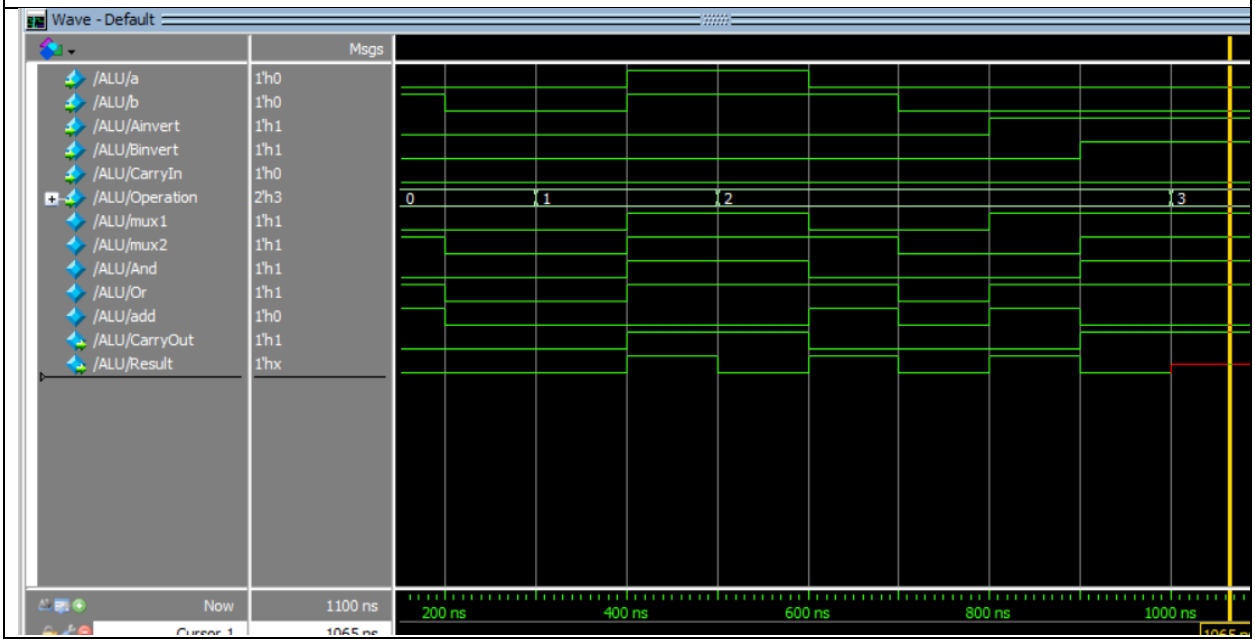
```
Ln#
1  module Prime_Number(A,out);
2  input [2:0]A;
3  output out;
4  assign out = (A[1] & (!A[2])) | (A[0] & A[2]);
5  endmodule
6
```

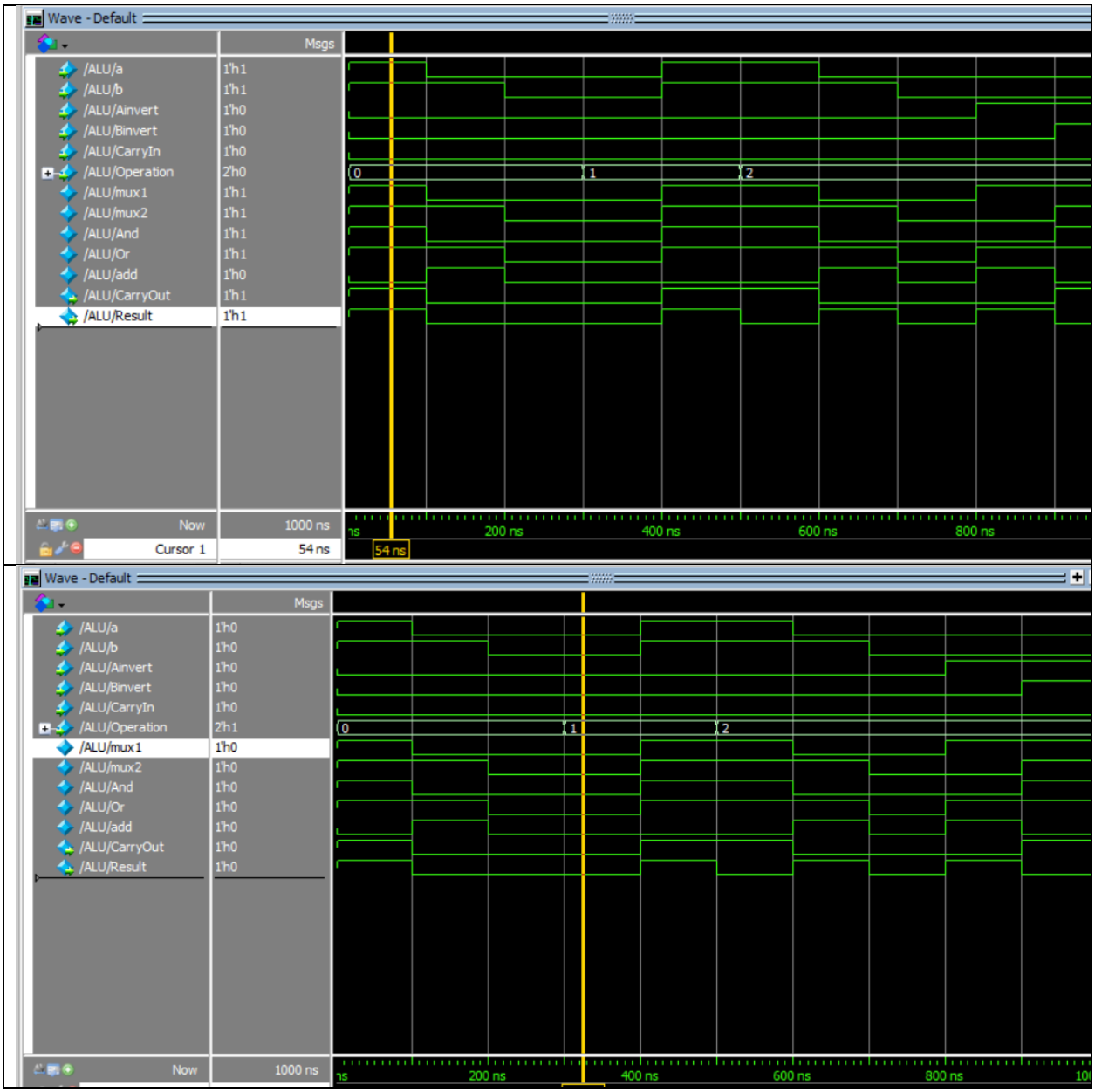


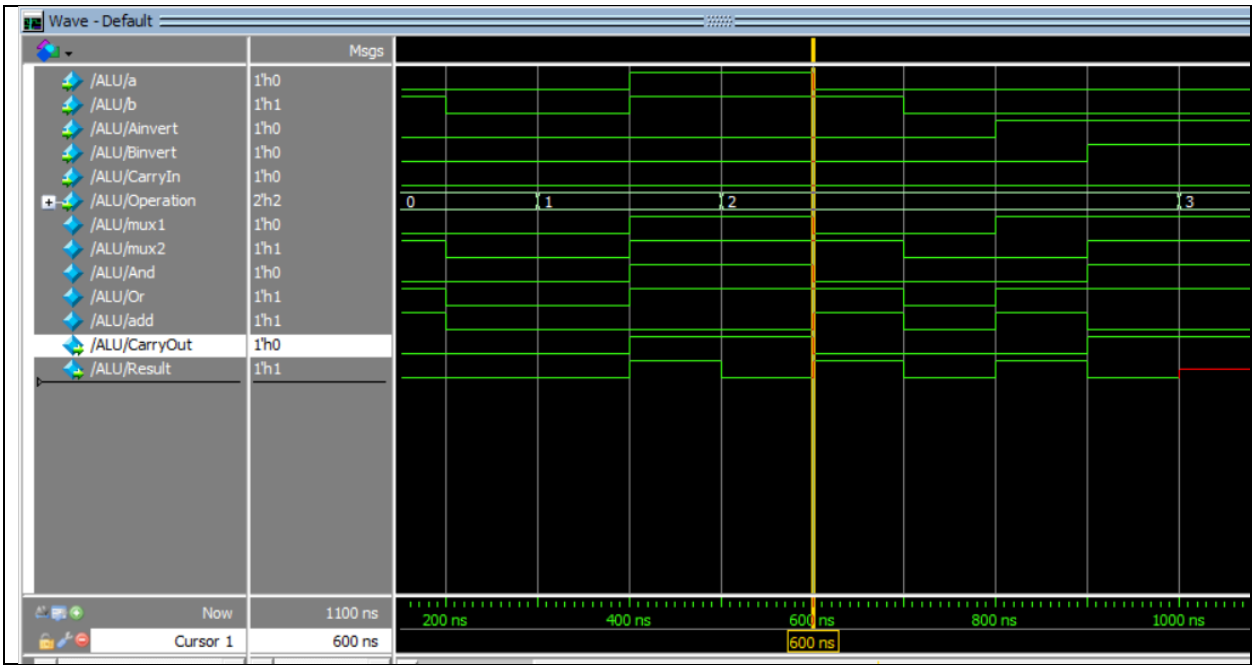
5)

C:/questasim64_2021.1/examples/TEN_CODE.v (/ALU) - Default

```
Ln#
1  module ALU(a,b,Ainvert,Binvert,CarryIn,Operation,CarryOut,Result);
2  input a,b,Ainvert,Binvert,CarryIn;
3  input [1:0]Operation;
4  output CarryOut,Result;
5  wire mux1,mux2;
6  wire And,Or,add;
7  assign mux1=(Ainvert==1)?(!a):(a);
8  assign mux2=(Binvert==1)?(!b):(b);
9  assign And=(mux1) & (mux2);
10 assign Or=(mux1) | (mux2);
11 assign {CarryOut,add}=mux1+mux2+CarryIn;
12 assign Result= (Operation==2'b00)?And:(Operation==2'b01)?Or:(Operation==2'b10)?add:1'bx;
13 endmodule
14
```




Wave - Default
Msgs
/ALU/a
/ALU/b
/ALU/Ainvert
/ALU/Binvert
/ALU/CarryIn
/ALU/Operation
/ALU/mux1
/ALU/mux2
/ALU/And
/ALU/Or
/ALU/add
/ALU/CarryOut
/ALU/Result
1'h1
1'h1
1'h0
1'h0
1'h0
2'h0
1'h1
1'h1
1'h1
1'h1
1'h0
1'h1
1'h1
0
1
2
Now
1000 ns
Cursor 1
54 ns
200 ns
400 ns
600 ns
800 ns
Wave - Default
Msgs
/ALU/a
/ALU/b
/ALU/Ainvert
/ALU/Binvert
/ALU/CarryIn
/ALU/Operation
/ALU/mux1
/ALU/mux2
/ALU/And
/ALU/Or
/ALU/add
/ALU/CarryOut
/ALU/Result
1'h0
1'h0
1'h0
1'h0
1'h0
2'h1
1'h0
1'h0
1'h0
1'h0
1'h0
1'h0
1'h0
0
1
2
Now
1000 ns
200 ns
400 ns
600 ns
800 ns


Wave - Default
Msgs
/ALU/a
/ALU/b
/ALU/Ainvert
/ALU/Binvert
/ALU/CarryIn
/ALU/Operation
/ALU/mux1
/ALU/mux2
/ALU/And
/ALU/Or
/ALU/add
/ALU/CarryOut
/ALU/Result
1'h0
1'h1
1'h0
1'h0
1'h0
2'h2
1'h0
1'h1
1'h0
1'h1
1'h1
1'h0
1'h1
0
1
2
3
Now
1100 ns
Cursor 1
600 ns
200 ns
400 ns
600 ns
800 ns
1000 ns
600 ns