Assignment 5 – Extra

1) The attached design contains design issues that can be identified early in the design process. Examine the code and make a list of potential issues that the linting tool can detect. Some of these design checks we covered in class, while others did not, so do your best to detect potential synthesis issues that can be seen in the design.

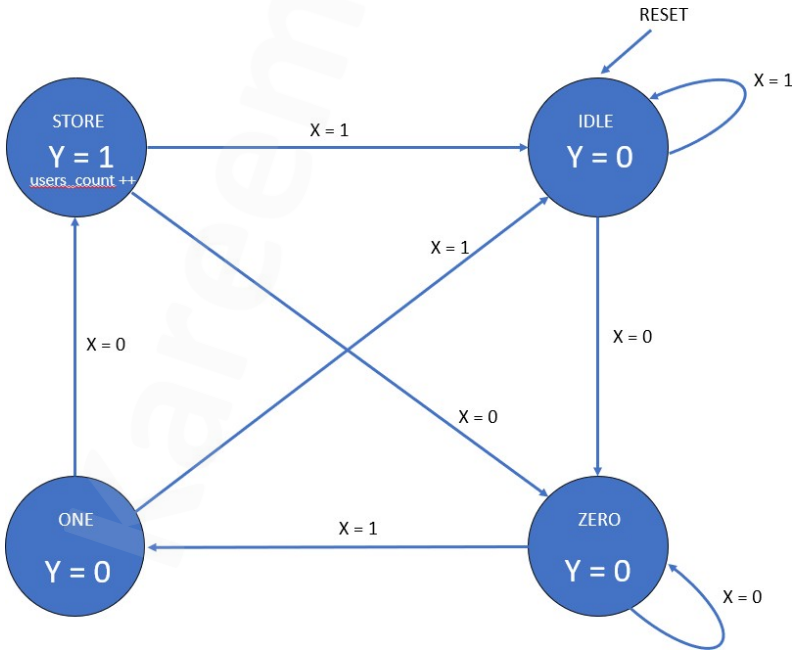
- The design is attached as Verilog file in the classroom assignment 5.

2) Requirements:

1- Design Moore FSM that detects “010” non-overlapped pattern. (Draw state transition diagram)
2- Use sequential encoding (2’b00, 2’b01, 2’b10, 2’b11)
3- Store how many time the pattern was detected (user_count is a sequential output that increments when the state is STORE)

Ports:

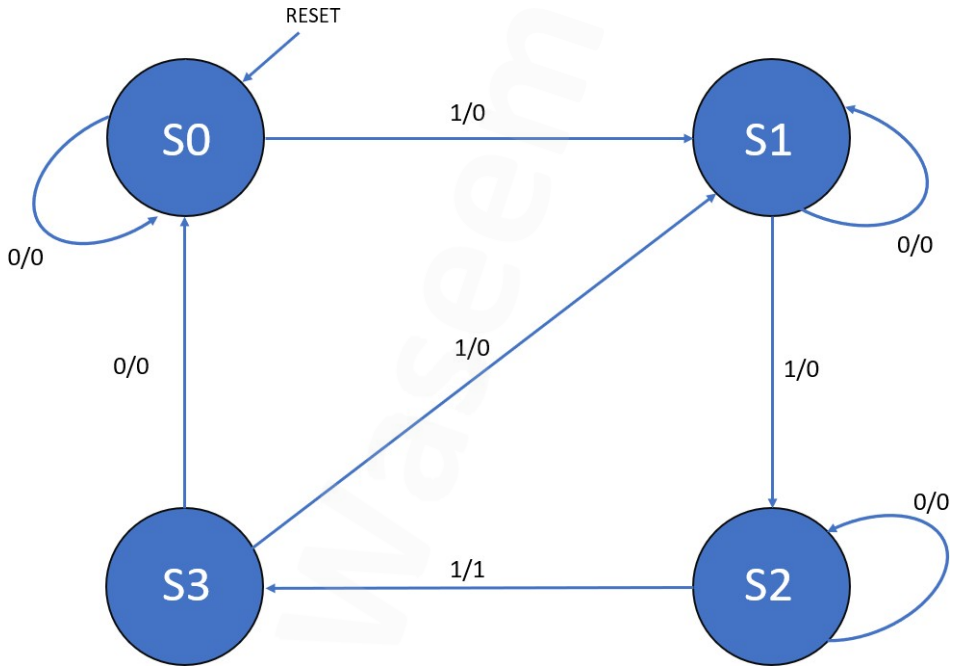
Name	Type	Size	Description
x	Input	1 bit	Input sequence
clk			Clock
rst			Active high asynchronous reset
y	Output	1 bit	Output that is HIGH when the sequence 010 is detected
count		10 bits	Outputs the number of time the pattern was detected



3) Create a sequence detector using a Mealy state machine. There is one input (in) and one output (y) in the Mealy state machine. If and only if the total number of 1s received is divisible by 3, the output yout is 1. The rst of the design is active high async.

FSM Encoding:

- S0 = 2'b00
- S1 = 2'b01
- S2 = 2'b10
- S3 = 2'b11



Create a constraint file and go through the design flow where the input in is connected to a switch, output y is connected to a led and the reset is connected to a button and then generate a bitstream file.

Deliverables:

1) The assignment should be submitted as a PDF file with this format <your_name>_Assignment5_Extra.
2) Snippets from the waveforms captured from QuestaSim for each design with inputs assigned values and output values visible
3) Snippets from the schematic after the elaboration
4) Snippet from the schematic after the synthesis and memories should be inferred in the synthesis schematic
5) Snippet from the utilization report
6) Snippet from the device after implementation

Note that your document should be organized as 3 sections corresponding to each design above, and in each section, I am expecting the Verilog code, and the snippets above.