SV synchronous FIFO project

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Verification plan:

Label	Description	Stimulus Generation	Functional Coverage (Later)	Functionality Check
almostfull_p	when the reset deasserted and count is equal FIFO_DEPTH - 1,the almostfull flag is asserted	concurrent assert		concurrent assertion to check for the almostfull flag functionality
property full_p	when the reset deasserted and write enable is high and count is lower than FIFO_DEPTH,the full flag is asserted	concurrent assert	-	concurrent assertion to check for the full flag functionality
empty_p	when the reset deasserted and read enable is high and count is equal to 0 the empty flag is asserted	concurrent assert		concurrent assertion to check for the empty flag functionality
almostempty_p	when the reset deasserted and count is equal 1,the almostempty flag is asserted	concurrent assert		concurrent assertion to check for the almostempty flag functionality
overflow_p	when the reset deasserted and write enable is high and the full flag is asserted then the overflag flag is asserted	concurrent assert		concurrent assertion to check for the overflag flag functionality
underflow_p	when the reset deasserted and read enable is high and the empty flag is asserted then the underflag flag is asserted	concurrent assert		concurrent assertion to check for the underflow flag functionality
wr_ack_p	when the reset deasserted and write enable is high and the full flag is not asserted then the wr_ack flag is asserted	concurrent assert		concurrent assertion to check for the wr_ack flag functionality
inc_count_p	when the reset deasserted and write enable is high and the full flag is not asserted then the wr_ack flag is	concurrent assert		concurrent assertion to check for the count varaible functionality
dec_count_p	when the reset deasserted and write enable is high and the full flag is not asserted then the wr_ack flag is	concurrent assert		concurrent assertion to check for the count varaible functionality
always_comb	cuz the rst is asynch. Signal so we must use always comb to chech the variables count and wr_ptr and rd_ptr	immediate assert		immediate assertion to check for the functionality of the var count and the pointers using assert final when the reset signal is asserted
Data_out_ref	to calculate the expected data_out	Directed		using the golden model (ref model) caculated in the scoreboard package

Design bugs:

- **Almostfull flag must be (count == FIFO_DEPTH -1) instead of (count ==FIFO_DEPTH -2)**
- **Underflow signal is a sequential output can't be used in assign statement, must be handle it in always block.**
- **Must handle some cases about the count:**

  1- when wr_en and rd_en are both to high and full is asserted.

2- when wr_en and rd_en are both to high and empty is asserted.
3- When wr_en is high and rd_en is low and full is asserted.
4- When wr_en is low and rd_en is high and empty is asserted.
5- when wr_en and rd_en are both to high and full is deasserted and empty is deasserted.

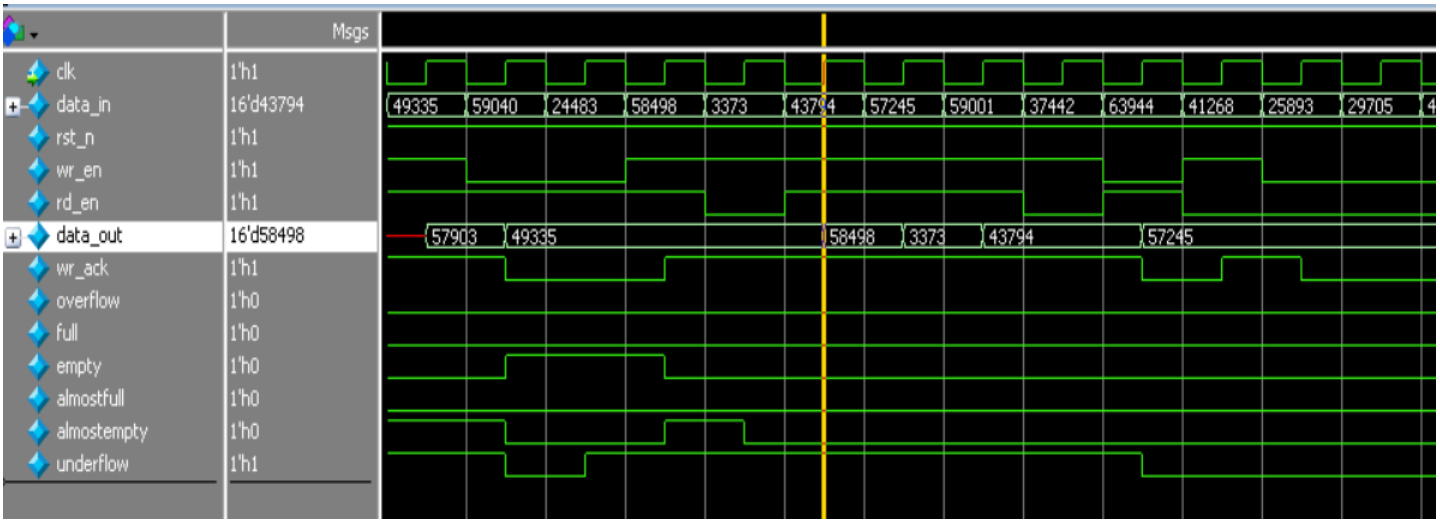
- **If a read and write enables were high and the FIFO was empty, only writing will take place and vice verse if the FIFO was full.**

Do file:

```
FIFO Project > run.do
1   vlib work
2   vlog -f src_files.txt
3   vsim -voptargs=+acc work.FIFO_top -classdebug
4   add wave /FIFO_top/fifo_if/*
5   coverage save FIFO_top.ucdb -onexit
6   run -all
```

```
O Project > src_files.txt
1   FIFO.sv
2   shared_pkg.sv
3   fifo_interface.sv
4   FIFO_transaction.sv
5   FIFO_coverage.sv
6   FIFO_scoreboard.sv
7   FIFO_monitor.sv
8   FIFO_test.sv
9   FIFO_top.sv
```

Questasim snippets:



Core directives:

Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads
/FIFO_top/d1/cover__dec_count	SVA	✓	Off	192	1	Unli...	1	100%		✓	0	0	0 ns	0
/FIFO_top/d1/cover__inc_count_p	SVA	✓	Off	345	1	Unli...	1	100%		✓	0	0	0 ns	0
/FIFO_top/d1/cover__wr_ack_p	SVA	✓	Off	345	1	Unli...	1	100%		✓	0	0	0 ns	0
/FIFO_top/d1/cover__underflow_p	SVA	✓	Off	11	1	Unli...	1	100%		✓	0	0	0 ns	0
/FIFO_top/d1/cover__overflow_p	SVA	✓	Off	337	1	Unli...	1	100%		✓	0	0	0 ns	0
/FIFO_top/d1/cover__almostempty...	SVA	✓	Off	7	1	Unli...	1	100%		✓	0	0	0 ns	0
/FIFO_top/d1/cover__empty_p	SVA	✓	Off	3	1	Unli...	1	100%		✓	0	0	0 ns	0
/FIFO_top/d1/cover__almostfull_p	SVA	✓	Off	35	1	Unli...	1	100%		✓	0	0	0 ns	0
/FIFO_top/d1/cover__full_p	SVA	✓	Off	227	1	Unli...	1	100%		✓	0	0	0 ns	0

Cover groups:

Assertions:

/FIFO_top/d1/assert__full_p	Concurrent	SVA	on	110	1	-	0B	0B	0 ns	0 off
/FIFO_top/d1/assert__almostfull_p	Concurrent	SVA	on	191	1	-	0B	0B	0 ns	0 off
/FIFO_top/d1/assert__empty_p	Concurrent	SVA	on	8	1	-	0B	0B	0 ns	0 off
/FIFO_top/d1/assert__almostempty_p	Concurrent	SVA	on	24	1	-	0B	0B	0 ns	0 off
/FIFO_top/d1/assert__overflow_p	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0 off
/FIFO_top/d1/assert__underflow_p	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0 off
/FIFO_top/d1/assert__wr_ack_p	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0 off
/FIFO_top/d1/assert__inc_count_p	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0 off
/FIFO_top/d1/assert__dec_count	Concurrent	SVA	on	93	1	-	0B	0B	0 ns	0 off
/FIFO_top/d1/co_assert	Immediate	SVA	on	0	1	-	-	-	-	off
/FIFO_top/d1/wr_assert	Immediate	SVA	on	0	1	-	-	-	-	off
/FIFO_top/d1/rd_assert	Immediate	SVA	on	0	1	-	-	-	-	off
/FIFO_top/tb1/#ublk#190103636#18/immed__19	Immediate	SVA	on	0	1	-	-	-	-	off

NOTE: there is an issue about timing between the reference model and the design, leads to unsatisfied result in the code coverage.

Transcript:

```
# Data_out = 51328,ref = 53303
# Error !!,Mismatch between expected and calculated
# Data_out = 9361,ref = 51328
# Error !!,Mismatch between expected and calculated
# Data_out = 9361,ref = 51328
# Error !!,Mismatch between expected and calculated
# Data_out = 9361,ref = 51328
# Error !!,Mismatch between expected and calculated
# Data_out = 9361,ref = 51328
# Error !!,Mismatch between expected and calculated
# Data_out = 41512,ref = 9361
# Error !!,Mismatch between expected and calculated
# Data_out = 41512,ref = 9361
# Error !!,Mismatch between expected and calculated
# Data_out = 41512,ref = 9361
# Error !!,Mismatch between expected and calculated
# Data_out = 11433,ref = 41512
# Error !!,Mismatch between expected and calculated
# Data_out = 11433,ref = 41512
# Error !!,Mismatch between expected and calculated
# Data_out = 11433,ref = 41512
# Error !!,Mismatch between expected and calculated
# Data_out = 11433,ref = 41512
# Error !!,Mismatch between expected and calculated
# Data_out = 34954,ref = 11433
# Error !!,Mismatch between expected and calculated
# Data_out = 34954,ref = 11433
# Error !!,Mismatch between expected and calculated
# Data_out = 34954,ref = 11433
# Error !!,Mismatch between expected and calculated
# Data_out = 34954,ref = 11433
# Error !!,Mismatch between expected and calculated
# Data_out = 34954,ref = 11433
# Error !!,Mismatch between expected and calculated
# Data_out = 34954,ref = 11433
# Test Finished,correct count = 55,Error count = 945
# ** Note: $stop    : FIFO_monitor.sv(52)
#    Time: 2001 ns  Iteration: 1  Instance: /FIFO_top/mon
# Break in Module FIFO_monitor at FIFO_monitor.sv line 52
```

Coverage code report:

```
================================================================================
=== Instance: /FIFO_top/tb1
=== Design Unit: work.FIFO_TEST
================================================================================
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      17        17         0   100.00%

================================Statement Details================================
```

```
================================================================================
== Instance: /FIFO_top/mon
== Design Unit: work.FIFO_monitor
================================================================================
ranch Coverage:
   Enabled Coverage              Bins      Hits    Misses  Coverage
   ----------------              ----      ----    ------  --------
   Branches                         2         2         0   100.00%

================================Branch Details================================
```

```
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                          2         2         0   100.00%

================================Toggle Details================================
```