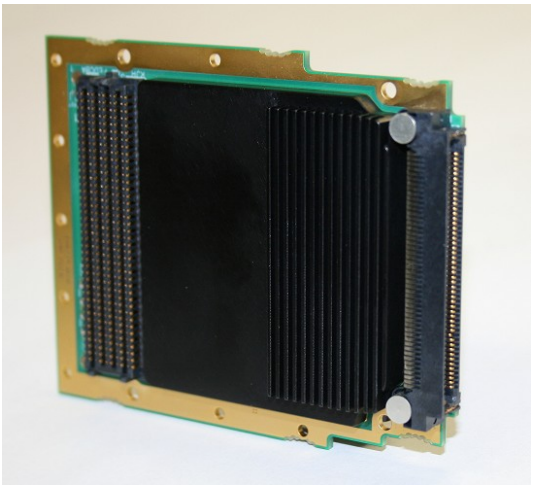
Nutaq® INNOVATION TODAY FOR TOMORROW®

# MI125

## User's Guide



October 2015

## Revision history

| Revision | Date | Comments |
|---|---|---|
| 0.1 | January 2013 | First draft. |
| 0.8 | February 2013 | Ready for revision |
| 0.9 | February 2013 | Linguistic revision |
| 1.0 | February 22nd 2013 | Linguistic revision approved |
| 1.1 | June 5th 2013 | Changed Vadj subsection |
| 1.2 | November 12th 2013 | Added analog bandwidth information |
| 1.3 | May 21st 2014 | Added information related to the new wideband version of the MI125 |
| 1.4 | May 23rd 2014 | Removed a table with specs of the input power of the 12V input of the card – Irrelevant information<br>Release 6.5 |
| 1.5 | November 25th 2014 | Corrected errors in the FMC HPC connector pinout (table 7) |
| 1.6 | October 2015 | New glossary<br>Up to date for Release 7 |

To ensure the accuracy of the information contained herein, particular attention was given to usage in preparing this document. It corresponds to the product version manufactured prior to the date appearing on the title page. There may be differences between the document and the product, if the product was modified after the production of the document.

Nutaq reserves itself the right to make changes and improvements to the product described in this document at any time and without notice.

Version 1.6

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### WARNING

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### FCC WARNING

This equipment is intended for use in a controlled environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of personal computers and peripherals pursuant to subpart J of part 15 of the FCC rules. These rules are designed to provide reasonable protection against radio frequency interference. Operating this equipment in other environments may cause interference with radio communications, in which case the user must, at his/her expense, take whatever measures are required to correct this interference.

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# Table of Contents

# List of Figures and Tables

# 1 Introduction

Congratulations on the purchase of the MI125 FMC.

This document contains all the information necessary to understand and use the MI125. It should be read carefully before using the card and stored in a handy location for future reference.

There are two existing versions of the MI125, the standard version and the wideband version. Throughout the document, everything that relates to both versions will only mention the name MI125. If the wideband version differs from the normal version, specific information will be indicated by the name MI125WB.

## 1.1 Conventions

In a procedure containing several steps, the operations are numbered (1, 2, 3…). The diamond (♦) is used to indicate a procedure containing only one step, or secondary steps. Lowercase letters (a, b, c…) can also be used to indicate secondary steps in a complex procedure.

The abbreviation NC is used to indicate no connection.

Capitals are used to identify any term marked as is on an instrument, such as the names of connectors, buttons, indicator lights, etc. Capitals are also used to identify key names of the computer keyboard.

All terms used in software, such as the names of menus, commands, dialog boxes, text boxes, and options, are presented in bold font style.

The abbreviation N/A is used to indicate something that is not applicable or not available at the time of press.

**Note:**
The screen captures in this document are taken from the software version available at the time of press. For this reason, they may differ slightly from what appears on your screen, depending on the software version that you are using. Furthermore, the screen captures may differ from what appears on your screen if you use different appearance settings.

## 1.2 Glossary

This section presents a list of terms used throughout this document and their definition.

| Term | Definition |
|---|---|
| Advanced Mezzanine Card (AMC) | AdvancedMC is targeted to requirements for the next generation of "carrier grade" communications equipment. This series of specifications are designed to work on any carrier card (primarily AdvancedTCA) but also to plug into a backplane directly as defined by MicroTCA specification. |
| Advanced Telecommunications Computing Architecture (or AdvancedTCA, ATCA) | AdvancedTCA is targeted primarily to requirements for "carrier grade" communications equipment, but has recently expanded its reach into more ruggedized applications geared toward the military/aerospace industries as well. This series of specifications incorporates the latest trends in high speed interconnect technologies, next-generation processors, and improved Reliability, Availability and Serviceability (RAS). |
| Application Programming Interface (API) | An application programming interface is the interface that a computer system, library, or application provides to allow requests for services to be made of it by other computer programs or to allow data to be exchanged between them. |
| Board Software Development Kit (BSDK) | The board software development kit gives users the possibility to quickly become fully functional |

| Term | Definition |
|---|---|
| | developing C/C++ for the host computer and HDL code for the FPGA through an understanding of all Nutaq boards major interfaces. |
| Boards and Systems (BAS) | Refers to the division part of Nutaq which is responsible for the development and maintenance of the hardware and software products related to the different Perseus carriers and their different FMC daughter cards. |
| Carrier | Electronic board on which other boards are connected. In the FMC context, the FMC carrier is the board on which FMC connectors allow a connection between an FMC card and an FPGA. Nutaq has two FMC carriers, the Perseus601x (1 FMC site) and the Perseus611x (2 FMC sites). |
| Central Communication Engine (CCE) | The Central Communication engine (CCE) is an application that executes on a virtual processor called a MicroBlaze in the FPGA of the Perseus products. It handles all the behavior of the Perseus such as module initialization, clock management, as well as other tasks. |
| Chassis | Refers to the rigid framework onto which the CPU board, Nutaq development platforms, and other equipment are mounted. It also supports the shell-like case—the housing that protects all the vital internal equipment from dust, moisture, and tampering. |
| Command Line Interface (CLI) | The Command Line Interface (or CLI) is a basic client interface for Nutaq's FMC carriers. It runs on a host device. It consists of a shell where commands can be typed, interacting with the different computing elements connected to the system. |
| FPGA Mezzanine Card (FMC) | FPGA Mezzanine Card is an ANSI/VITA standard that defines I/O mezzanine modules with connection to an FPGA or other device with re-configurable I/O capability. It specifies a low profile connector and compact board size for compatibility with several industry standard slot card, blade, low profile motherboard, and mezzanine form factors. |
| HDL | Stands for hardware description language. |
| Host | A host is defined as the device that configures and controls a Nutaq board. The host may be a standard computer or an embedded CPU board in the same chassis system where the Nutaq board is installed. You can develop applications on the host for Nutaq boards through the use of an application programming interface (API) that comprises protocols and functions necessary to build software applications. These API are supplied with the Nutaq board. |
| MicroTCA (or μTCA) | The MicroTCA (μTCA) specification is a PICMG Standard which has been devised to provide the requirements for a platform for telecommunications equipment. It has been created for AMC cards. |
| Model-Based Design | Refers to all the Nutaq board-specific tools and software used for development with the boards in MATLAB and Simulink and the Nutaq model-based design kits. |
| Model-Based Development Kit (MBDK) | The model-based development kit gives users the possibility to create FPGA configuration files, or bitstreams, without the need to be fluent in VHDL. By combining Simulink from Matlab, System Generator from Xilinx and Nutaq's tools, someone can quickly create fully-functional FPGA bitstreams for the Perseus platforms. |
| NTP | Network Time Protocol. NTP is a protocol to synchronize the computer time over a network. |
| Peer | A host peer is an associated host running RTDEx on either Linux or Windows.<br>An FPGA peer is an associated FPGA device. |
| PicoDigitizer / PicoSDR Systems | Refers to Nutaq products composed of Perseus AMCs and digitizer or SDR FMCs in a table top format. |
| PPS | Pulse per second. Event to indicate the start of a new second. |
| Reception (Rx) | Any data received by the referent is a reception. |
| Reference Design | Blueprint of an FPGA system implemented on Nutaq boards. It is intended for others to copy and contains the essential elements of a working system (in other words, it is capable of data processing), but third parties may enhance or modify the design as necessary. |
| Transmission (Tx) | Any data transmitted by the referent is a transmission. Abbreviated TX. |
| μDigitizer / μSDR Systems | Any Nutaq system composed of a combination of μTCA or ATCA chassis, Perseus AMCs and digitizer or SDR FMCs. |
| VHDL | Stands for VHSIC hardware description language. |

**Table 1 Glossary**

## 1.3 Technical Support

Nutaq is firmly committed to providing the highest level of customer service and product support. If you experience any difficulties using our products or if it fails to operate as described, first refer to the documentation accompanying the product. If you find yourself still in need of assistance, visit the technical support page in the Support section of our Web site at www.nutaq.com.

# 2 Product Description

The MI125 FPGA mezzanine card (FMC) is a 16/32 channels phased aligned A/D card design around the high-performance LTM9012 QUAD ADC from Linear Technology. The MI125 takes full advantage of the LTM9012 integrated low-noise amplifiers which are suitable for single-ended drive and pulse train signals such as required for imaging applications. Combined with multiple clocks and trigger modes, the MI125 is at its best in DSP applications such as medical/industrial imaging (PET/ultrasound systems), multichannel DAQ, nondestructive testing, radar beamformers, phased array antennas and multichannel pulse detectors (linear accelerators, synchrotron). The MI125 complies with VITA 57.1, a widely used standard in the FPGA-based digital signal processing industry, making it easier for developers to integrate FPGAs into embedded system designs. The MI125 is also completely integrated to the Nutaq µTCA Perseus AMCs, but it can as easily be used on any other FMC carrier on the market. It is compatible with low-pin-count (16 channels) or high-pin-count (32 channels) FMC interfaces.

### Outstanding features

- 16 125-MHz ADC channels with low noise amplifiers
- Selectable clock source from high performance onboard oscillator or external source

### VITA 57.1 FPGA mezzanine card compliant

The MI125 uses the VITA 57.1 standard, widely used in the digital signal processing industry. The FMC is completely Plug and Play with Nutaq's µTCA Perseus AMCs, but the MI125 can as easily be used on any other FMC carrier.

**Note:**
When the MI125 is used in stacked MI125-32 configuration, the FMC mechanical compliance is not respected. The mechanical envelope of the carrier needs to be confirmed.

### MI125 and MI125WB

There are two existing versions of the MI125, the standard version and the wideband version. Throughout the document, everything that relates to both versions will only mention the name MI125. If the wideband version differs from the normal version, specific information will be indicated by the name MI125WB.

The MI125WB only exist in AC-coupled modes, for DC-coupled applications, the standard MI125 should be used.

## 2.1 Hardware Description

This section presents the MI125 hardware from a functional standpoint; introducing its parts and their functions.

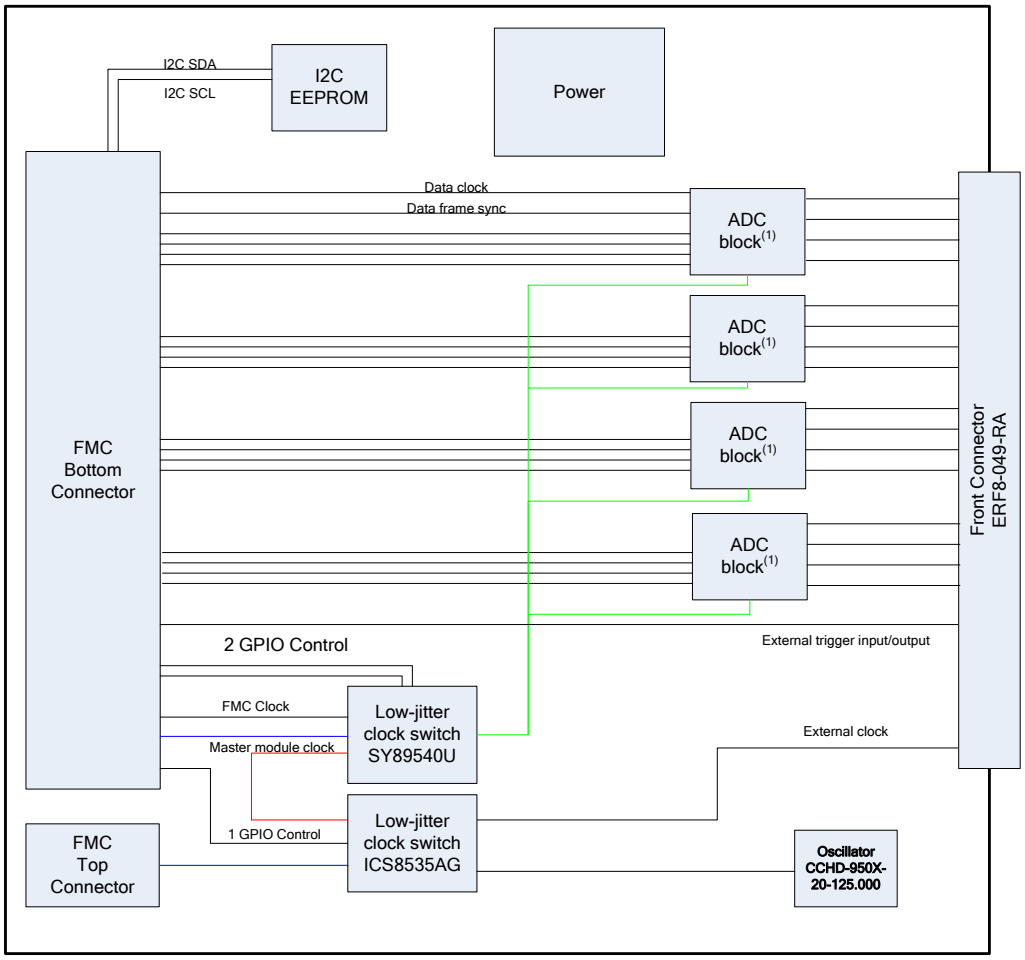


**Figure 2-1 MI125 and MI125WB diagram**

**(1)** Each ADC block handles 4 channels. The ADC block composition differs between the MI125 and the MI125WB. The parts composing the ADC block are, for each model respectively:

MI125:

- 1 LTM9012 – Quad 14-Bit, 125Msps ADC with Integrated Drivers

MI125WB:

- 1 LTC2175 – Quad 14-Bit, Low Power 125Msps ADC
- 4 LTC6409 – 10GHz GBW, Differential Amplifier/ADC Driver
- Passive components

### 2.1.1 MI125-16 and MI125WB-16 Top

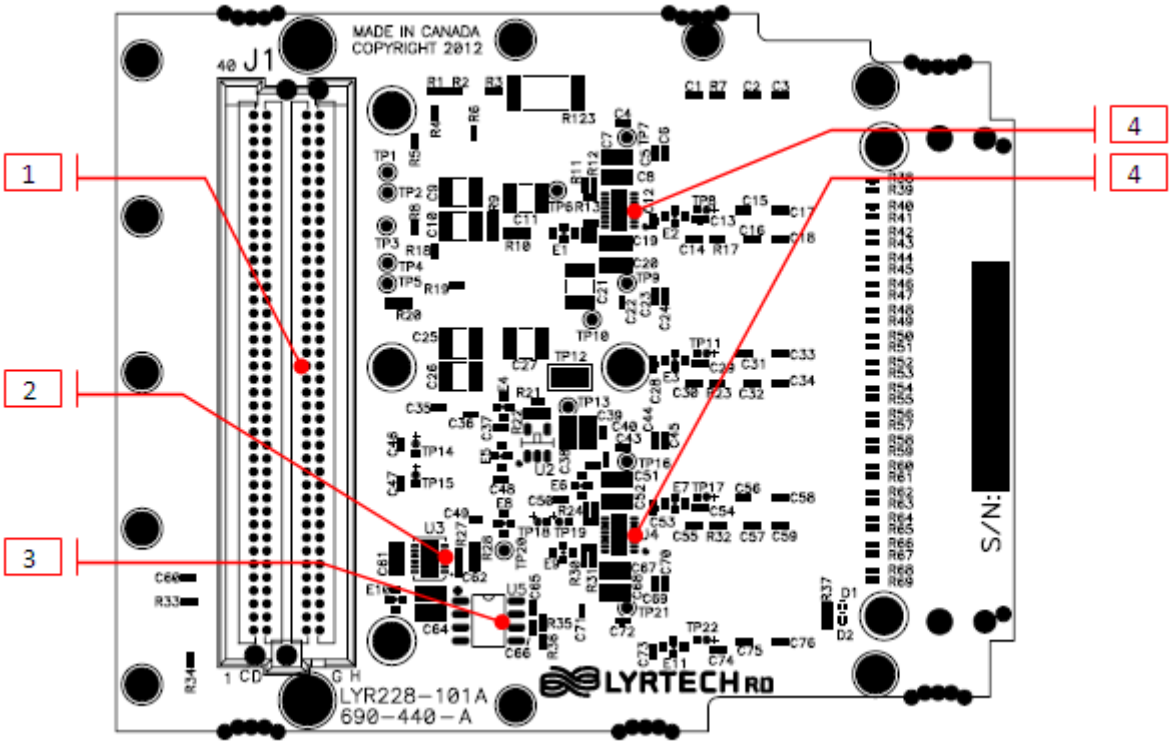


**Figure 2-2 Top view of the MI125-16 and MI125WB hardware**

**1- Expansion FMC connector**

To support 32 channels, the MI125 uses a second low-pin-count connector to route the second channel to the HPC connector of the master FMC. Refer to the "FMC interface" section for details.

**2- Micropower regulator**

The micropower regulator used on the MI125 is an LT1763 from Linear Technology. This is a low-noise, low-dropout regulator capable of supplying 500 mA of output current with a dropout voltage of 300 mV. The LT1763 regulator has a low output noise making it ideal for analog signal acquisition.

**3- $I^2C$ EEPROM**

Every FMC is equipped with a serial $I^2C$ EEPROM to identify itself to its carrier board. The $I^2C$ EEPROM contains information such as the type of hardware, the onboard FPGA, and the interface used. The EEPROM can serve as storage for calibration and user data. A total of 128 Kb are available.

**4- Dual linear regulator**

The dual micropower regulator used on the MI125 is an LT3029 from Linear Technology. This is a low-noise, low-dropout linear regulator. Each channel of the LT3029 can supply up to 500 mA of output current with a dropout voltage of 300 mA.

### 2.1.2 MI125-16 Bottom

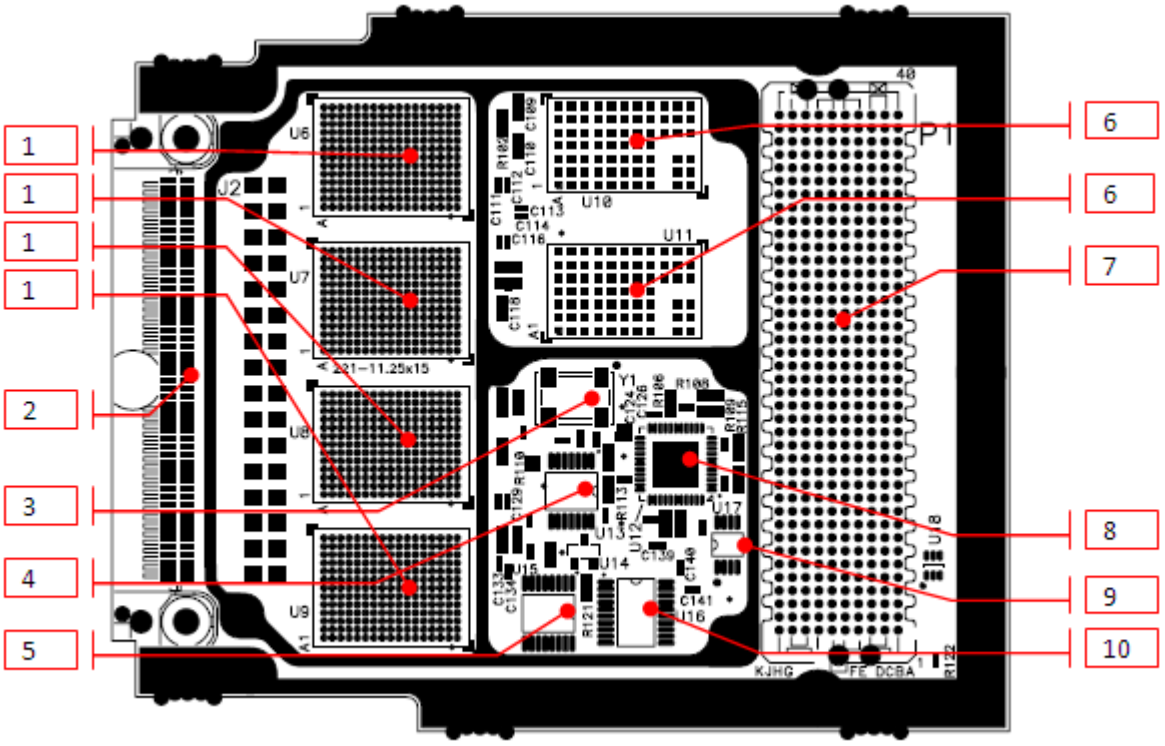


**Figure 2-3 Bottom view of the MI125-16 hardware**

**1- 14-bit 125 MSPS, 4-channel ADC**

The ICs used as ADCs on the MI125 are the LTM9012 Quad 14-bit, 125MSPS ADCs with integrated drivers. To provide 16 input channels, four of these chips are used. These chips feature 4-channel simultaneous sampling ADC with fixed gain. They are low-power chips with excellent SNR and SFDR specifications.

**2- Faceplate connector**

The faceplate connector used is from the ERF8 connector family of Samtec. The exact part number is ERF8-049-01-L-D-RA-L, a rugged high speed socket connector providing a high density of connections to support multiple channels.

**3- Ultralow phase noise oscillator**

The clock oscillator used on the MI125 is a CCHD-575 from Crystek. This is the lowest jitter clock oscillator in such a small package. It has a typical phase jitter of 82 fSec RMS at 100 MHz. It also has an ultra-low phase noise floor at -168 dBc/Hz.

**4- Clock distributor**

The ICS8535 is a low skew, high performance 1 to 2 LVCMOS/LVTTL to 3.3 V LVPECL fanout buffer. It has two single-ended clock inputs. Guaranteed output and part-to-part skew characteristics make the ICS8535 ideal for applications demanding well defined performance and repeatability.

**5- $I^2C$-bus to SPI bridge**

The SC18IS602B serves as an interface between a standard $I^2C$ bus of a microcontroller and a SPI bus. On the MI125, it is used to communicate to the 4 ADCs which use the SPI communication protocol in a transparent way using the available $I^2C$ bus.

**6- Ultralow noise 5 V/2 A DC/DC µModule regulator**

Two LTM8032 µModule regulators present on the MI125 board comply with the EN55022B standard. They have a low profile package, perfect for the limited space of the MI125.

**7- FMC connector**

The MI125 is equipped with an FMC connector used to interface with high-pin-count (HPC) FMCs such as the Nutaq Perseus. The MI125 uses the HPC connector on the MI125-32 and a low-pin-count connector on the MI125-16. The connector uses LA00 to LA34 for channels 1 to 16, and HA00 to HA23 and HB00 to HB09 to communicate with channels 17 to 32 of the MI125-32.

**8- Precision low jitter 4x4 LVDS crosspoint switch**

One of the key part of the clock distribution system on the MI125 is the SY89540U IC. It is a low-jitter, low-skew, high-speed 4x4 crosspoint switch which guarantees data rates of up to 3.2 Gbps over temperature and voltage.

**9- Digital temperature sensor**

The MI125 features an LM75A temperature-to-digital converter using an on-chip band gap temperature sensor and a sigma-delta, A-to-D conversion technique. This device is accessed via the two-wire serial $I^2C$ bus interface.

**10- 8-bit I/O expander for $I^2C$ bus**

A PCF8574A is used to control the different ICs of the MI125 through the $I^2C$ bus.

### 2.1.3 MI125WB-16 Bottom

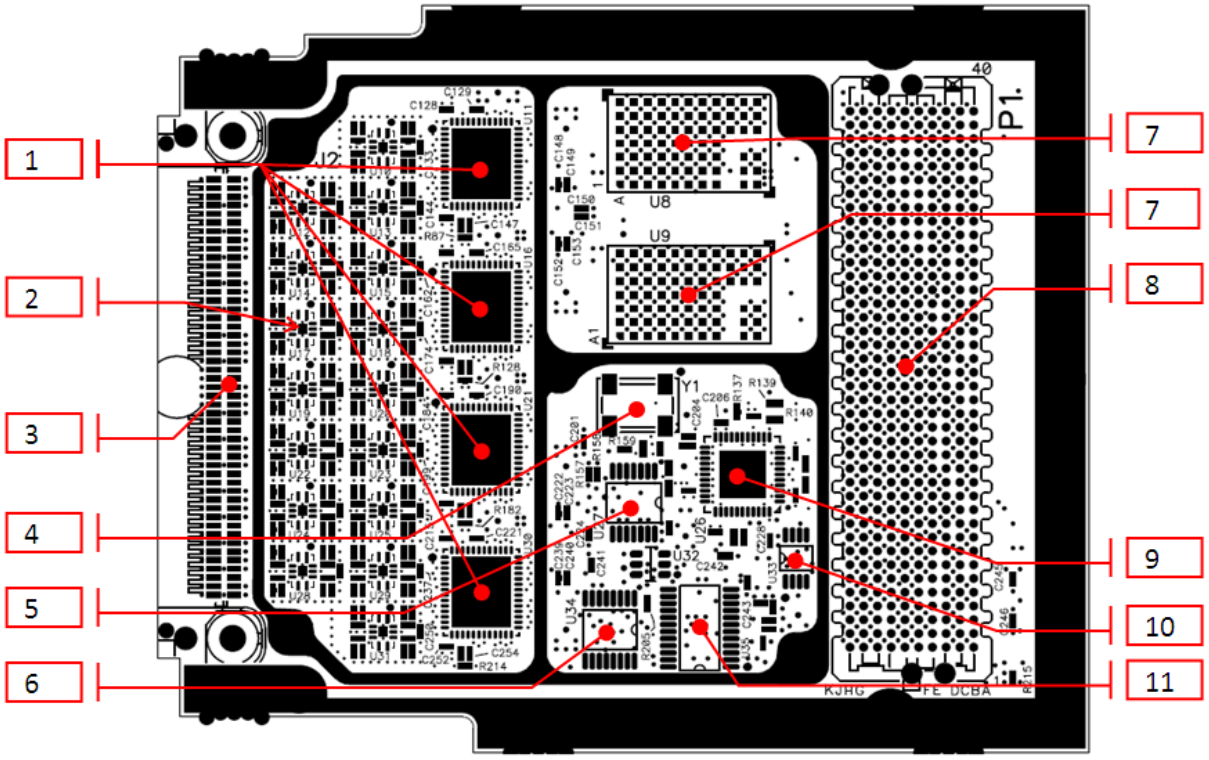


**Figure 2-4 Bottom view of the MI125WB-16 hardware**

**1- 14-bit 125 MSPS, 4-channel ADC**

The ICs used as ADCs on the MI125 are the LTM9012 Quad 14-bit, 125MSPS ADCs with integrated drivers. To provide 16 input channels, four of these chips are used. These chips feature 4-channel simultaneous sampling ADC with fixed gain. They are low-power chips with excellent SNR and SFDR specifications.

**2- Differential amplifiers/ADC drivers**

A series of 16 LTC6409 differential amplifiers/ADC drivers, one for each channel are used in the analog frontend of the MI125WB FMC card. The LTC6409 is a very high speed, low distortion, differential amplifier from Linear Technologies.

**3- Faceplate connector**
The faceplate connector used is from the ERF8 connector family of Samtec. The exact part number is ERF8-049-01-L-D-RA-L, a rugged high speed socket connector providing a high density of connections to support multiple channels.

**4- Ultralow phase noise oscillator**
The clock oscillator used on the MI125 is a CCHD-575 from Crystek. This is the lowest jitter clock oscillator in such a small package. It has a typical phase jitter of 82 fSec RMS at 100 MHz. It also has an ultra-low phase noise floor at -168 dBc/Hz.

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Two LTM8032 µModule regulators present on the MI125 board comply with the EN55022B standard. They have a low profile package, perfect for the limited space of the MI125.

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One of the key part of the clock distribution system on the MI125 is the SY89540U IC. It is a low-jitter, low-skew, high-speed 4x4 crosspoint switch which guarantees data rates of up to 3.2 Gbps over temperature and voltage.

**10- Digital temperature sensor**
The MI125 features an LM75A temperature-to-digital converter using an on-chip band gap temperature sensor and a sigma-delta, A-to-D conversion technique. This device is accessed via the two-wire serial $I^2C$ bus interface.

**11- 8-bit I/O expander for $I^2C$ bus**
A PCF8574A is used to control the different ICs of the MI125 through the $I^2C$ bus.

### 2.1.4 MI125 Front Panel

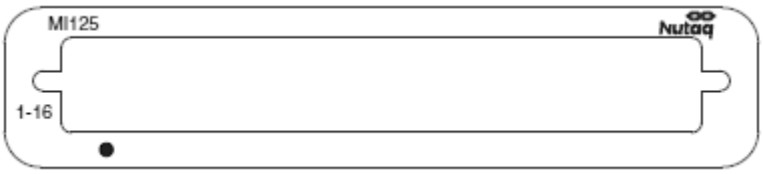


**Figure 2-5 MI125-16 front panel**

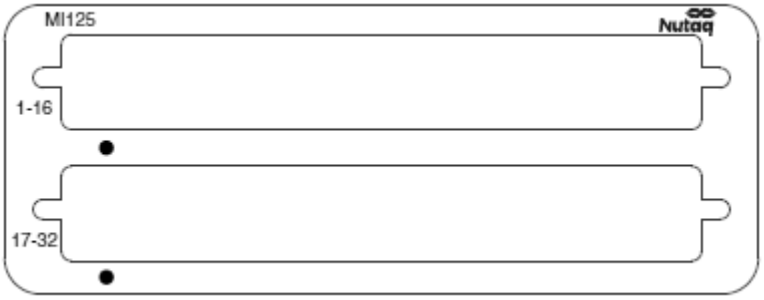


**Figure 2-6 MI125-32 front panel**

### MI125 connector

The front panel of the MI125 is equipped with a single connector from Samtec's ERF8 Series. The exact part number of the connector is ERF8-049-01-L-D-RA-L. You can learn more about the connector on Samtec's Web site by following this link:

http://www.samtec.com/ProductInformation/TechnicalSpecifications/Overview.aspx?series=ERF8

Nutaq offers a custom cable with its MI125 boards. Please contact us for more details about this solution.

**Figure 2-7 MI125 custom breakout cable**

Figure 2-8 presents the pinout of the front panel connector. The first pinout represents the pinout of a MI125 single-ended configuration and the second one represents the pinout of a differential configuration.

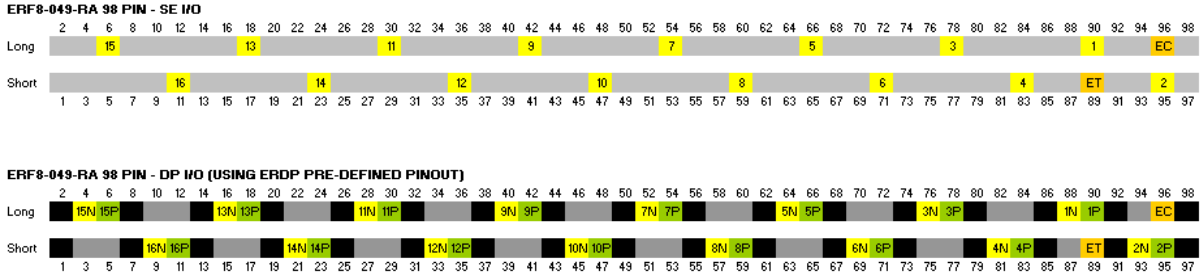


**Figure 2-8 Front panel connector pinout**

#### External clock (EC)

The external clock input connector, EC on the custom breakout cable of the MI125 and has an impedance of 50 Ω. The input signal is LVCMOS 3.3 V and is AC coupled.

For details about the clock selection on the MI125, refer to the "Clock Distribution Circuit" section.

**External trigger (ET)**
The external trigger pin of the front panel connector can be used either as an input or an output. The trigger must be used as a 2.5-V signal.

For details about the external trigger, refer to the "Trigger" section.

**Channels 1 to 16 (single-ended configuration)**
Signals 1 to 16 are connected to the analog signal inputs of the MI125 and have an input impedance of 50 Ω. The characteristics of these signals should respect the configuration of your MI125. With the default configuration, their amplitude should not exceed 2 Vpp.

**Channels 1 to 16 (differential configuration)**
Signals 1 to 16 are connected to the analog signal inputs of the MI125, respectively to the positive and negative signal of each channel input and have an input impedance of 100 Ω. The characteristics of these signals should respect the configuration of your MI125. With the default configuration, their amplitude should not exceed 2 Vpp.

## 2.2 Component Details

### 2.2.1 Clock Distribution Circuit

The user has access to different clock sources to drive the ADCs of the MI125. In addition to the local oscillator clock, the user can select an external clock coming from the front panel connector, an FMC clock coming from the FMC carrier, or a master module clock that comes from the FMC connector and is sourced by the extender board of a two-board stack (32-input system). The clock source switching is performed by the combination of an ICS8535AG and a SY89540UMY.

The following diagram shows the clock distribution scheme in a 32-input system (2-board stack).

**Notes:**

- The red and blue signal paths have the exact same total trace length on the PCB to allow both boards in a MI125-32 system to be sourced by a synchronized clock.
- All 4 green traces have the exact same length to ensure the 4 ADCs are properly synchronized.

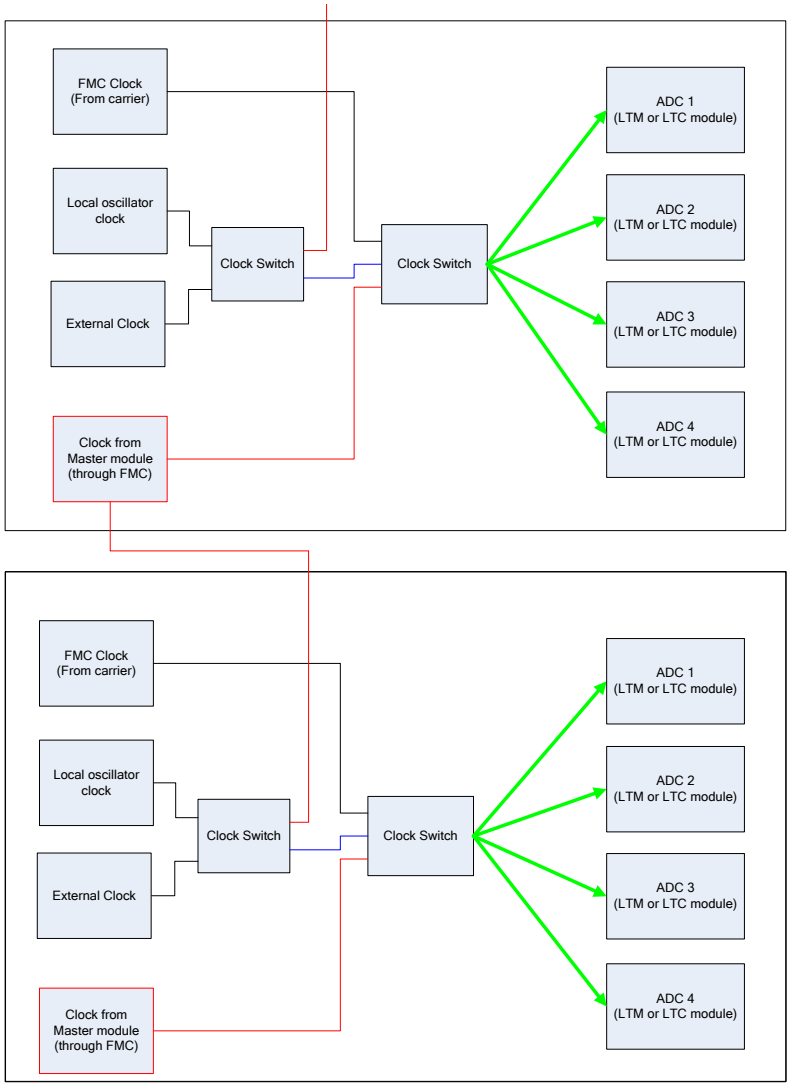


**Figure 2-9 Clock distribution circuit diagram**

### 2.2.2 Trigger

The trigger signal from the front panel point of view can be used either as an input or an output. On the FMC connector though, the trigger input and the trigger output signal are both connected. An analog switch controlled by a signal connected to the I²C GPIO expander of the MI125 connects the trigger output signal to the trigger input signal when a user wants to generate a trigger signal.

**Note:**
Injecting a signal on the External Trigger pin of the front connector of the MI125, when it is configured in trigger output mode, could damage the FMC carrier.

Details on how to set the trigger signal in input or output mode can be found in the *Programmer's Reference Guide MI125*.

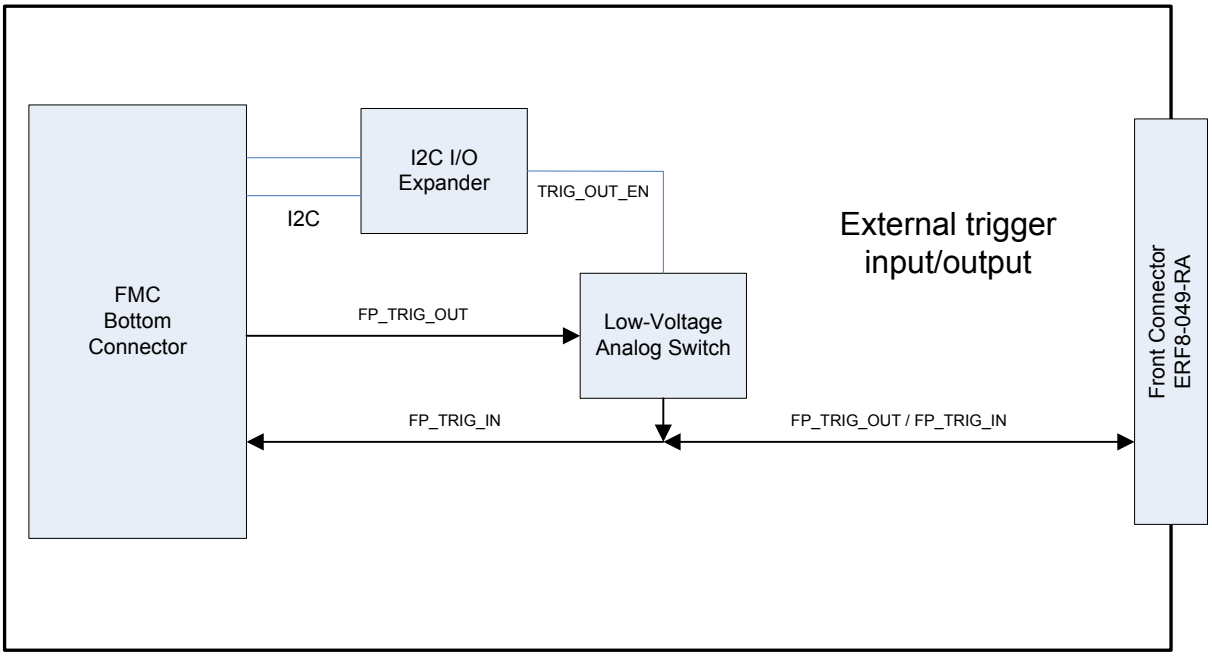


**Figure 2-10 Trigger circuit diagram**

### 2.2.3 I²C Devices

The following is a summary of the devices present on the I²C bus of the MI125 FMC card and their respective addresses.

**MI125-16**

| I²C Device Address | |
|---|---|
| **Device** | **Address** |
| EEPROM | 1010 $0G_0G_1x$ |
| I/O expander | 0100 $0G_0G_1x$ |
| SPI bridge | 0101 $0G_0G_1x$ |
| Temperature sensor | 1001 $0G_0G_1x$ |

**Table 2 MI125-16 I²C device address**

| Geographical Address | | Devices | | | |
|---|---|---|---|---|---|
| GA0 | GA1 | EEPROM | I/O Expander | SPI Bridge | Temperature Sensor |
| 0 | 0 | 0xA0 | 0x40 | 0x50 | 0x90 |
| 0 | 1 | 0xA2 | 0x42 | 0x52 | 0x92 |
| 1 | 0 | 0xA4 | 0x44 | 0x54 | 0x94 |
| 1 | 1 | 0xA6 | 0x46 | 0x56 | 0x96 |

**Table 3 MI125-16 I²C complete address map**

**MI125-16-E**

| I²C Device Address | |
|---|---|
| Device | Address |
| EEPROM | 1010 1G0G1x (0xAx) |
| I/O expander | 0100 1G0G1x (0x4x) |
| SPI bridge | 0101 1G0G1x (0x5x) |
| Temperature sensor | 1001 1G0G1x (0x9x) |

**Table 4 MI125-16-E I²C device address**

| Geographical Address | | Device | | | |
|---|---|---|---|---|---|
| GA0 | GA1 | EEPROM | I/O Expander | SPI Bridge | Temperature Sensor |
| 0 | 0 | 0xA8 | 0x48 | 0x58 | 0x98 |
| 0 | 1 | 0xAA | 0x4A | 0x5A | 0x9A |
| 1 | 0 | 0xAC | 0x4C | 0x5C | 0x9C |
| 1 | 1 | 0xAE | 0x4E | 0x5E | 0x9E |

**Table 5 MI125-16-E I²C complete address map**

### 2.2.4 FMC Connector

The MI125 is designed to function on any carrier with a low-pin-count (LPC) FMC connector. Under the FMC, the MI125 is equipped with a high-pin-count (HPC) connector completely compatible with LPC sockets, but including extra pins, to interface with an FMC carrier. On top of the MI125-E there is also an LPC connector. These two connectors allow cascading a MI125-16 and MI125-16-E (a MI125-16 with an additional connector to cascade another MI125-16), yielding a 32-channel system, which is the equivalent of an MI125-32.

Figure 2-11 illustrates the FMC connections of MI125-32. The HPC connectors are shown as containing LPC pins and HPC pins. The LPC connectors only contain LPC pins.

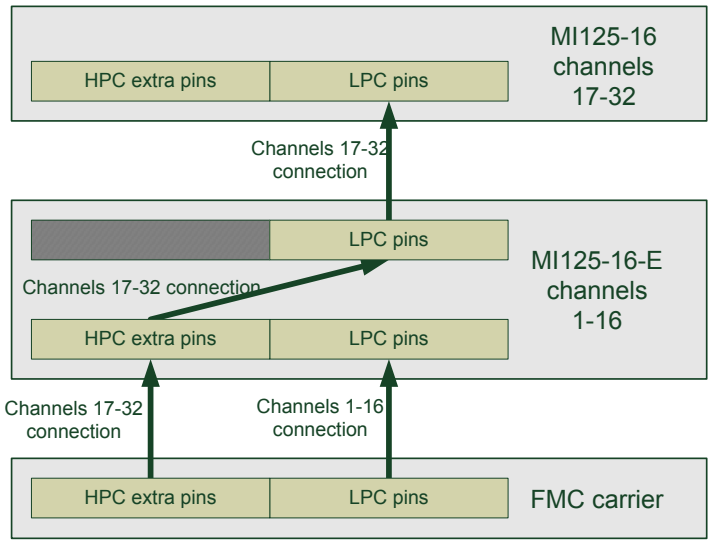


**Figure 2-11 Channels routing in an MI125-32**

The MI125-32 configuration is only possible with carriers supporting HPC FMC connections. In such systems, the LPC pins from the carrier are directly routed to channel 1 to 16 of the MI125-32. The HPC pins from the carrier are routed, through MI125-16-E LPC connection, directly to channels 17 to 32 of the MI125-32.

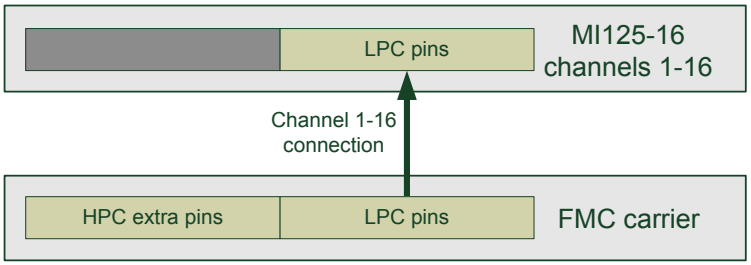


**Figure 2-12 Channels routing in an MI125-16**

**WARNING**
Cascading an MI125-16 with an MI125-16-E to make an MI125-32 is only possible with these two FMCs because HPC connectors do not have enough pins to route more channels.

## 2.2.5 FMC Interface

The MI125 is equipped with a VITA 57.1 FMC high-pin-count connector to interface with FMC carriers such as the Nutaq Perseus. The FMC interface creates a high-bandwidth path between the carrier card and the MI125. A low-pin-count carrier is necessary when using an MI125-16 and a high-pin-count carrier when using a MI125-32.

### $V_{adj}$ setting

The MI125 uses a value of 2,5V for $V_{adj}$.

### FMC connector pin assignment

To function correctly, the FMC carrier connected to the MI125 must have the following connected pins: LA00 to LA33, HA00 to HA23, and HB00 to HB11. The tables below show the MI125 FMC connector pin assignments on the FMC bus. The assignments are divided into two sections: LPC pin assignment (MI125-16) and HPC pin assignment (MI125-32).

**MI125-16 low-pin-count connector**

| LPC Pin | | | |
|---|---|---|---|
| **FMC Pin** | **Pin Name** | **Function** | **Direction (Carrier POV)** |
| G9 | LA03_P | ADC Channel 1 OUTA_N | Input |
| G10 | LA03_N | ADC Channel 1 OUTA_P | Input |
| H7 | LA02_P | ADC Channel 1 OUTB_N | Input |
| H8 | LA02_N | ADC Channel 1 OUTB_P | Input |
| C10 | LA06_P | ADC Channel 2 OUTA_N | Input |
| C11 | LA06_N | ADC Channel 2 OUTA_P | Input |
| H10 | LA04_P | ADC Channel 2 OUTB_N | Input |
| H11 | LA04_N | ADC Channel 2 OUTB_P | Input |
| G12 | LA08_P | ADC Channel 3 OUTA_N | Input |
| G13 | LA08_N | ADC Channel 3 OUTA_P | Input |
| H13 | LA07_P | ADC Channel 3 OUTB_N | Input |
| H14 | LA07_N | ADC Channel 3 OUTB_P | Input |
| D11 | LA05_P | ADC Channel 4 OUTA_N | Input |
| D12 | LA05_N | ADC Channel 4 OUTA_P | Input |
| D14 | LA09_P | ADC Channel 4 OUTB_N | Input |
| D15 | LA09_N | ADC Channel 4 OUTB_P | Input |
| C14 | LA10_P | ADC Channel 5 OUTA_N | Input |
| C15 | LA10_N | ADC Channel 5 OUTA_P | Input |
| D17 | LA13_P | ADC Channel 5 OUTB_N | Input |
| D18 | LA13_N | ADC Channel 5 OUTB_P | Input |
| G15 | LA12_P | ADC Channel 6 OUTA_N | Input |
| G16 | LA12_N | ADC Channel 6 OUTA_P | Input |
| H16 | LA11_P | ADC Channel 6 OUTB_N | Input |
| H17 | LA11_N | ADC Channel 6 OUTB_P | Input |
| G18 | LA16_P | ADC Channel 7 OUTA_N | Input |
| G19 | LA16_N | ADC Channel 7 OUTA_P | Input |
| H19 | LA15_P | ADC Channel 7 OUTB_N | Input |
| H20 | LA15_N | ADC Channel 7 OUTB_P | Input |
| C18 | LA14_P | ADC Channel 8 OUTA_N | Input |
| C19 | LA14_N | ADC Channel 8 OUTA_P | Input |
| D20 | LA17_P_CC | ADC Channel 8 OUTB_N | Input |
| D21 | LA17_N_CC | ADC Channel 8 OUTB_P | Input |
| C22 | LA18_P_CC | ADC Channel 9 OUTA_N | Input |
| C23 | LA18_N_CC | ADC Channel 9 OUTA_P | Input |
| D23 | LA23_P | ADC Channel 9 OUTB_N | Input |
| D24 | LA23_N | ADC Channel 9 OUTB_P | Input |
| G21 | LA20_P | ADC Channel 10 OUTA_N | Input |
| G22 | LA20_N | ADC Channel 10 OUTA_P | Input |
| H22 | LA19_P | ADC Channel 10 OUTB_N | Input |
| H23 | LA19_N | ADC Channel 10 OUTB_P | Input |
| G24 | LA22_P | ADC Channel 11 OUTA_N | Input |
| G25 | LA22_N | ADC Channel 11 OUTA_P | Input |
| H25 | LA21_P | ADC Channel 11 OUTB_N | Input |
| H26 | LA21_N | ADC Channel 11 OUTB_P | Input |

| LPC Pin | | | |
|---|---|---|---|
| **FMC Pin** | **Pin Name** | **Function** | **Direction (Carrier POV)** |
| D26 | LA26_P | ADC Channel 12 OUTA_N | Input |
| D27 | LA26_N | ADC Channel 12 OUTA_P | Input |
| C26 | LA27_P | ADC Channel 12 OUTB_N | Input |
| C27 | LA27_N | ADC Channel 12 OUTB_P | Input |
| G27 | LA25_P | ADC Channel 13 OUTA_N | Input |
| G28 | LA25_N | ADC Channel 13 OUTA_P | Input |
| H28 | LA24_P | ADC Channel 13 OUTB_N | Input |
| H29 | LA24_N | ADC Channel 13 OUTB_P | Input |
| G30 | LA29_P | ADC Channel 14 OUTA_N | Input |
| G31 | LA29_N | ADC Channel 14 OUTA_P | Input |
| H31 | LA28_P | ADC Channel 14 OUTB_N | Input |
| H32 | LA28_N | ADC Channel 14 OUTB_P | Input |
| G36 | LA33_P | ADC Channel 15 OUTA_N | Input |
| G37 | LA33_N | ADC Channel 15 OUTA_P | Input |
| H37 | LA32_P | ADC Channel 15 OUTB_N | Input |
| H38 | LA32_N | ADC Channel 15 OUTB_P | Input |
| G33 | LA31_P | ADC Channel 16 OUTA_N | Input |
| G34 | LA31_N | ADC Channel 16 OUTA_P | Input |
| H34 | LA30_P | ADC Channel 16 OUTB_N | Input |
| H35 | LA30_N | ADC Channel 16 OUTB_P | Input |
| G6 | LA00_P_CC | ADC_1-16_DCO_P | Input |
| G7 | LA00_N_CC | ADC_1-16_DCO_N | Input |
| D8 | LA01_P_CC | ADC_1-16_FR_P | Input |
| D9 | LA01_N_CC | ADC_1-16_FR_N | Input |
| C30 | SCL | FMC_SCL | Output |
| C31 | SDA | FMC_SDA | Input/Output |
| C34 | GA0 | FMC_GA0 | Output |
| D35 | GA1 | FMC_GA1 | Output |

**Table 6 FMC connections to the carrier (LPC)**

### MI125-32 high-pin-count connector

**Note:**

The MI125-32 HPC connector shares all the pins of the LPC connector above. Only the additional HPC pins are described below.

| HPC Pin | | | |
|---|---|---|---|
| **FMC Pin** | **Pin Name** | **Function** | **Direction (Carrier POV)** |
| J9 | HA07_P | ADC Channel 17 OUTA_N | Input |
| J10 | HA07_N | ADC Channel 17 OUTA_P | Input |
| F7 | HA04_P | ADC Channel 17 OUTB_N | Input |
| F8 | HA04_N | ADC Channel 17 OUTB_P | Input |
| E9 | HA09_P | ADC Channel 18 OUTA_N | Input |
| E10 | HA09_N | ADC Channel 18 OUTA_P | Input |
| K10 | HA06_P | ADC Channel 18 OUTB_N | Input |

| HPC Pin | | | |
|---|---|---|---|
| **FMC Pin** | **Pin Name** | **Function** | **Direction (Carrier POV)** |
| K11 | HA06_N | ADC Channel 18 OUTB_P | Input |
| J12 | HA11_P | ADC Channel 19 OUTA_N | Input |
| J13 | HA11_N | ADC Channel 19 OUTA_P | Input |
| K13 | HA10_P | ADC Channel 19 OUTB_N | Input |
| K14 | HA10_N | ADC Channel 19 OUTB_P | Input |
| E12 | HA13_P | ADC Channel 20 OUTA_N | Input |
| E13 | HA13_N | ADC Channel 20 OUTA_P | Input |
| F13 | HA12_P | ADC Channel 20 OUTB_N | Input |
| F14 | HA12_N | ADC Channel 20 OUTB_P | Input |
| E15 | HA16_P | ADC Channel 21 OUTA_N | Input |
| E16 | HA16_N | ADC Channel 21 OUTA_P | Input |
| F16 | HA15_P | ADC Channel 21 OUTB_N | Input |
| F17 | HA15_N | ADC Channel 21 OUTB_P | Input |
| J15 | HA14_P | ADC Channel 22 OUTA_N | Input |
| J16 | HA14_N | ADC Channel 22 OUTA_P | Input |
| K16 | HA17_P_CC | ADC Channel 22 OUTB_N | Input |
| K17 | HA17_N_CC | ADC Channel 22 OUTB_P | Input |
| J18 | HA18_P | ADC Channel 23 OUTA_N | Input |
| J19 | HA18_N | ADC Channel 23 OUTA_P | Input |
| K19 | HA21_P | ADC Channel 23 OUTB_N | Input |
| K20 | HA21_N | ADC Channel 23 OUTB_P | Input |
| E18 | HA20_P | ADC Channel 24 OUTA_N | Input |
| E19 | HA20_N | ADC Channel 24 OUTA_P | Input |
| F19 | HA19_P | ADC Channel 24 OUTB_N | Input |
| F20 | HA19_N | ADC Channel 24 OUTB_P | Input |
| E21 | HB03_P | ADC Channel 25 OUTA_N | Input |
| E22 | HB03_N | ADC Channel 25 OUTA_P | Input |
| F22 | HB02_P | ADC Channel 25 OUTB_N | Input |
| F23 | HB02_N | ADC Channel 25 OUTB_P | Input |
| J21 | HA22_P | ADC Channel 26 OUTA_N | Input |
| J22 | HA22_N | ADC Channel 26 OUTA_P | Input |
| K22 | HA23_P | ADC Channel 26 OUTB_N | Input |
| K23 | HA23_N | ADC Channel 26 OUTB_P | Input |
| J24 | HB01_P | ADC Channel 27 OUTA_N | Input |
| J25 | HB01_N | ADC Channel 27 OUTA_P | Input |
| K25 | HB00_P_CC | ADC Channel 27 OUTB_N | Input |
| K26 | HB00_N_CC | ADC Channel 27 OUTB_P | Input |
| F25 | HB04_P | ADC Channel 28 OUTA_N | Input |
| F26 | HB04_N | ADC Channel 28 OUTA_P | Input |
| E24 | HB05_P | ADC Channel 28 OUTB_N | Input |
| E25 | HB05_N | ADC Channel 28 OUTB_P | Input |
| J27 | HB07_P | ADC Channel 29 OUTA_N | Input |
| J28 | HB07_N | ADC Channel 29 OUTA_P | Input |
| K28 | HB06_P_CC | ADC Channel 29 OUTB_N | Input |
| K29 | HB06_N_CC | ADC Channel 29 OUTB_P | Input |

| HPC Pin | | | |
|---|---|---|---|
| **FMC Pin** | **Pin Name** | **Function** | **Direction (Carrier POV)** |
| E2 | HA01_P_CC | ADC Channel 30 OUTA_N | Input |
| E3 | HA01_N_CC | ADC Channel 30 OUTA_P | Input |
| F10 | HA08_P | ADC Channel 30 OUTB_N | Input |
| F11 | HA08_N | ADC Channel 30 OUTB_P | Input |
| J6 | HA03_P | ADC Channel 31 OUTA_N | Input |
| J7 | HA03_N | ADC Channel 31 OUTA_P | Input |
| E27 | HB09_P | ADC Channel 31 OUTB_N | Input |
| E28 | HB09_N | ADC Channel 31 OUTB_P | Input |
| K7 | HA02_P | ADC Channel 32 OUTA_N | Input |
| K8 | HA02_N | ADC Channel 32 OUTA_P | Input |
| F28 | HB08_P | ADC Channel 32 OUTB_N | Input |
| F29 | HB08_N | ADC Channel 32 OUTB_P | Input |
| F4 | HA00_P_CC | ADC_17-32_DCO_P | Input |
| F5 | HA00_N_CC | ADC_17-32_DCO_N | Input |
| E6 | HA05_P | ADC_17-32_FR_P | Input |
| E7 | HA05_N | ADC_17-32_FR_N | Input |
| J30 | HB11_P | FP_TRIG_OUT | Output |
| K31 | HB10_P | FP_TRIG_IN | Input |

**Table 7 FMC connections to the carrier (HPC)**

# 3 Specifications

This chapter presents the main technical specifications of the MI125 FMC.

**Note:**
The specifications presented here are subject to change without notice.

## 3.1 Mechanical

### 3.1.1 Dimensions

| MI125 Product | Width (mm) | Height (mm) | Depth (mm) |
|---|---|---|---|
| MI125-16 | 69 | 10 | 86[(1)] |
| MI125-16-E | 69 | 15.4 | 86[(1)] |
| MI125-32 | 69 | 20 | 86[(1)] |

**Table 8 MI125 dimensions**

[(1)] A complete description of the board dimensions is presented in Appendix A.

### 3.1.2 Mass

| MI125 Product | Without Shield | With Shield | With the Faceplate |
|---|---|---|---|
| MI125-16 | 0.100 lbs/45.5 g | 0.132 lbs/60.0 g | 0.150 lbs/68.2 g |
| MI125-16-E | 0.106 lbs/48.1 g | 0.138 lbs/62.7 g | N/A |
| MI125-32 | 0.206 lbs/93.6 g | 0.270 lbs/122.7 g | 0.300 lbs/136.4 g |
| MI125WB-16 | 0.092 lbs/41.8 g | 0.124 lbs/56.3 g | 0.142 lbs/64.5 g |
| MI125WB-16-E | 0.098 lbs/44.5 g | 0.130 lbs/59.0 g | N/A |
| MI125WB-32 | 0.190 lbs/86.4 g | 0.254 lbs/115.5 g | 0.284 lbs/129.0 g |

**Table 9 MI125 and MI125WB mass**

### 3.1.3 VITA 57.1 Compliance

The MI125 FMC card respects the physical envelope imposed by the rule 3.18 of the VITA 57.1 standard.

Due to the height of certain components, the shield provided with the MI125 FMC card slightly exceeds this envelop by 0.8 mm over region 2.

To be able to fix the front connector securely to the PCB, a small extension has been added to the PCB; a band of 2.30 mm mainly running under the connector. This small extension explains the 86-mm depth of the card instead of the 84 mm from the standard.

A complete description of the board compliance and exceptions is presented in Appendix B: MI125 VITA Compliance.

# 3.2 Electrical

## 3.2.1 Power Consumption

The following is a summary of the power consumption of a MI125-16 board with the following setup:

- ADC output terminations set to ON
- ADC LVDS drive set to 2.5 mA

| Number of Active Channels | Current (A) | Power Usage (W) |
|---|---|---|
| 4 | 0.270 | 3.240 |
| 8 | 0.416 | 4.992 |
| 12 | 0.570 | 6.840 |
| 16 | 0.732 | 8.784 |

**Table 10 MI125-16 power consumption**

**Notes:**

- Current is measured on the 12-V rail directly using an FMC adapter.
- Current is measured on a Perseus carrier with an FPGA bit file loaded and all MI125 digital ADC lines calibrated.
- When inactive, channels are put in software sleep mode and hardware shutdown.
- These values apply to the MI125-16, for values applicable to a MI125-32 double-stack, add the current consumption for each MI125-16 configuration.

## 3.2.2 VITA 57.1 Compliance

The MI125-16 FMC card respects the power supply requirements imposed by the rule 5.10 of the VITA 57.1 standard. This rule sets the value for the maximum current an FMC card can use on the 12-V supply of the LPC connector to 1 A.

An MI125-32 stack violates this same rule since it can use up to 1.46 A on the 12-V supply of the HPC connector.

## 3.3 Onboard Oscillator

The specifications of the onboard clock on the MI125 are the following:

| Specification | Value |
|---|---|
| Frequency | 125 MHz |
| Phase-jitter (12 kHz-80 MHz) | 82 fSec RMS typical (100 MHz) |
| Phase-noise floor | -168 dBc/Hz typical<br>-165 dBc/Hz maximum |

**Table 11 Onboard oscillator specifications**

## 3.4 Acquisition

| Specification | Minimum | Typical | Maximum |
|---|---|---|---|
| Input channels | - | 16 | - |
| Resolution | - | 14 signed bits | - |
| Sampling rate | 50 MHz [(1)] | - | 125 MHz |
| Input channel impedance | - | 50 ohms | - |

**Table 12 Analog front-end specifications**

[(1)] Minimum tested sampling frequency was 50 MHz.

| Mode | Input | Power | Voltage |
|---|---|---|---|
| Single-ended | 1 MHz | 10 dBm | 2000 mVpp |
| | 30 MHz | 10 dBm | 2000 mVpp |
| | 70 MHz | 10 dBm | 2000 mVpp |

**Table 13 Full-scale input levels**

## 3.5 External Clock Input

| Specification | Minimum | Typical | Maximum |
|---|---|---|---|
| Input impedance | - | 50 ohms | - |
| Input voltage | - | 3.3 | - |
| AC coupling | | | |
| Frequency | 50 MHz[(1)] | | 125 MHz |

**Table 14 External clock input specifications**

[(1)] Minimum tested sampling frequency was 50 MHz.

## 3.6 External Trigger

| Specification | Minimum | Typical | Maximum |
|---|---|---|---|
| Input high voltage | - | 2.5 | - |

**Table 15 Trigger input specifications**

| Specification | Minimum | Typical | Maximum |
|---|---|---|---|

| | | | |
|---|---|---|---|
| Output high voltage | - | 2.5 | - |

**Table 16 Trigger output specifications**

## 3.7 Analog Performances

The results in the following tables and graphs were obtained using a 65-k-point FFT. Channel crosstalk is obtained by applying an FFT on the signal of the target channel while the first channel receives an input at -1 dBFS. All the measurements were made using the onboard 125-MHz oscillator as a source for the sampling frequency.

### 3.7.1 MI125 AC-Coupled Single-Ended Performances

| Parameter | Input Frequency | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| SNR | 1 MHz | 65 | 66.8 | 68.0 | dB |
| | 30 MHz | 64 | 66.1 | 66.7 | dB |
| | 70 MHz | 62 | 64.6 | 65.4 | dB |
| SFDR | 1 MHz | 69 | 70.0 | 71.3 | dB |
| | 30 MHz | 69 | 74.1 | 79.3 | dB |
| | 70 MHz | 66 | 75.1 | 80.8 | dB |
| THD | 1 MHz | 68 | 69.0 | 69.6 | dB |
| | 30 MHz | 80 | 83.8 | 83.8 | dB |
| | 70 MHz | 76 | 80.0 | 82.3 | dB |
| Crosstalk, near channel (adjacent channels on the same ADC) | 30 MHz | - | 64 | - | dB |
| Crosstalk, far channel (channel 1 with channel 16) | 30 MHz | - | 86 | - | dB |
| Analog Bandwidth (-3dB) | - | - | 90 | - | MHz |

**Table 17 MI125 AC-coupled single-ended analog performances**

### 3.7.2 MI125WB AC-Coupled Single-Ended Performances

| Parameter | Input Frequency | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| SNR | 48 MHz | 61.5 | 62.4 | - | dB |
| | 76 MHz | 60.7 | 61.5 | - | dB |
| | 157 MHz | 57.7 | 59.3 | - | dB |
| | 199 MHz | 55.7 | 58.0 | - | dB |
| SFDR | 48 MHz | - | -71.5 | - | dB |
| | 76 MHz | - | -71.8 | - | dB |
| | 157 MHz | - | -64.1 | - | dB |
| | 199 MHz | - | -51.4 | - | dB |
| THD | 48 MHz | - | -70.9 | - | dB |
| | 76 MHz | - | -70.7 | - | dB |
| | 157 MHz | - | -58.9 | - | dB |
| | 199 MHz | - | -46.7 | - | dB |
| IMD @ 48MHz +/- | 2F1 - F2 Power | - | 67,6 | - | dB |

| Parameter | Input Frequency | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| 500kHz | 2F1 + F2 Power | - | -69,2 | - | dB |
| | 2F2 - F1 Power | - | -63,0 | - | dB |
| | 2F2 + F1 Power | - | -69,3 | - | dB |
| IMD @ 157MHz +/- 500kHz | 2F1 - F2 Power | - | 58,4 | - | dB |
| | 2F1 + F2 Power | - | -64,0 | - | dB |
| | 2F2 - F1 Power | - | -58,6 | - | dB |
| | 2F2 + F1 Power | - | -64,1 | - | dB |
| Crosstalk, near channel (adjacent channels on the | 48 MHz | - | 66.9 | - | dB |
| | 199 MHz | - | 56.6 | - | dB |
| Crosstalk, far channel (channel 1 with channel 16) | 48 MHz | - | 85.1 | - | dB |
| | 199 MHz | - | 73.3 | - | dB |
| Analog Bandwidth (-3dB) | - | - | 250 | - | MHz |

**Table 18 MI125WB AC-coupled single-ended analog performances**

### 3.7.3 DC-Coupled Single-Ended Performances

| Parameter | Input Frequency | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| SNR | 1 MHz | 65 | 66.9 | 68.0 | dBFS |
| | 30 MHz | 64 | 66.1 | 66.7 | dBFS |
| | 70 MHz | 62 | 64.2 | 65.4 | dBFS |
| SFDR | 1 MHz | 69 | 70.4 | 71.3 | dBFS |
| | 30 MHz | 69 | 74.6 | 79.3 | dBFS |
| | 70 MHz | 66 | 72.6 | 80.8 | dBFS |
| THD | 1 MHz | 68 | 69.0 | 69.6 | dBFS |
| | 30 MHz | 80 | 82.5 | 83.8 | dBFS |
| | 70 MHz | 76 | 73.8 | 82.3 | dBFS |
| Crosstalk, near channel (adjacent channels on the same ADC) | 30 MHz | - | 64 | | dBFS |
| Crosstalk, far channel (channel 1 with channel 16) | 30 MHz | - | 86 | - | dBFS |
| Analog Bandwidth (-3dB) | - | - | 90 | - | MHz |

**Table 19 DC-coupled single-ended analog performances**

### 3.7.4 FFT Plots

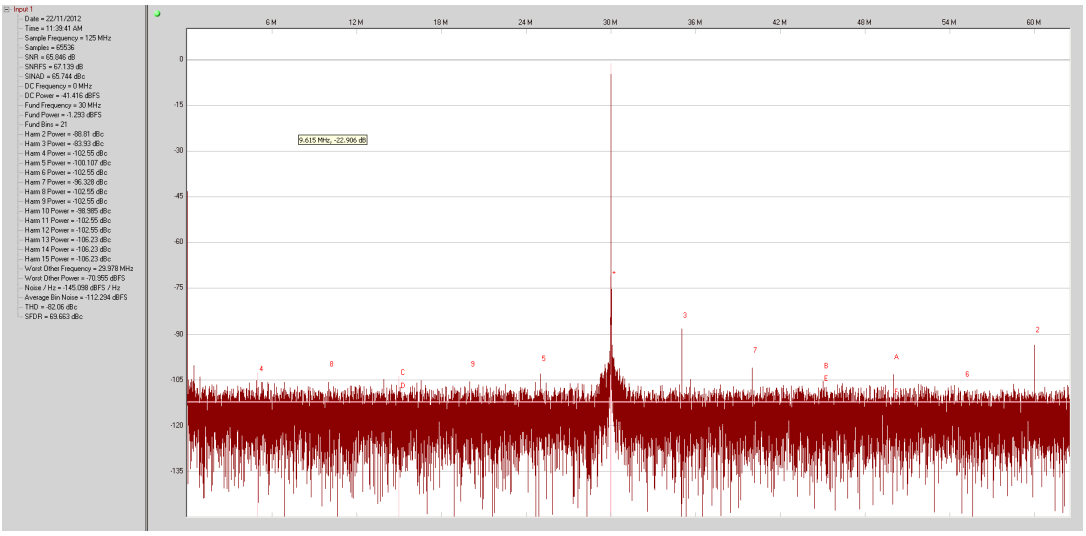


**Figure 3-1 125-MHz internal clock - 30-MHz input signal**

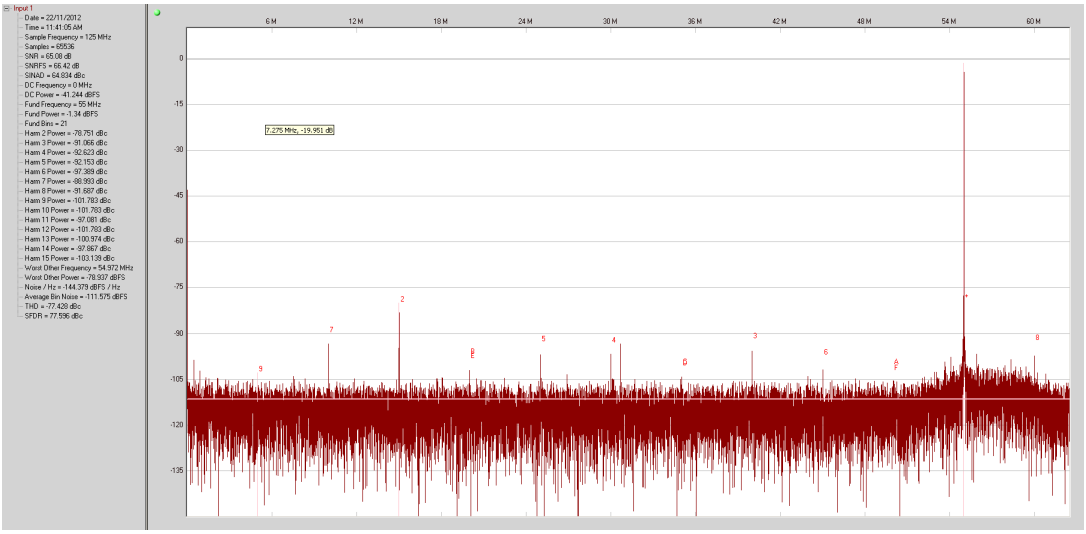


**Figure 3-2 125-MHz internal clock - 70-MHz input signal**

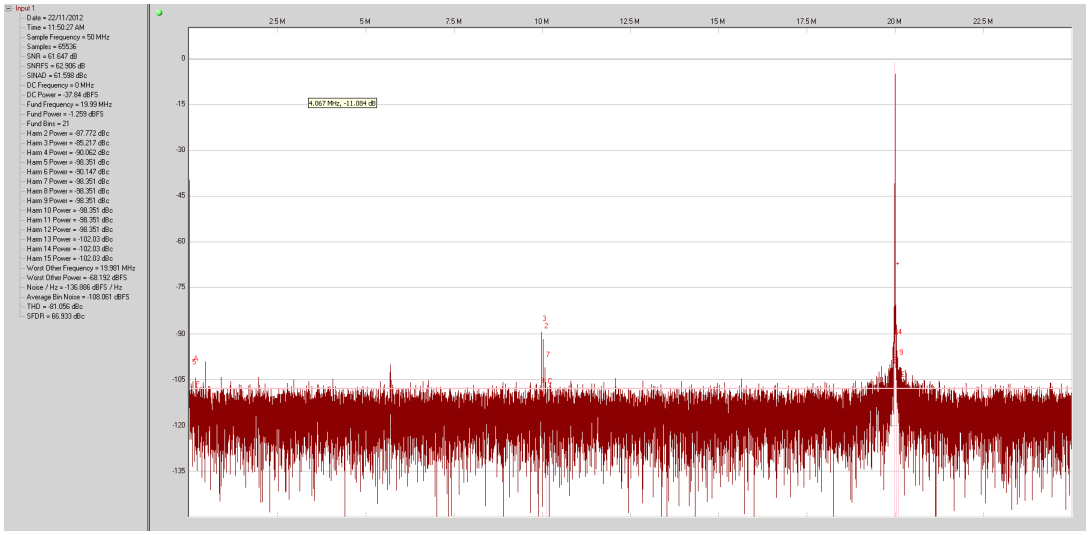


**Figure 3-3 50-MHz external clock - 30-MHz input signal**

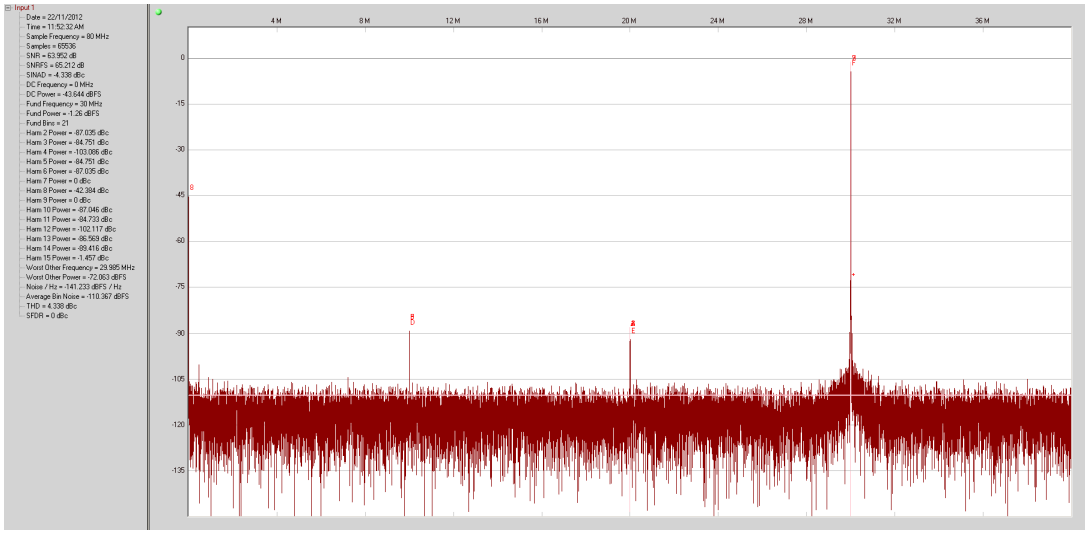


**Figure 3-4 80-MHz external clock - 30-MHz input signal**

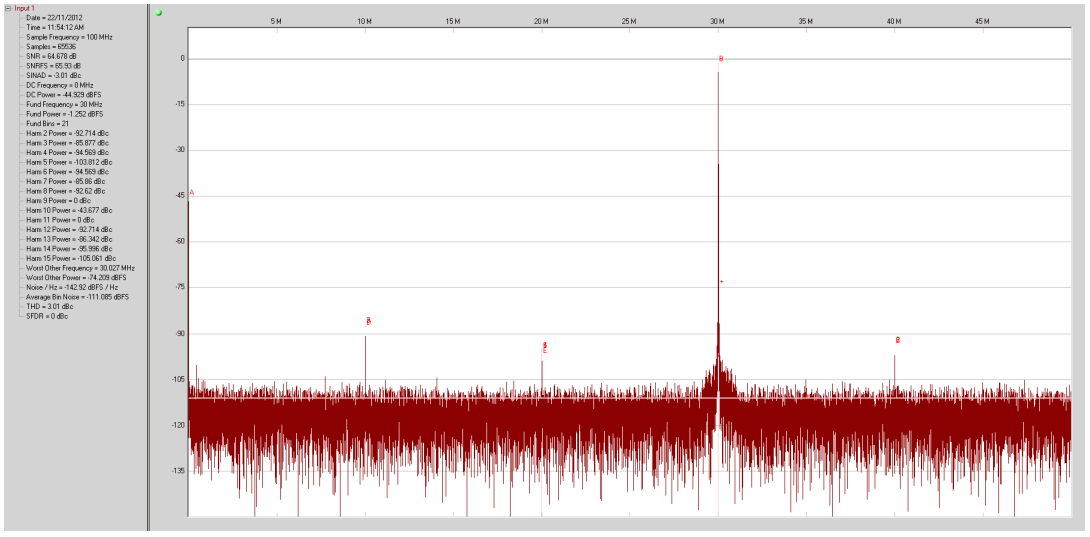


**Figure 3-5 100-MHz external clock - 30-MHz input signal**

### 3.7.5 Analog Bandwidth

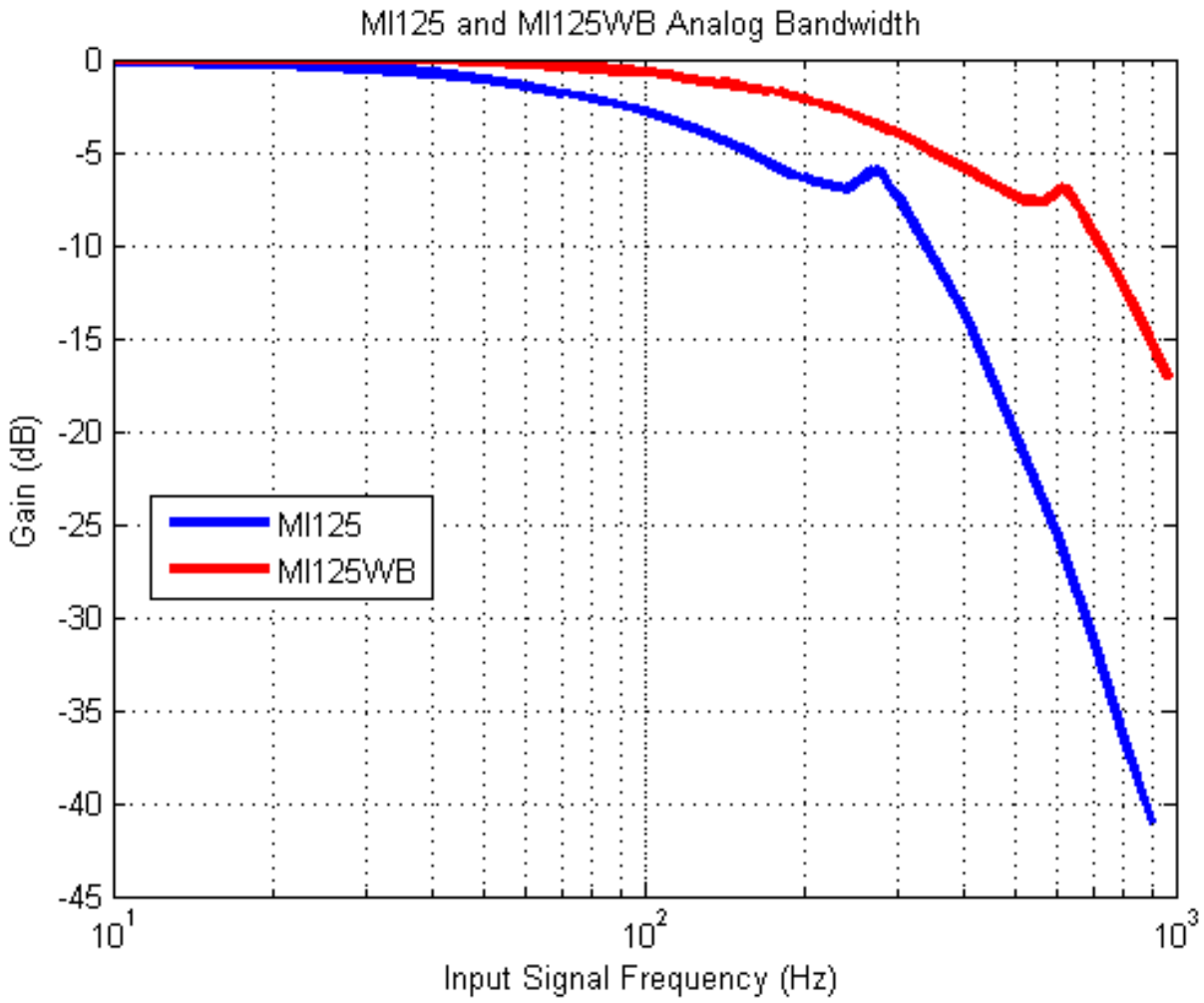


**Figure 3-6 MI125 and MI125WB Analog Bandwidth**

# 4 MI125 Board Dimensions

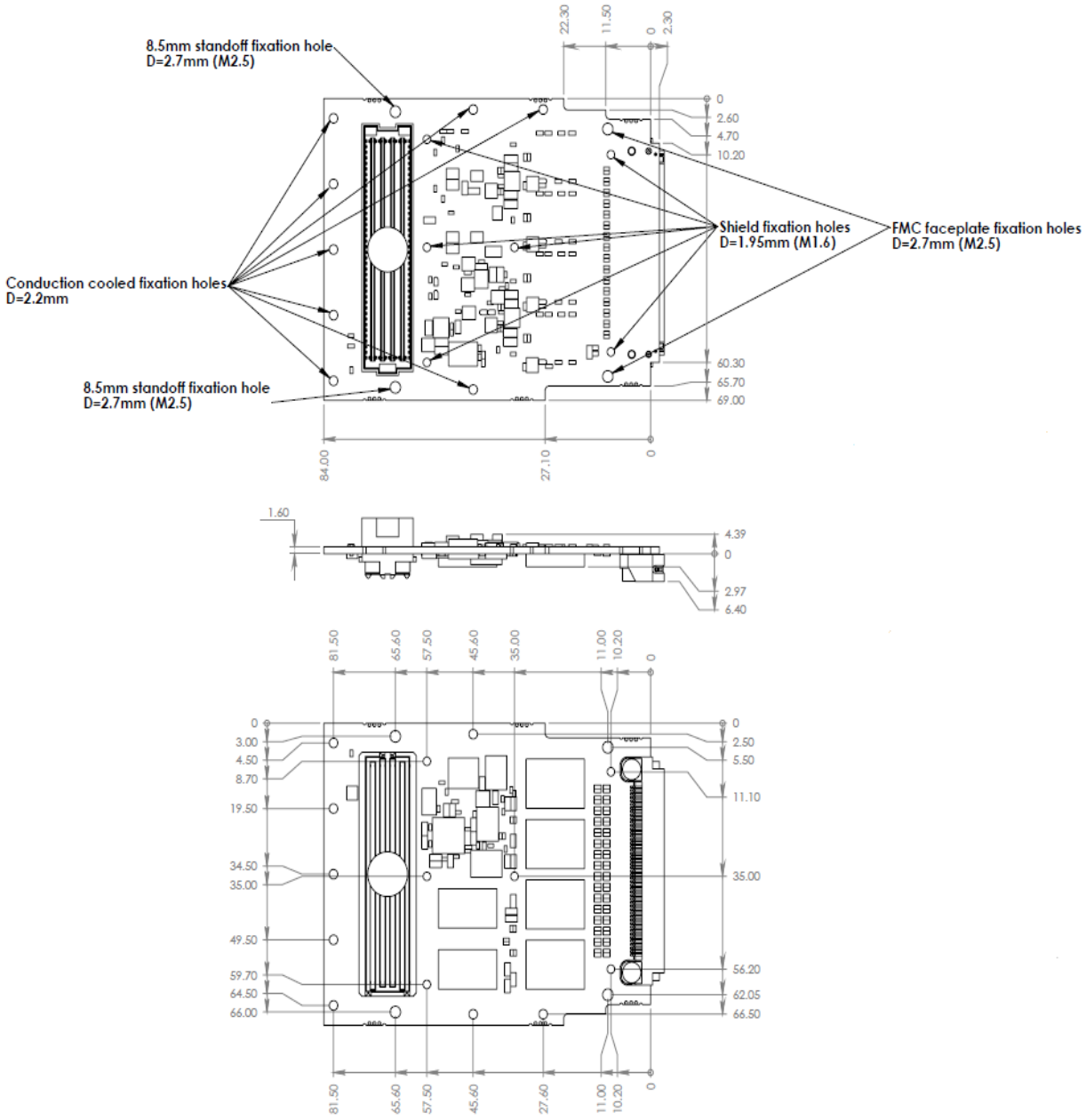


**Figure 4-1 MI125 board dimensions**

# 5 MI125 Mechanical Compliance to VITA57.1

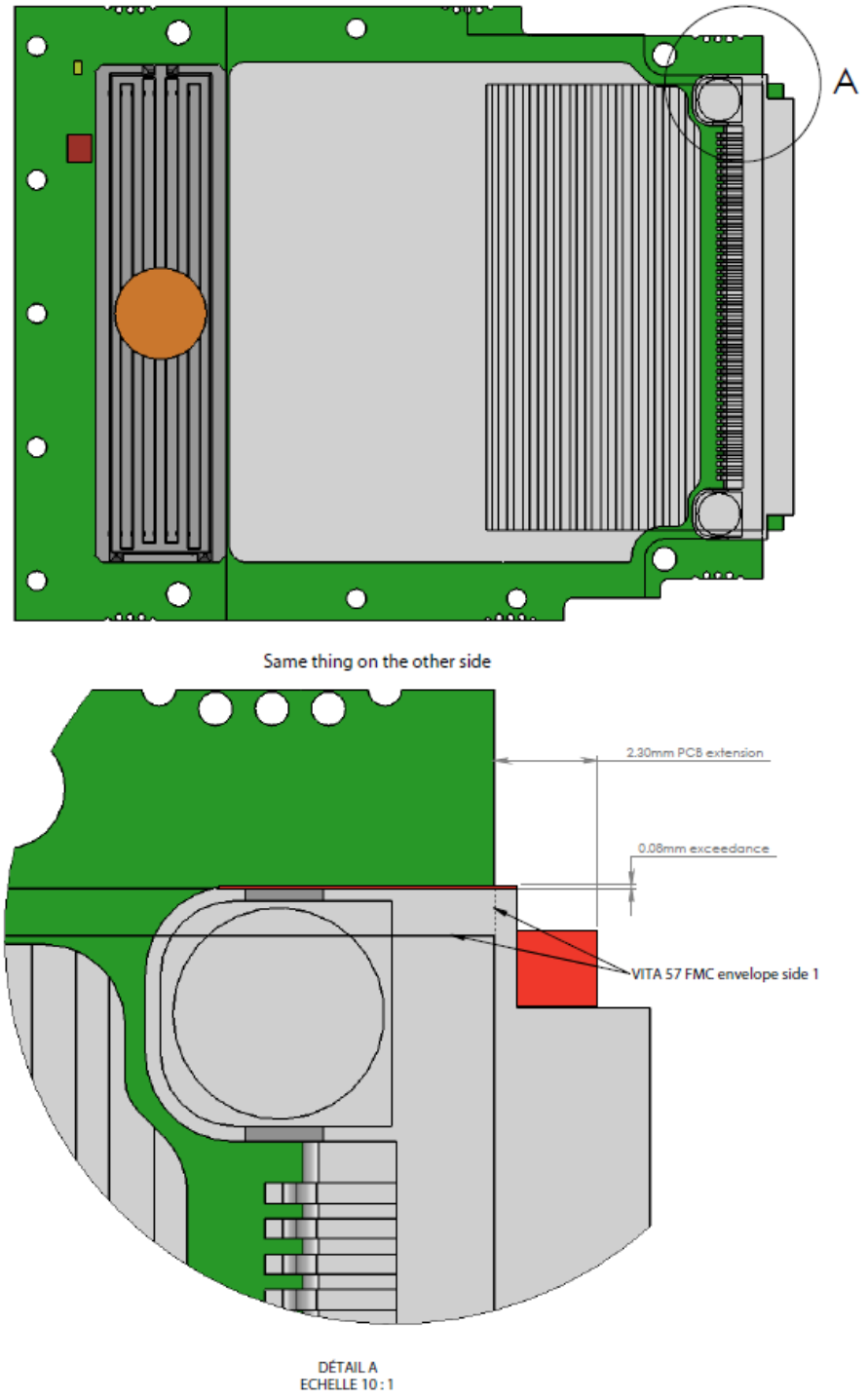


**Figure 5-1 MI125 PCB addition for the connector**

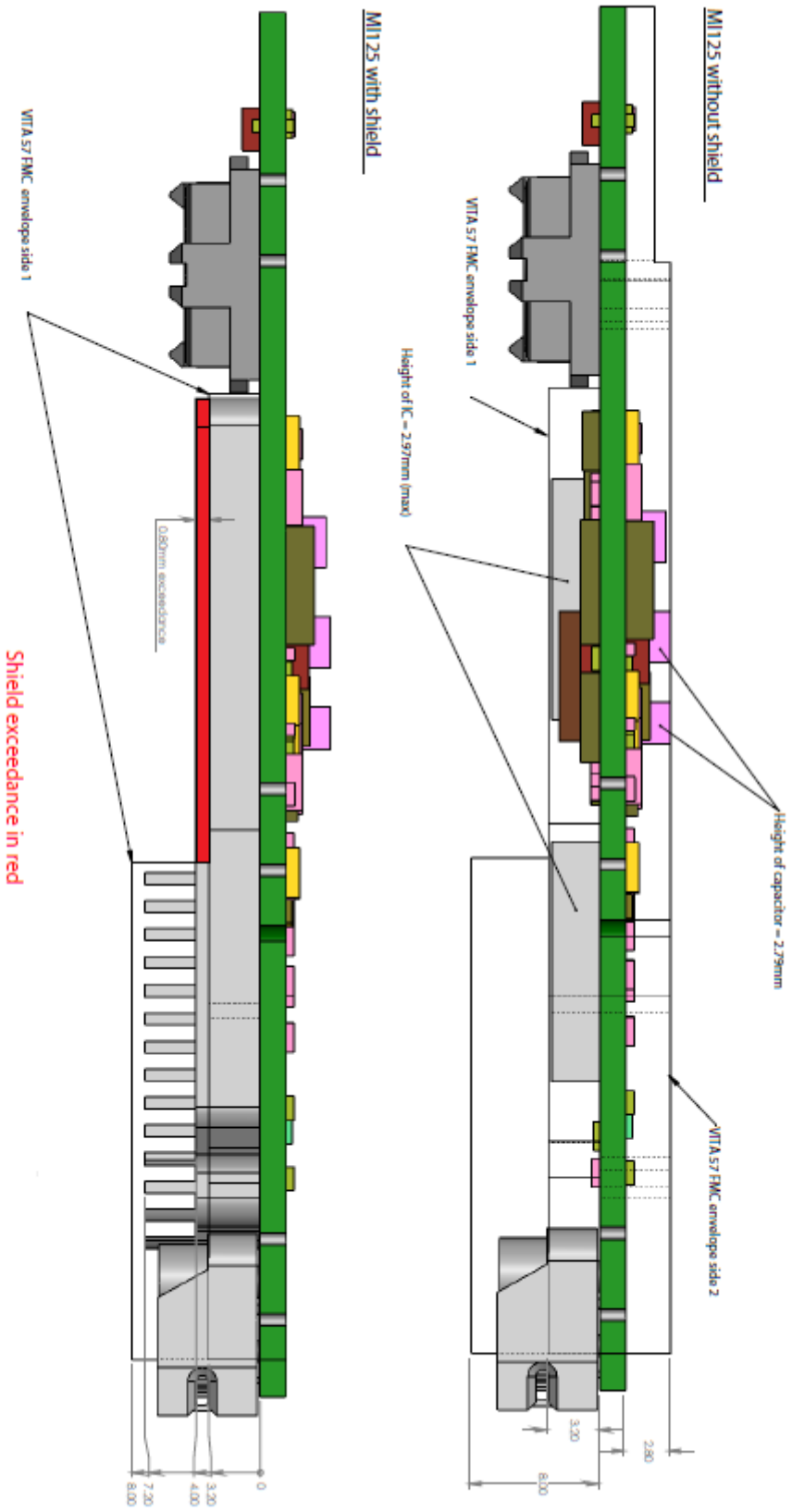


**Figure 5-2 MI125 envelope compliance to VITA 57.1**