Nutaq® INNOVATION TODAY FOR TOMORROW®

Perseus 611X

January 2016

Revision history

Revision	Date	Comments
1.0	October 2015	First release of the document
1.1	January 2016	Added Pins HB18 to HB21 in FPGA pin description table for both FMC sites (sections 2.5.1 and 2.5.2)

To ensure the accuracy of the information contained herein, particular attention was given to usage in preparing this document. It corresponds to the product version manufactured prior to the date appearing on the title page. There may be differences between the document and the product, if the product was modified after the production of the document.

Nutaq reserves itself the right to make changes and improvements to the product described in this document at any time and without notice.

Trademarks

Acrobat, Adobe, and Reader are either registered trademarks or trademarks of Adobe Systems Incorporated in the United States and/or other countries. IBM is a registered trademark of International Business Machines Corporation in the United States, other countries, or both. Intel and Pentium are registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries. Microsoft, MS-DOS, Windows, Windows NT, and the Windows logo are either registered trademarks or trademarks of Microsoft Corporation in the United States and/or other countries. MATLAB, Simulink, and Real-Time Workshop are registered trademarks of The MathWorks, Inc. Xilinx, Spartan, and Virtex are registered trademarks of Xilinx, Inc. Texas Instruments, Code Composer Studio, C62x, C64x, and C67x are trademarks of Texas Instruments Incorporated. All other product names are trademarks or registered trademarks of their respective holders.

The ™ and ® marks have been omitted from the text.

WARNING

Do not use Nutaq products in conjunction with life-monitoring or life-critical equipment. Failure to observe this warning relieves Nutaq of any and all responsibility.

FCC WARNING

This equipment is intended for use in a controlled environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of personal computers and peripherals pursuant to subpart J of part 15 of the FCC rules. These rules are designed to provide reasonable protection against radio frequency interference. Operating this equipment in other environments may cause interference with radio

communications, in which case the user must, at his/her expense, take whatever measures are required to correct this interference.

This page was left intentionally blank.

Table of Contents

List of Figures and Tables

1 Introduction

Congratulations on the purchase of the Perseus611X.

This document contains all the information necessary to understand and use the Perseus611X. It should be read carefully before using the card and stored in a handy location for future reference.

1.1 Conventions

In a procedure containing several steps, the operations are numbered (1, 2, 3…). The diamond (♦) is used to indicate a procedure containing only one step, or secondary steps. Lowercase letters (a, b, c…) can also be used to indicate secondary steps in a complex procedure.

The abbreviation NC is used to indicate no connection.

Capitals are used to identify any term marked as is on an instrument, such as the names of connectors, buttons, indicator lights, etc. Capitals are also used to identify key names of the computer keyboard.

All terms used in software, such as the names of menus, commands, dialog boxes, text boxes, and options, are presented in bold font style.

The abbreviation N/A is used to indicate something that is not applicable or not available at the time of press.

Note:
The screen captures in this document are taken from the software version available at the time of press. For this reason, they may differ slightly from what appears on your screen, depending on the software version that you are using. Furthermore, the screen captures may differ from what appears on your screen if you use different appearance settings.

1.2 Glossary

This section presents a list of terms used throughout this document and their definition.

Term	Definition
Advanced Mezzanine Card (AMC)	AdvancedMC is targeted to requirements for the next generation of "carrier grade" communications equipment. This series of specifications are designed to work on any carrier card (primarily AdvancedTCA) but also to plug into a backplane directly as defined by MicroTCA specification.
Advanced Telecommunications Computing Architecture (or AdvancedTCA, ATCA)	AdvancedTCA is targeted primarily to requirements for "carrier grade" communications equipment, but has recently expanded its reach into more ruggedized applications geared toward the military/aerospace industries as well. This series of specifications incorporates the latest trends in high speed interconnect technologies, next-generation processors, and improved Reliability, Availability and Serviceability (RAS).
Application Programming Interface (API)	An application programming interface is the interface that a computer system, library, or application provides to allow requests for services to be made of it by other computer programs or to allow data to be exchanged between them.
Board Software Development Kit (BSDK)	The board software development kit gives users the possibility to quickly become fully functional developing C/C++ for the host computer and HDL code for the FPGA through an understanding of all Nutaq boards major interfaces.
Boards and Systems (BAS)	Refers to the division part of Nutaq which is responsible for the development and maintenance of the hardware and software products related to the different Perseus carriers and their different FMC daughter cards.
Carrier	Electronic board on which other boards are connected. In the FMC context, the FMC carrier is the board on which FMC connectors allow a connection between an FMC card and an FPGA. Nutaq has two FMC carriers, the Perseus601x (1 FMC site) and the Perseus611x (2 FMC sites).
Central Communication Engine (CCE)	The Central Communication engine (CCE) is an application that executes on a virtual processor called a MicroBlaze in the FPGA of the Perseus products. It handles all the behavior of the Perseus such as module initialization, clock management, as well as other tasks.
Chassis	Refers to the rigid framework onto which the CPU board, Nutaq development platforms, and other equipment are mounted. It also supports the shell-like case—the housing that protects all the vital internal equipment from dust, moisture, and tampering.
Command Line Interface (CLI)	The Command Line Interface (or CLI) is a basic client interface for Nutaq's FMC carriers. It runs on a host device. It consists of a shell where commands can be typed, interacting with the different computing elements connected to the system.
FPGA Mezzanine Card (FMC)	FPGA Mezzanine Card is an ANSI/VITA standard that defines I/O mezzanine modules with connection to an FPGA or other device with re-configurable I/O capability. It specifies a low profile connector and compact board size for compatibility with several industry standard slot card, blade, low profile motherboard, and mezzanine form factors.
HDL	Stands for hardware description language.
Host	A host is defined as the device that configures and controls a Nutaq board. The host may be a standard computer or an embedded CPU board in the same chassis system where the Nutaq board is installed. You can develop applications on the host for Nutaq boards through the use of an application programming interface (API) that comprises protocols and functions necessary to build software applications. These API are supplied with the Nutaq board.
MicroTCA (or μTCA)	The MicroTCA (μTCA) specification is a PICMG Standard which has been devised to provide the requirements for a platform for telecommunications equipment. It has been created for AMC cards.
Model-Based Design	Refers to all the Nutaq board-specific tools and software used for development with the boards in MATLAB and Simulink and the Nutaq model-based design kits.
Model-Based Development Kit (MBDK)	The model-based development kit gives users the possibility to create FPGA configuration files, or bitstreams, without the need to be fluent in VHDL. By combining Simulink from Matlab, System Generator from Xilinx and Nutaq's tools, someone can quickly create fully-functional FPGA bitstreams for the Perseus platforms.
NTP	Network Time Protocol. NTP is a protocol to synchronize the computer time over a network.
Peer	A host peer is an associated host running RTDEx on either Linux or Windows. An FPGA peer is an associated FPGA device.

Term	Definition
PicoDigitizer / PicoSDR Systems	Refers to Nutaq products composed of Perseus AMCs and digitizer or SDR FMCs in a table top format.
PPS	Pulse per second. Event to indicate the start of a new second.
Reception (Rx)	Any data received by the referent is a reception.
Reference Design	Blueprint of an FPGA system implemented on Nutaq boards. It is intended for others to copy and contains the essential elements of a working system (in other words, it is capable of data processing), but third parties may enhance or modify the design as necessary.
Transmission (Tx)	Any data transmitted by the referent is a transmission. Abbreviated TX.
µDigitizer / µSDR Systems	Any Nutaq system composed of a combination of µTCA or ATCA chassis, Perseus AMCs and digitizer or SDR FMCs.
VHDL	Stands for VHSIC hardware description language.

Table 1 Glossary

1.3 Technical Support

Nutaq is firmly committed to providing the highest level of customer service and product support. If you experience any difficulties using our products or if it fails to operate as described, first refer to the documentation accompanying the product. If you find yourself still in need of assistance, visit the technical support page in the Support section of our Web site at www.nutaq.com.

2 Product Description

This chapter presents the hardware description of the Perseus611X module.

2.1 Overview

The Perseus 611X advanced mezzanine card (AMC or AdvancedMC) is designed around the powerful Virtex-6 FPGA, combining unsurpassed fabric flexibility and a colossal external memory, as well as benefiting from multiple high-pin-count, modular, add-on FMC-based I/O cards.

The Perseus is intended for high-performance, high-bandwidth, low-latency processing applications. The card also takes full advantage of the Virtex-6 FPGA power, which, when combined with Nutaq's advanced software development tools, makes the Perseus perfect for reducing size, complexity, risks and costs associated to leading-edge telecommunications, networking, industrial, defense and medical applications. On top this, the Perseus' FMC expansion site offers almost endless I/O possibilities.

2.1.1 Outstanding Features

- Mid-size AMC for µTCA and AdvancedTCA platforms
- Powerful SXT Virtex-6 FPGA
- Two high-pin-count VITA 57.1 FMC expansion sites for I/Os
- 4 GB DDR3 SODIMM
- Support for AMC R2.0 and R1.0 through onboard clock switch
- Available GTX base clocks — 100 MHz, 125 MHz, 156.25 MHz (PCIe/GigE/XAUI/SRIO)
- Fabric clock — RX or TX (100 MHz PCIe, default)
- IPMI controller (based on the AVR version of the Pigeon Point AdvancedMC MMC)
- FPGA and IPMI JTAGs on the Mestor interface

2.1.2 Options

The Perseus611x benefits from an extensive line of options that allow you to further enhance your development experience and final applications.

Optional Nutaq development software

The optional Perseus611x MBDK allows you to easily design high-performance digital signal processing systems within the card FPGA with the MATLAB/Simulink design environment and extensive DSP IP libraries from Xilinx.

Visit www.nutaq.com for details about this software kit.

Optional debugging hardware

Nutaq offers two optional Mestor debugging modes, from the AMC backplane or from the onboard Mestor interface.

Mestor-to-FPGA JTAG adapter

Offers direct onboard access to the FPGA JTAG chain.

Mestor expander

Offers front-panel access to the FPGA and IPMI JTAGs, 14 user LVDS I/Os, one clock, and an FPGA UART interface (serial RX/TX—Mini-B USB).

Contact Nutaq for details about these options at info@nutaq.com.

Optional FMC modules

Through its two VITA 57.1 high-pin-count (HPC) FMC expansion sites, the Perseus611x can interface with a wide variety of FMCs, such as the MI125 high-speed 16 channels A/D module.

Visit the Nutaq Web site at www.nutaq.com for more FMC modules for the Perseus611x as they become available.

2.2 Hardware Description

This section presents the Perseus611x hardware from a functional standpoint, introducing its parts and their functions.

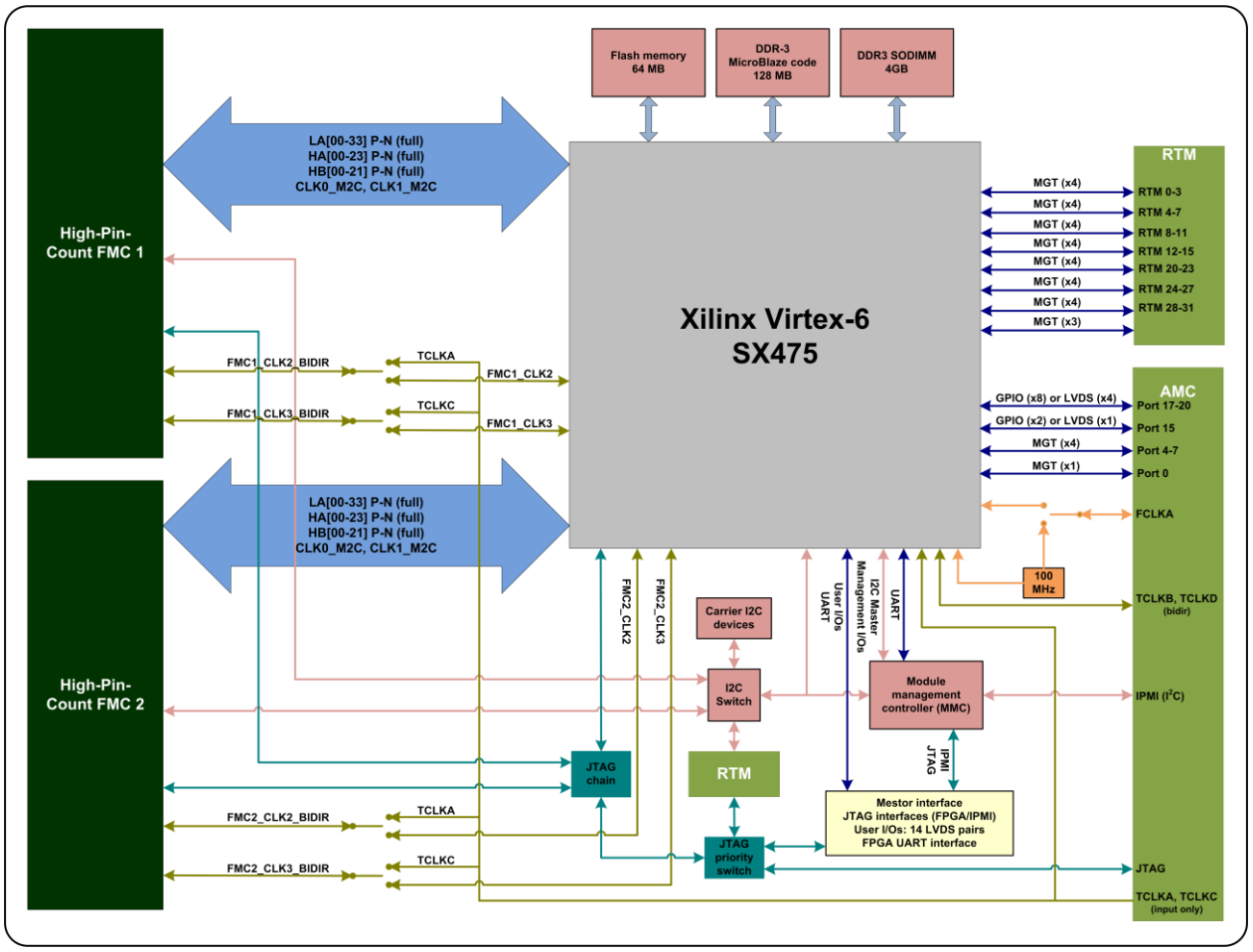

Figure 2-1 Perseus611x block diagram

2.2.1 Perseus611x Top

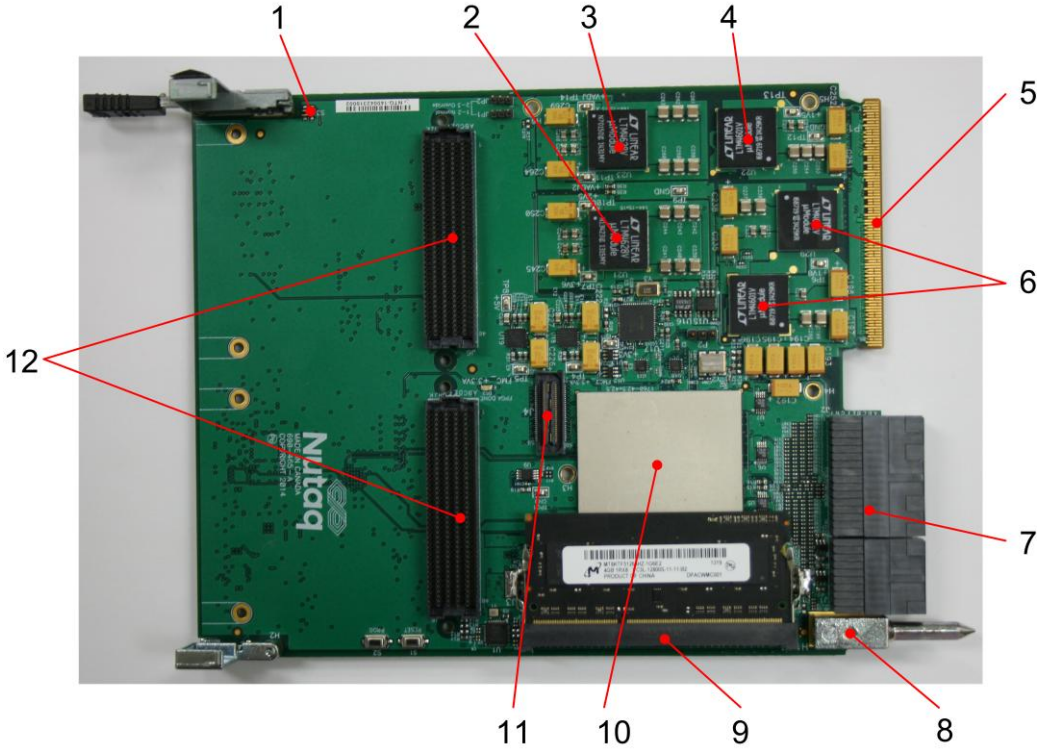

Figure 2-2 Hardware parts on the top of the Perseus611x

1) AMC handle switch

Switch enabling hot swap. When you press the switch (through the AMC handle), you instruct the system to connect the Perseus611x to the AMC backplane and to apply power.

2) 2.5V and 3.6 V power supply

Switching regulator that can supply up to 12 A at 2.5 and 3.6 V from the 12 V input. These two powers are used as intermediate tensions to supply different linear and switching regulators that are sensitive to large voltage drops.

3) Vadj1 and Vadj2 power supply

The Vadj outputs are used to supply the FPGA and the card FMC sites. The outputs can supply up to 6 A at 1.2 V, 1.5 V, 1.8 V, or 2.5 V, depending on the FPGA selection pins (respectively 00, 01, 10 or11).

4) 1.5 V power supply

Switching regulator that can supply up to 12 A at 1.5 V from the 12 V input. This power is used to supply the DDR3 SDRAM and its associated I/O bank.

5) AMC backplane connector

This connector supplies a high bandwidth to the Perseus611x. A total of 5 bidirectional gigabit-capable high-speed ports are available. Many clock inputs and outputs are also available, as well as a JTAG interface.

Important:

The Ethernet connection of the Perseus611x is only capable of Gigabit Ethernet (GigE). It is important, when connecting the chassis containing the Perseus611x with your computer Ethernet card or Ethernet switch in a point-to-point manner that your card or switch is Gigabit Ethernet capable. If not, you may encounter Ethernet communication problems.

6) 1 V power supplies

Switching regulators that can supply up to 12 A at 1 V from the 12 V input. This power is used to supply the FPGA core.

7) RTM connector

This connector supplies a huge bandwidth to the Perseus611x. A total of 31 bidirectional gigabit-capable high-speed ports are available. Many clock inputs and outputs are also available, as well as a JTAG interface.

This connector also carries an I2C and a USB bus.

The 3.3V and 12V supplied from the AMC connector to the RTM connector.

8) RTM guide pin

Guide pin for safe RTM connector insertion.

9) 64-bit DDR3 SODIMM interface

By default, this interface is connected to a 64-bit, 4 GB SODIMM for the FPGA, which can be used to support acquisition processing. Because of the Virtex-6 architecture, the maximum speed of the memory is limited to 400 MHz.

10) FPGA

The FPGA is the main processing unit of the Perseus611x. This Virtex-6 device supplies all the necessary processing power to design your algorithms and incorporates high-speed serial transceivers (GTX).

Perseus	Device	Package	Speed	Flip flop	Logic cell	Block RAM bit (#)	XtremeDSP slices	MMCM
6113	SX475T	SX475T	-1	595200	476160	38304 (1064)	2016	18

Table 2 Supported Virtex-6s

Important:
Make sure that the supplied heatsink is correctly installed on your FPGA. An incorrectly installed heatsink could lead to damages to the FPGA of your card. Verify that the heatsink three fixing pins are correctly in place.

Note:
By default, Perseus always come equipped with –1 speed FPGAs, but this can differ if you have requested it.

11) Mestor interface

Expansion connector that supplies outside-world connectivity to the Perseus611x, offering FPGA JTAG and IPMI JTAG accesses. Additionally, you can use this interface as a high-speed expansion port, using its 14 LVDS I/Os and one clock. The connector is a Samtec QSH-030-01-L-D-A-K. See Mestor interface for details.

A serial RX/TX port is also directly connected to the FPGA, making it possible for the MicroBlaze soft processor core to connect a UART to the outside world.

12) Two High-pin-count FMC (VITA 57.1) connectors

These FMC interfaces fully comply with VITA 57.1 specifications. Using FMC modules minimizes design efforts and resources. Refer to the VITA specification for details. The Perseus611x supports 80 FMC LVDS I/Os (LA00-33/HA00-23/HB00-21) with four FPGA global clocks (two FMC-to-FPGA clocks and two bidirectional clocks.

2.2.2 Perseus611x Bottom

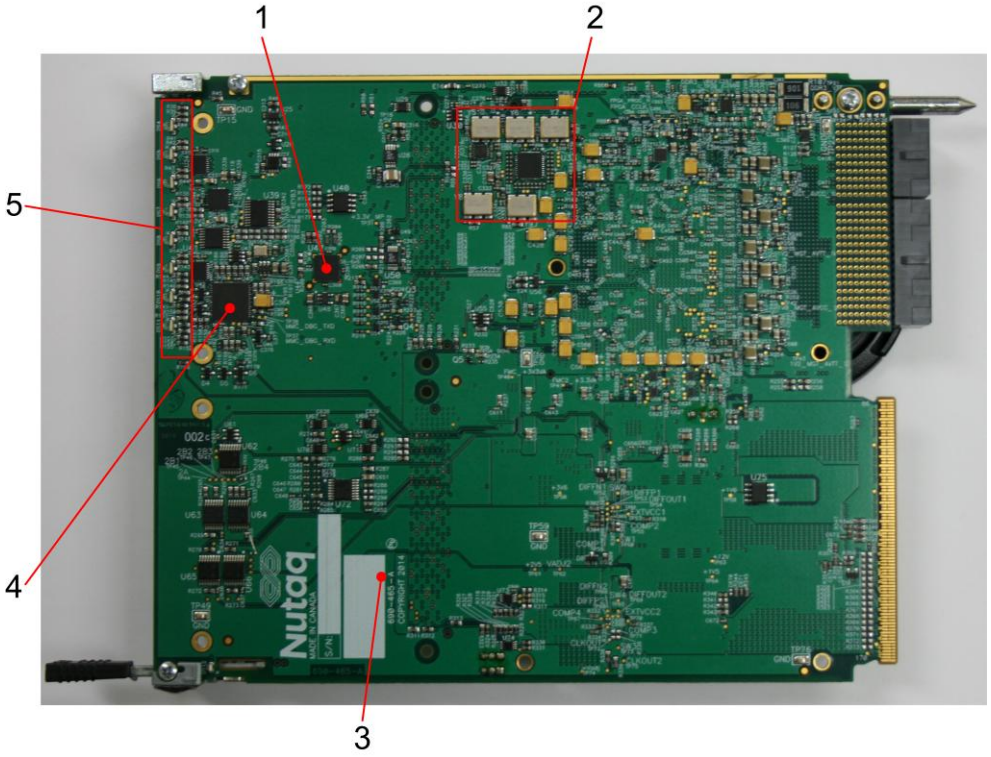

Figure 2-3 Hardware parts on the bottom of the Perseus611x

1 CPLD

The CPLD of the Perseus611x handles the arbitration of the I2C buses of the board as well as the control on the front panel LEDS. The FPGA controls the CPLD through an SPI bus.

2 Local oscillators

The Perseus611x is equipped with five local oscillators that supply the source clocks for your designs. A 200 MHz clock is available to drive logic, IODELAY controller and the onboard 128 MB DDR3 memory chip. A 400 MHz clock is vailable to drive the DDR3 SDRAM controller. A 100 MHz clock, a 125 MHz clock, and a 156.25 MHz clock drive the GTX section of the Virtex-6.

3 Board revision

The letter following 690-465 indicates the revision of the board. A indicates a revision A Perseus611x, B indicates a revision B Perseus611x and so on.

4 Module management controller

More commonly known as the MMC, this controller manages the intelligent platform management interface (IPMI) of the Perseus611x and is necessary for hot swap. The IPMI controller is based on the AVR version of the Pigeon Point AdvancedMC MMC. The controller firmware may be modified. Nutaq is equipped to deal with such requests or you can do it yourself by buying the Pigeon Point AdvancedMC MMC.

5 Front panel LEDs

The Perseus611x is equipped with eight dual-color LEDs connected to the CPLD through a buffer. The buffer must be enabled to drive the LEDs. LEDs light when a zero is driven to the appropriate I/Os of the CPLD.

2.2.3 Front Panels

Depending on the configuration of your Perseus611x, you may need to use one of the two available front panels. One enables the use of two full-size FMCs, the other 1 full-size and one half-size.

Perseus611x Half-size/full-size front panel

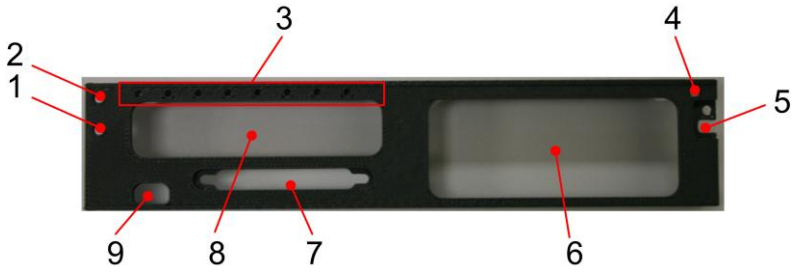

Figure 2-4 Half-size/full-size front panel description

1) Malfunction LED

This red LED lights when a critical power supply signal is not asserted as good or the board is overheating.

2) Power LED

This green LED is ON when all the signals from critical power supplies are asserted as good and that a bitstream can be loaded in the FPGA. The LED blinks when the MicroBlaze is functioning properly.

3) Front panel LEDs

The Perseus is equipped with eight dual-color LEDs connected to the CPLD through a buffer. The buffer must be enabled, through the output enable pin of the buffer, to drive the LEDs. LEDs light when a zero is driven to the appropriate I/Os of the CPLD.

Note:
LED behavior is defined by you for your applications.

4) AMC state LED

This blue LED is governed by the operational state (hotswap behavior) of the Perseus MMC (see previous page).

AMC state LED conditions:

Condition	Description
Off	The Perseus is running properly. At this point, the power LED is also on.
Blinking	The Perseus is: - Powering up (after pressing the AMC handle, upon insertion) - Powering down (after pulling the AMC handle)
On	When the LED is on, you can: - If you inserted the Perseus in the chassis: press the AMC handle to power up the card. - If you are attempting to remove the Perseus from the chassis, do so.

Note:
If the AMC state LED does not stop blinking, it is likely that the Perseus cannot power up. Refer to your chassis IPMI log for details as to the reason(s). Usually, using a more powerful chassis or removing cards from your current chassis will resolve the situation.

5) AMC handle

The handle of the Perseus fits here.

6) Full-size FMC module faceplate

The faceplate of your chosen full-size FMC module fits here.

7) Mestor interface

When the Mestor is connected to the Perseus, it provides a 30-pin GPIO interface directly connected to the FPGA as well as the access to the FPGA and MMC JTAG chains and a UART bus interface.

8) Mid-size FMC module faceplate

The faceplate of your chosen mid-size FMC module fits here.

9) USB/UART port

When the Mestor is connected to the Perseus, this port is used as a USB-to-UART bridge for your remote computer.

Perseus Full-size/full-size front panel

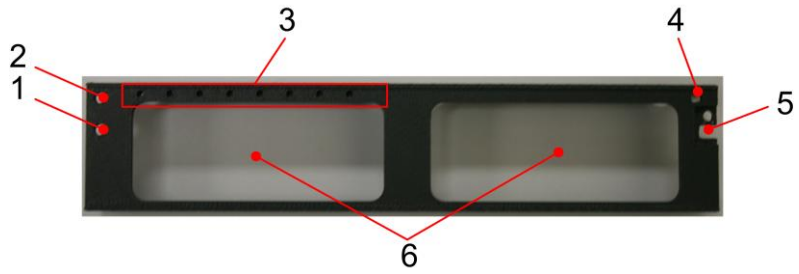

Figure 2-5 Full-size/full-size front panel description

1) Malfunction LED

This red LED lights when a critical power supply signal is not asserted as good or the board is overheating.

2) Power LED

This green LED is ON when all the signals from critical power supplies are asserted as good and that a bitstream can be loaded in the FPGA. The LED blinks when the MicroBlaze is functioning properly.

3) Front panel LEDs

The Perseus is equipped with eight dual-color LEDs connected to the CPLD through a buffer. The buffer must be enabled, through the output enable pin of the buffer, to drive the LEDs. LEDs light when a zero is driven to the appropriate I/Os of the CPLD.

Note:
LED behavior is defined by you for your applications.

4) AMC state LED

This blue LED is governed by the operational state (hotswap behavior) of the Perseus MMC (see previous page).

AMC state LED conditions:

Condition	Description
Off	The Perseus is running properly. At this point, the power LED is also on.
Blinking	The Perseus is: - Powering up (after pressing the AMC handle, upon insertion) - Powering down (after pulling the AMC handle)
On	When the LED is on, you can: - If you inserted the Perseus in the chassis: press the AMC handle to power up the card. - If you are attempting to remove the Perseus from the chassis, do so.

Note:
If the AMC state LED does not stop blinking, it is likely that the Perseus cannot power up. Refer to your chassis IPMI log for details as to the reason(s). Usually, using a more powerful chassis or removing cards from your current chassis will resolve the situation.

5) AMC handle

The handle of the Perseus fits here.

6) Full-size FMC module faceplates

The faceplates of your chosen full-size FMC modules fit here.

2.3 Component Details

2.3.1 Perseus611x Clock Tree

The Perseus611x is equipped with many clock sources. Depending on your application, you can select almost any of the FPGA clocks.

The diagram below shows every clock available on the Perseus611x and its related FPGA pin.

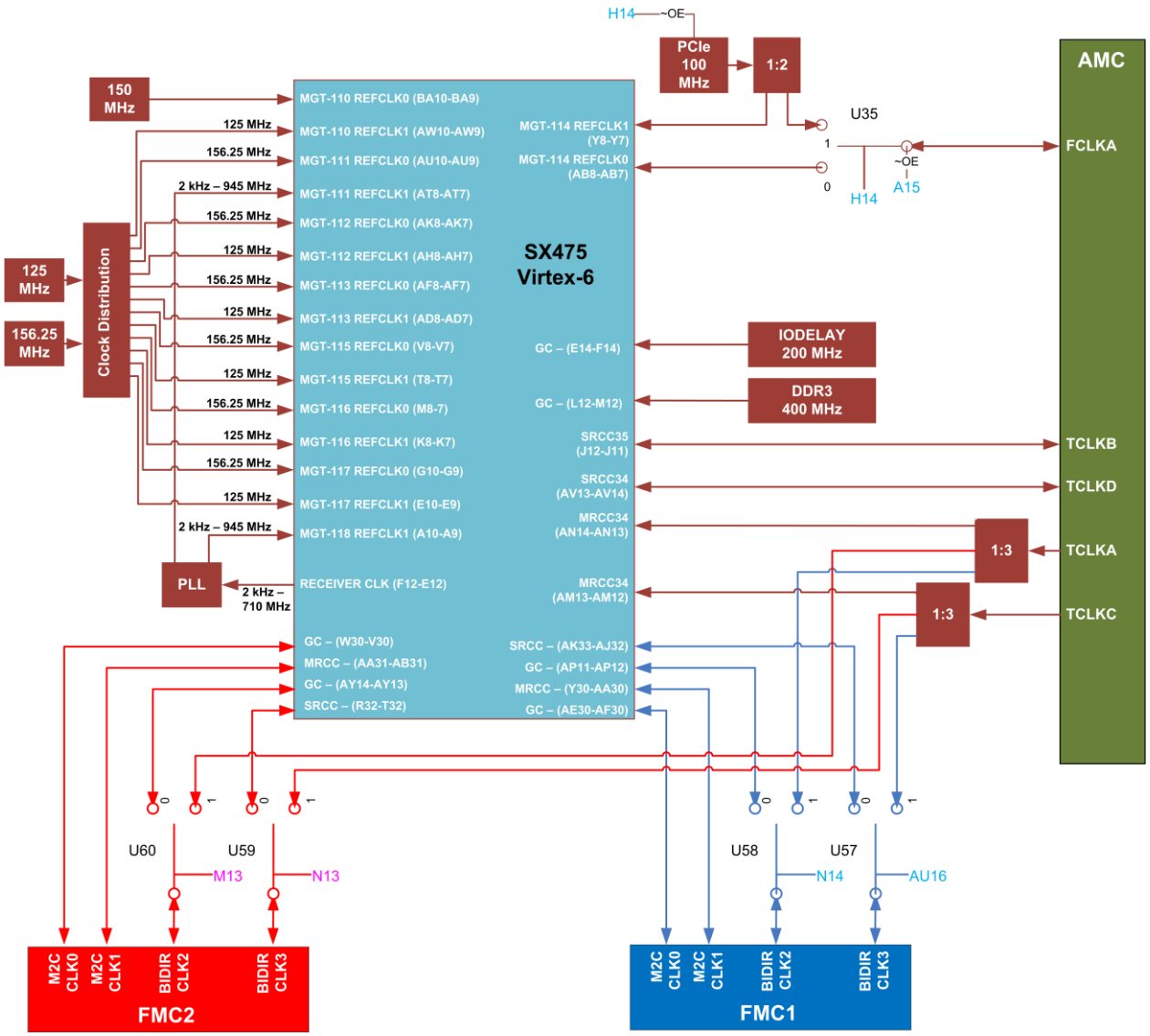

Figure 2-6 Perseus611x clock scheme

Type of reference clocks

There are four types of clocks on the Perseus: global clocks (GC), the multi-region capable clocks (MRCC), single-region capable clocks (SRCC), and Gigabit transceiver (MGT) reference clocks. Clock outputs are only normal I/Os.

Global clock

In the Perseus FPGA, global clocks are a dedicated network specifically designed to route all the clock inputs to the various resources of the FPGA. This network is designed for low skew and low-duty-cycle distortion, to consume very little power, and to have an improved tolerance to jitter compared to older generations. They are also designed to support very-high-frequency signals. On the Perseus, FMC clocks are used to forward A/D, D/A, and communication reference clocks. The FMC CLK0 of both FMC connectors are

connected to GC inputs. The DDR3 400 MHz reference is also be connected to the DDR3 memory controller through a GC. A 200 MHz clock is also connected to the FPGA as a reference clock for the I/O delays and as the MicroBlaze system clock.

Multi-region capable clocks and single-region capable clocks

Regional clocks are a different network that does not depend on the global clock network. Unlike global clocks, the span of regional clock signals are limited to three clock regions, while two I/O clock signals drive a single region (SRCC) and two other I/O clocks drive the regions/banks above/below (MRCC). The I/O banks in Virtex-6 FPGAs are the same size as a clock region.

Regional clocks are especially useful in source-synchronous interface designs, but, as AMC TCLK are reference clocks, they are often used by the MMCM. The platform connects each TCLK to unused MRCCs and SRCCs. These pins have, internally, a direct connection to an MMCM, thus you can reach the global clock tree and use the TCLKx as your design system clock.

Note:

To learn more about regional clocks, refer to Xilinx documentation.

MGT reference clock

MGTs, also called GTX, offer several available reference clock inputs. This feature allows the same MGT to be used under more than one standard. MGTs can, in fact, be used by six external reference clocks. As MGTs are organized in groups of four, they can use two reference clocks in their own group or two reference clocks in the groups directly before or after. For details, see Virtex-6 high-speed serial transceivers (GTX).

Six 125 MHz and six 156.25 MHz clocks are connected to MGT reference clock inputs. There are also a 150 MHz clock and a 100 MHz clock that are connected to MGT reference clock inputs. In addition, there are two MGT clock inputs that can be configured from an onboard clock multiplier and jitter attenuator chip (Si5324).

2.3.2 Virtex-6 High-Speed Serial Transceivers (GTX)

This section explains Perseus611x from its high-speed serial transceivers perspective. These transceivers are usually called GTX in the range of speeds of the Virtex-6 FPGA on the Perseus611x.

Unit interconnection

The AdvancedMC (AMC) standard relies heavily on high-speed serial communications to enable multiple communication schemes. AMC allows direct interconnections, point to point. Direct interconnection implies that Perseus611x A can communicate directly with Perseus611x B through a given high-speed port, while communicating with Perseus611x C through a different port and, at the same time, Perseus611x B communicates with Perseus611x C through yet another port in the same chassis. Of course, each link must go through a dedicated backplane interconnection (static) or through a switch in an MCH (dynamic). This architecture eliminates the bottle necks common in other architectures such as cPCI, for example, where a processor must orchestrate all the data transfers. Such a topology makes it impossible to unintentionally use all the throughput of all the units at the same time in a given chassis; whereas, with AMC it becomes easy.

The ability to easily interconnect units also makes it possible to vastly expand systems. For example, if Perseus611x A receives data from its FMC interface, transmits this data to Perseus611x B, which transmits the result on its FMC interface. Now, imagine the processing performed by these two Perseus611x getting larger as you approach your project goals (or through natural product evolution), so large that two units are no longer sufficient despite efficient partition design. AMC and the Virtex-6 GTX offer a simple solution: add a third Perseus611x between the existing two, properly connect the high-speed ports and spread the processing over the three cards. This way, you can easily daisy chain many units to suit your needs.

GTX layout

The Virtex-6 GTX come in groups of four to form what is called a GTX quad and are numbered 110 to 118 in the Xilinx documentation. Each quad has two dedicated clock reference inputs, called MgtRefClk. These inputs are used to supply the GTX with a high-quality clock signal. A GTX clock can come from the MgtRefClk of its own quad or from any one of the two adjacent quads, as long as the adjacent quad supplying the clock is populated with at least

one GTX, (even if it is a dummy one). In other words, a given MgtRefClk can feed its own quad and the two adjacent ones, as illustrated here.

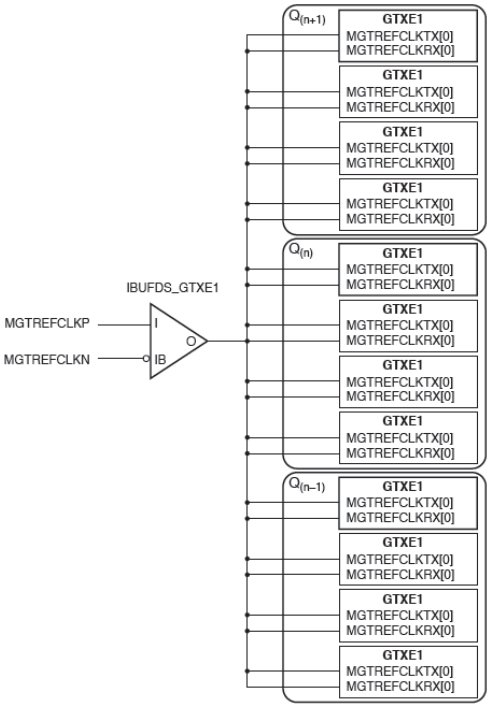

Figure 2-7 Multiple GTX with shared reference clock

The tables below show the clock signals connected to each GTX quad and list the various clock inputs and frequencies available to the GTX of the Perseus611x, according to the various high-speed serial ports. The FClkA label represents the frequency of the clock supplied by the backplane and is typically 100 MHz. The PLL1 and PLL2 labels represent the frequencies of the clocks generated by the onboard clock multiplier and jitter attenuator chip (Si5324)of the Perseus611x. They are implementation specific and can range from 2 kHz to 945 MHz.

150.00 MHz 125.00 MHz 156.25 MHz PLL1	Quad 110 - SATA + SGMII
156.25 MHz 125.00 MHz	Quad 111 - RTM0-3
156.25 MHz 125.00 MHz	Quad 112 - RTM8-11
FCLKA 100.00 MHz	Quad 113 - RTM12-15
156.25 MHz 125.00 MHz	Quad 114 - AMC4-7
156.25 MHz 125.00 MHz	Quad 115 - RTM20-23
156.25 MHz 125.00 MHz	Quad 116 - RTM24-27
156.25 MHz 125.00 MHz	Quad 117 - RTM28-31
PLL2	Quad 118 - RTM4-7

Table 3 GTX clocks interconnect

			Available Clocks (grey = available)						
Quad	**GTX Signal**	**FPGA GTX Address**	**100.00 MHz**	**125.00 MHz**	**150.00 MHz**	**156.25 MHz**	**FCLKA**	**PLL1**	**PLL2**
110	RTMSATA0	GTXE1_X0Y0							
	RTMSATA1	GTXE1_X0Y1							
	RTMSATA2	GTXE1_X0Y2							
	AMC0	GTXE1_X0Y3							
111	RTM0	GTXE1_X0Y4							
	RTM1	GTXE1_X0Y5							
	RTM2	GTXE1_X0Y6							
	RTM3	GTXE1_X0Y7							
112	RTM8	GTXE1_X0Y8							
	RTM9	GTXE1_X0Y9							
	RTM10	GTXE1_X0Y10							
	RTM11	GTXE1_X0Y11							
113	RTM12	GTXE1_X0Y12							
	RTM13	GTXE1_X0Y13							
	RTM14	GTXE1_X0Y14							
	RTM15	GTXE1_X0Y15							
114	AMC4	GTXE1_X0Y16							
	AMC5	GTXE1_X0Y17							
	AMC6	GTXE1_X0Y18							
	AMC7	GTXE1_X0Y19							
115	RTM20	GTXE1_X0Y20							
	RTM21	GTXE1_X0Y21							
	RTM22	GTXE1_X0Y22							
	RTM23	GTXE1_X0Y23							
116	RTM24	GTXE1_X0Y24							
	RTM25	GTXE1_X0Y25							
	RTM26	GTXE1_X0Y26							
	RTM27	GTXE1_X0Y27							
117	RTM28	GTXE1_X0Y28							
	RTM29	GTXE1_X0Y29							
	RTM30	GTXE1_X0Y30							
	RTM31	GTXE1_X0Y31							
118	RTM4	GTXE1_X0Y32							
	RTM5	GTXE1_X0Y33							
	RTM6	GTXE1_X0Y34							
	RTM7	GTXE1_X0Y35							

Table 4 GTX quads clocks availability

RX/TX PLLs

Among other features, each GTX comprises an RX PLL and a TX PLL that can generate numerous data rates from the reference clock. The figure below illustrates how each PLL can be sourced by the two MgtRefClk of its own quad, as well as by those of the two adjacent quads.

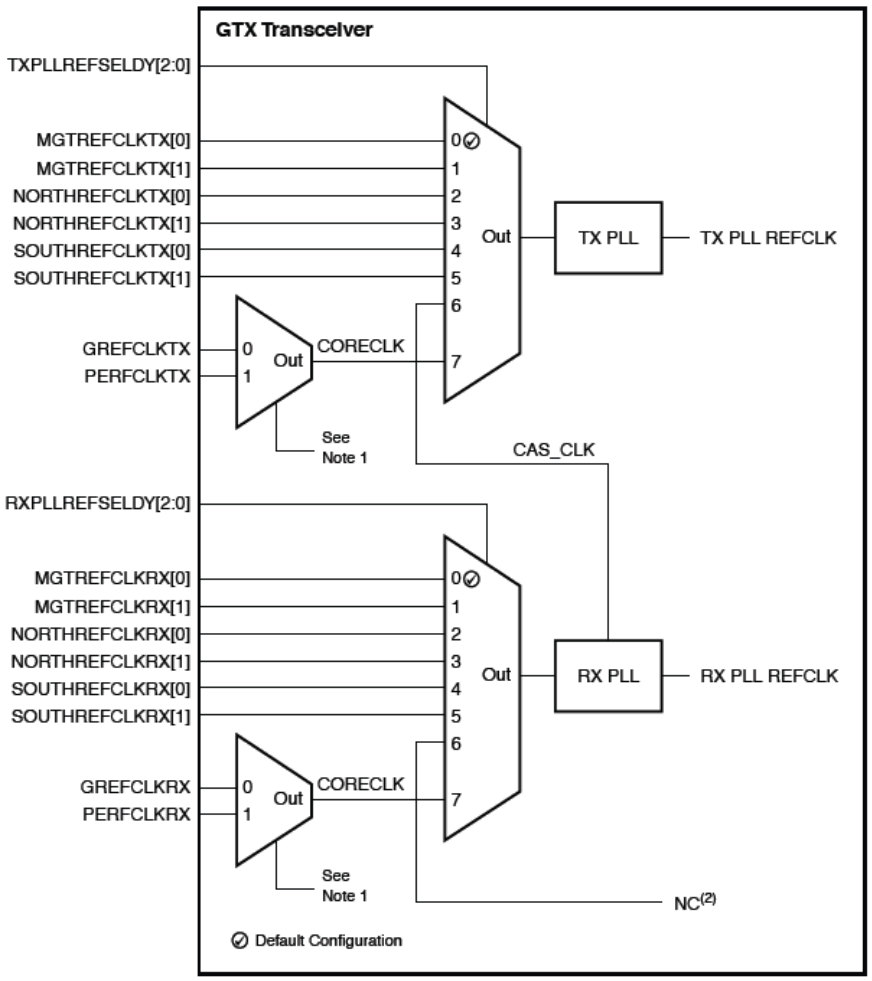

Figure 2-8 GTX detailed diagram

When you use the same clock in RX and TX, you can share the RX PLL and turn off the TX PLL to reduce power consumption.

Equalization

To ensure good data reception by the GTX, its RX section is equipped with an equalizer. You can tune this equalizer so that it fits the operating frequency of the GTX while more or less cutting the lower frequency portion of the spectrum. Available equalizer settings are illustrated here:

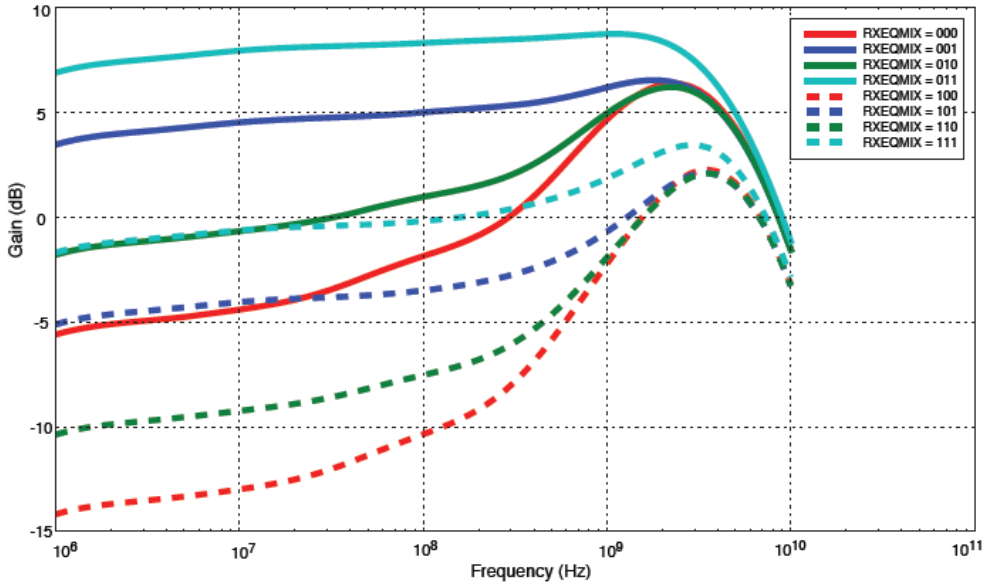

Figure 2-9 Absolute gain (voltage transfer function)

Perseus Interfaces

The GTX on the AMC and RTM backplanes support several communications standards such as GigE, PCIe, XAUI, SATA, and SRIO. Each standard already has a prescribed position in the port map of the AMC backplane, as described in the AdvancedMC standard. The generic nature of the GTX, however, also allows you to use them for other purposes (custom or not), as long as you do not need interoperability with other systems on these ports. For example, the Xilinx Virtex-6 Embedded Tri-Mode Ethernet MAC Wrapper core supports typical Ethernet data rates, but it also supports overclocking at rates up to 2.5 Gbps. In other words, using two Perseus on a backplane that supports 2.5 Gbps, you can leverage transferring data over Ethernet at twice the standard speed.

From the FMC standpoint, the GTX have no protocols, which is consistent with the GTX philosophy. The FMC interface is dynamic — it is designed to support a vast variety of I/O standards, voltages, directions, differential/single-ended combinations, within limits.

For details about GTX, refer to the Virtex-6 FPGA GTX user's guide available from the Xilinx Web site at www.xilinx.com.

2.3.3 Mestor Interface

The Mestor interface is the Perseus connection. It offers JTAG capabilities, 14 differential I/Os or 28 single-ended I/Os, a differential clock I/O, and an FPGA UART interface (serial TX and RX) based on LVCMOS 2.5 V signaling. The Mestor expander allows you to interface directly with these I/Os.

The Mestor is the debugging connection for the Perseus 601X. It is a unique, onboard interface that regroups standard debugging ports and other interfaces. The Mestor interface offers access to:

- FPGA JTAG
- IPMI JTAG (typically used to debug the Atmel AVR MCU)
- FPGA UART (serial TX and RX)
- User LVDS I/Os (differential data × 14, differential clock × 1)
- 2.5 V and 3.3 V power (used to supply Mestor breakout boxes)

Mestor interface

The following table presents the Mestor interface pin assignment.

Pin	Assignment	Pin	Assignment
1	DPIO_0_P	2	DPIO_10_P
3	DPIO_0_N	4	DPIO_10_N
5	GND	6	GND
7	DPIO_1_P	8	DPIO_11_P
9	DPIO_1_N	10	DPIO_11_N
11	+2.5V	12	GND
13	DPIO_2_P	14	DPIO_12_P
15	DPIO_2_N	16	DPIO_12_N
17	GND	18	GND
19	DPIO_3_P	20	DPIO_13_P
21	DPIO_3_N	22	DPIO_13_N
23	+2.5V	24	GND
25	DPIO_4_P	26	DPIO_CLK_P
27	DPIO_4_N	28	DPIO_CLK_N
29	GND	30	JTAG_PRSNT_N
31	DPIO_5_P	32	SERIAL_RX
33	DPIO_5_N	34	SERIAL_TX

Pin	Assignment	Pin	Assignment
35	+2.5V	36	+3.3V
37	DPIO_6_P	38	+3.3V
39	DPIO_6_N	40	+3.3V
41	GND	42	AVR_TDI
43	DPIO_7_P	44	FPGA_TDI
45	DPIO_7_N	46	AVR_TMS
47	+2.5V	48	FPGA_TMS
49	DPIO_8_P	50	AVR_TDO
51	DPIO_8_N	52	FPGA_TDO
53	GND	54	AVR_TCK
55	DPIO_9_P	56	FPGA_TCK
57	DPIO_9_N	58	AVR_TRST
59	Daughter_prsnt_n	60	FPGA_TRST
61	GND	62	GND
63	GND	64	GND

Table 5 Mestor interface pin assignments of the Perseus board

Note:
The DPIO name convention of the Mestor Expander board does not follow the same convention than the Mestor DPIO name of the Perseus board.

Mestor JTAG adapters

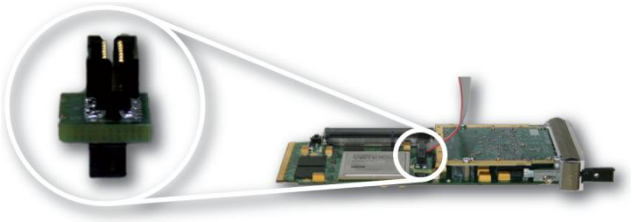

Figure 2-10 Mestor JTAG adapter

To access the Perseus' JTAG chains, you can use the Mestor JTAG adapters (LSP158-901) that includes a Mestor-to-FPGA JTAG adapter and a Mestor-to-AVR JTAG adapter. Connected to a Xilinx platform cable, you can easily troubleshoot your FPGA software through the FPGA JTAG chain with the Mestor-to-FPGA adapter. With an Atmel AVR MCU and the Mestor-to-AVR adapter, you can as easily troubleshoot the IPMI stack of the Perseus.

Mestor expander

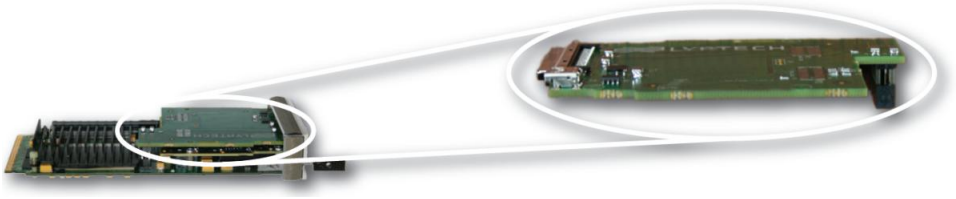

Figure 2-11 Mestor expander

The Mestor expander saves you from having to free µTCA slots or to open the chassi shelf to access debugging interfaces. The kit includes the necessary front panel cables.

The Mestor expander offers two front panel connections:

- FPGA UART (mini-AB USB). This connector maps the FPGA UART pins through a USB-to-UART bridge (CP2110 from Silicon Labs).
- Mestor debugging I/Os (VHDCI connector), regrouping IPMI and FPGA JTAGs, user LVDS I/Os and power. This connector allows you or Nutaq to expand the capabilities of the Perseus.

More information on the Mestor expander card is available in the Mestor expander documentation.

2.3.4 JTAG Chain

The FPGA JTAG chain is used to download bitstreams and debug the FPGA. It is also connected to the FMC connector and to the Mestor interface. JTAG configurations are automatically adjusted according to your hardware. The chain also supports three configurations: the Mestor interface, the RTM USB and the AMC backplane as master. By default, the chain is routed through the AMC backplane but when a JTAG pod is present at the Mestor interface, it automatically becomes the chain master as it has the most priority (see below).

Only one of the three JTAG connections is active at a time. To insure this behavior, the following priority has been implemented on the board.

1. Mestor interface (1 of 2 ways)
    a. Through the Mestor JTAG adaptor
    b. Through the Mestor expander
2. RTM USB interface
3. AMC backplane

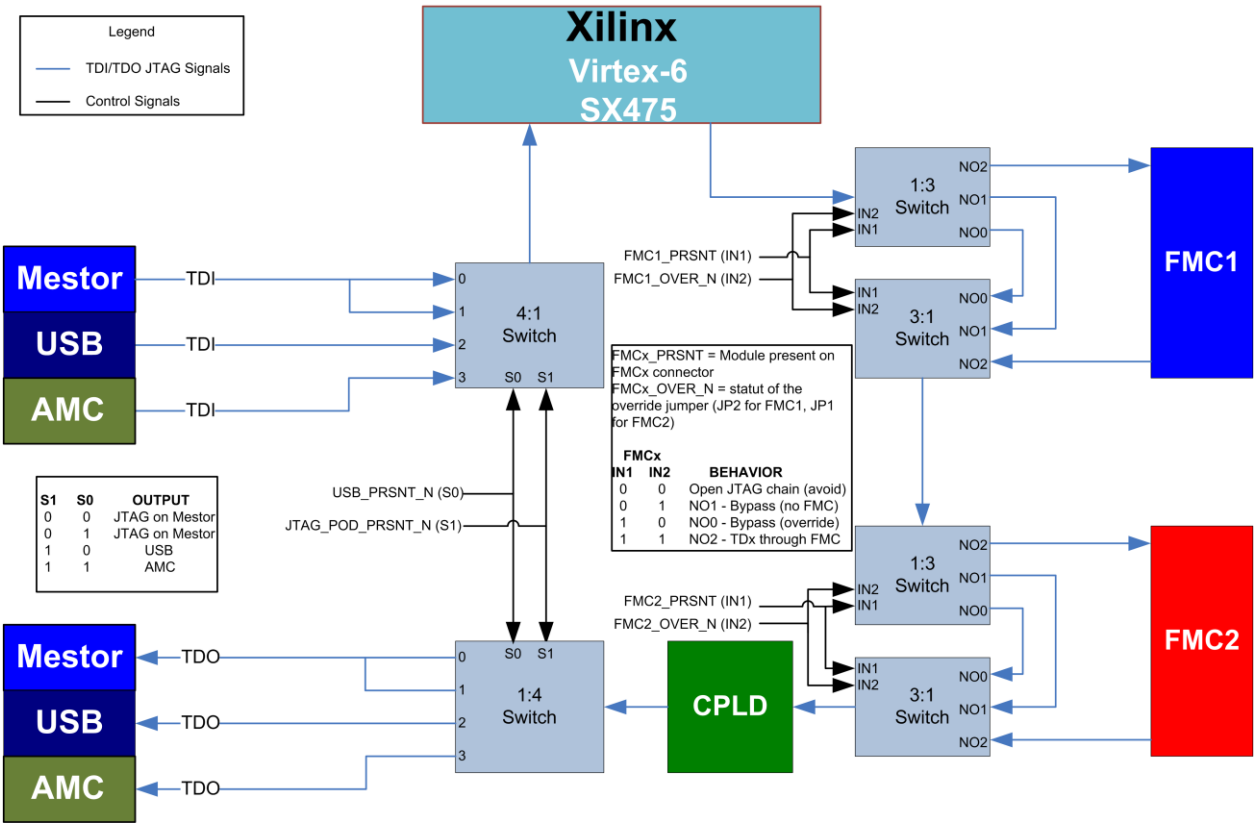

Figure 2-12 Perseus JTAG chain

2.3.5 AMC Backplane Connector

The Perseus611x comes with a fully compliant AMC backplane connector. The following pin assignments are provided as reference, so that you can ascertain whether your backplane is compatible with the Perseus611x.

Note:
The pin assignments below take into account that you are familiar with AMC signals. Refer to the PICMG AMC.0 R2.0 specifications for signal descriptions.

AMC Backplane Connector

Pin	Assignment	Pin	Assignment	Pin	Assignment	Pin	Assignment	Pin	Assignment
1	GND	35	TX3+	69	RX7–	103	TX10+	137	GND
2	12 V	36	TX3–	70	GND	104	GND	138	TCLKD–
3	~PS1	37	GND	71	IPMI_SDA	105	RX11–	139	TCLKD+
4	3.3V_MP	38	RX3+	72	12 V	106	RX11+	140	GND
5	GA0	39	RX3–	73	GND	107	GND	141	RX17–
6	RSVD	40	GND	74	TCLKA+	108	TX11–	142	RX17+
7	GND	41	~Enable	75	TCLKA–	109	TX11+	143	GND
8	RSVD	42	12 V	76	GND	110	GND	144	TX17–
9	12 V	43	GND	77	TCLKB+	111	RX12–	145	TX17+
10	GND	44	TX4+	78	TCLKB–	112	RX12+	146	GND
11	TX0+	45	TX4–	79	GND	113	GND	147	RX18–
12	TX0–	46	GND	80	FCLKA+	114	TX12–	148	RX18+
13	GND	47	RX4+	81	FCLKA–	115	TX12+	149	GND
14	RX0+	48	RX4–	82	GND	116	GND	150	TX18–
15	RX0–	49	GND	83	~PS0	117	RX13–	151	TX18+
16	GND	50	TX5+	84	12 V	118	RX13+	152	GND
17	GA1	51	TX5–	85	GND	119	GND	153	RX19–
18	12 V	52	GND	86	GND	120	TX13–	154	RX19+
19	GND	53	RX5+	87	RX8–	121	TX13+	155	GND
20	TX1+	54	RX5–	88	RX8+	122	GND	156	TX19–
21	TX1–	55	GND	89	GND	123	RX14–	157	TX19+

Pin	Assignment	Pin	Assignment	Pin	Assignment	Pin	Assignment	Pin	Assignment
22	GND	56	IPMI_SCL	90	TX8–	124	RX14+	158	GND
23	RX1+	57	12 V	91	TX8+	125	GND	159	RX20–
24	RX1–	58	GND	92	GND	126	TX14–	160	RX20+
25	GND	59	TX6+	93	RX9–	127	TX14+	161	GND
26	GA2	60	TX6–	94	RX9+	128	GND	162	TX20–
27	12 V	61	GND	95	GND	129	RX15–	163	TX20+
28	GND	62	RX6+	96	TX9–	130	RX15+	164	GND
29	TX2+	63	RX6–	97	TX9+	131	GND	165	JTAG_TCK
30	TX2-	64	GND	98	GND	132	TX15–	166	JTAG_TMS
31	GND	65	TX7+	99	RX10–	133	TX15+	167	JTAG_TRSTN
32	RX2+	66	TX7–	100	RX10+	134	GND	168	JTAG_TDO
33	RX2–	67	GND	101	GND	135	TCLKC–	169	JTAG_TDI
34	GND	68	RX7+	102	TX10–	136	TCLKC+	170	GND

Table 6 AMC backplane connector pin assignments

2.3.6 Module Management Controller

The module management controller (MMC) is responsible for the AMC hot swap capabilities and the supervision of its functionalities. In an AMC chassis, each card is known as a field-replaceable unit (FRU). Each FRU can be queried for its status. (Refer to the user's guide of your chassis to learn how to read your FRU data.)

The MMC is equipped with a suite of sensors that monitor the card parameters. Each sensor is linked to an ID number so that it can read its value through the IPMI link. The following table presents the ID of each sensor.

MMC sensor definition records

ID	Name	Description
1	Hot swap	Hot swap handle switch.
2	3.3 V	Voltage reading of the 3.3V_MP power supply.
3	12 V	Voltage reading of the 12 V power supply.
4	TMP411 local temp	I^2C sensor for local temperature.
5	BMC watchdog	AVR watchdog.
6	PG_DDR3_VTT	Power good signal from the DDR3_VREF supply.
7	PG_3V3	Power good signal from the 3V3 supply.
8	PG_1V8	Power good signal from the 1V8 supply.
9	PG_VADJ	Power good signal from the V_{adj} supply.
10	PG_2V5	Power good signal from the 2V5 supply.
11	PG_3V8	Power good signal from the 3V8 supply.
12	PG_1V5	Power good signal from the 1V5 supply.
13	PG_1V0	Power good signal from the 1V0 supply.
14	FMC_PG_M2C	Power good signal from the 3V3 supply of the FMC module on the Perseus.
15	PG_MGT_AVTT_N	Power good signal from the 1V2 supply for the MGTAVTT_N supply.
16	PG_MGT_AVCC_N	Power good signal from the 1V0 supply for the MGTAVCC_N supply.
17	PG_MGT_AVCC_S	Power good signal from the 1V0 supply for the MGTAVCC_S supply.
18	PG_MGT_AVTT_S	Power good signal from the 1V2 supply for the MGTAVTT_S supply.

Table 7 MMC sensor definition records

2.4 FPGA Pin Assignments

In this section, we present the FPGA pins and their I/O assignments. For differential pairs, the LOC+ symbol represents the positive “p” pin and the LOC– symbol represents the negative “n” pin. “GTXEx” indicates the GTX address in the core, but has no valid standard for the UCF.

External reset FPGA pin assignment

Pin name	LOC+	I/O buffer	I/O standard	Resistor
EXT_RESET	AV16	IN	LVCMOS25	PULLDOWN

Table 8 External reset

AMC Connector FPGA pin assignment

Pin name	Index	LOC+	LOC–	I/O buffer	GTX address/ I/O standard
AMC_RX	0	AW5	AW6	INDS	GTXE1_X0Y3
AMC_RX	4	AC5	AC6	INDS	GTXE1_X0Y16
AMC_RX	5	AB3	AB4	INDS	GTXE1_X0Y17
AMC_RX	6	AA5	AA6	INDS	GTXE1_X0Y18
AMC_RX	7	Y3	Y4	INDS	GTXE1_X0Y19
AMC_RX	15	C13	D12	INDS	LVDS_25/LVCMOS25
AMC_TX	0	AW1	AW2	OUTDS	GTXE1_X0Y3
AMC_TX	4	AE1	AE2	OUTDS	GTXE1_X0Y16
AMC_TX	5	AC1	AC2	OUTDS	GTXE1_X0Y17
AMC_TX	6	AA1	AA2	OUTDS	GTXE1_X0Y18
AMC_TX	7	W1	W2	OUTDS	GTXE1_X0Y19
AMC_TX	15	J13	K13	OUTDS	LVDS_25/LVCMOS25

Table 9 AMC connector

AVR (IPMI) FPGA pin assignment

Pin name	LOC+	I/O buffer	I/O standard
AVR_RXD	AW35	IN	LVCMOS25
AVR_TXD	AY34	OUT	LVCMOS25
E_KEY0_FPGA	D15	INOUT	LVCMOS25
E_KEY1_FPGA	C15	INOUT	LVCMOS25
E_KEY2_FPGA	G12	INOUT	LVCMOS25
E_KEY3_FPGA	H13	INOUT	LVCMOS25

Table 10 AVR (IPMI)

Rear Transition Module (RTM) FPGA pin assignment

Pin name	Index	LOC+	LOC–	I/O buffer	GTX address
RX_SATA	0	BB7	BB8	INDS	GTXE1_X0Y0
RX_SATA	1	BA5	BA6	INDS	GTXE1_X0Y1
RX_SATA	2	AY7	AY8	INDS	GTXE1_X0Y2
MGT_RTM_RX	0	AV7	AV8	INDS	GTXE1_X0Y4
MGT_RTM_RX	1	AU5	AU6	INDS	GTXE1_X0Y5
MGT_RTM_RX	2	AR5	AR6	INDS	GTXE1_X0Y6
MGT_RTM_RX	3	AP7	AP8	INDS	GTXE1_X0Y7
MGT_RTM_RX	4	D7	D8	INDS	GTXE1_X0Y32
MGT_RTM_RX	5	C5	C6	INDS	GTXE1_X0Y33
MGT_RTM_RX	6	B7	B8	INDS	GTXE1_X0Y34
MGT_RTM_RX	7	A5	A6	INDS	GTXE1_X0Y35
MGT_RTM_RX	8	AN5	AN6	INDS	GTXE1_X0Y8
MGT_RTM_RX	9	AM7	AM8	INDS	GTXE1_X0Y9
MGT_RTM_RX	10	AL5	AL6	INDS	GTXE1_X0Y10
MGT_RTM_RX	11	AJ5	AJ6	INDS	GTXE1_X0Y11

Pin name	Index	LOC+	LOC–	I/O buffer	GTX address
MGT_RTM_RX	12	AG5	AG6	INDS	GTXE1_X0Y12
MGT_RTM_RX	13	AF3	AF4	INDS	GTXE1_X0Y13
MGT_RTM_RX	14	AE5	AE6	INDS	GTXE1_X0Y14
MGT_RTM_RX	15	AD3	AD4	INDS	GTXE1_X0Y15
MGT_RTM_RX	16	AC5	AC6	INDS	GTXE1_X0Y16
MGT_RTM_RX	17	AB3	AB4	INDS	GTXE1_X0Y17
MGT_RTM_RX	18	AA5	AA6	INDS	GTXE1_X0Y18
MGT_RTM_RX	19	Y3	Y4	INDS	GTXE1_X0Y19
MGT_RTM_RX	20	W5	W6	INDS	GTXE1_X0Y20
MGT_RTM_RX	21	V3	V4	INDS	GTXE1_X0Y21
MGT_RTM_RX	22	U5	U6	INDS	GTXE1_X0Y22
MGT_RTM_RX	23	R5	R6	INDS	GTXE1_X0Y23
MGT_RTM_RX	24	P7	P8	INDS	GTXE1_X0Y24
MGT_RTM_RX	25	N5	N6	INDS	GTXE1_X0Y25
MGT_RTM_RX	26	L5	L6	INDS	GTXE1_X0Y26
MGT_RTM_RX	27	J5	J6	INDS	GTXE1_X0Y27
MGT_RTM_RX	28	H7	H8	INDS	GTXE1_X0Y28
MGT_RTM_RX	29	G5	G6	INDS	GTXE1_X0Y29
MGT_RTM_RX	30	F7	F8	INDS	GTXE1_X0Y30
MGT_RTM_RX	31	E5	E6	INDS	GTXE1_X0Y31
TX_SATA	0	BB3	BB4	OUTDS	GTXE1_X0Y0
TX_SATA	1	BA1	BA2	OUTDS	GTXE1_X0Y1
TX_SATA	2	AY3	AY4	OUTDS	GTXE1_X0Y2
MGT_RTM_TX	0	AV3	AV4	OUTDS	GTXE1_X0Y4
MGT_RTM_TX	1	AU1	AU2	OUTDS	GTXE1_X0Y5

Pin name	Index	LOC+	LOC–	I/O buffer	GTX address
MGT_RTM_TX	2	AT3	AT4	OUTDS	GTXE1_X0Y6
MGT_RTM_TX	3	AR1	AR2	OUTDS	GTXE1_X0Y7
MGT_RTM_TX	4	E1	E2	OUTDS	GTXE1_X0Y32
MGT_RTM_TX	5	D3	D4	OUTDS	GTXE1_X0Y33
MGT_RTM_TX	6	C1	C2	OUTDS	GTXE1_X0Y34
MGT_RTM_TX	7	B3	B4	OUTDS	GTXE1_X0Y35
MGT_RTM_TX	8	AP3	AP4	OUTDS	GTXE1_X0Y8
MGT_RTM_TX	9	AN1	AN2	OUTDS	GTXE1_X0Y9
MGT_RTM_TX	10	AM3	AM4	OUTDS	GTXE1_X0Y10
MGT_RTM_TX	11	AL1	AL2	OUTDS	GTXE1_X0Y11
MGT_RTM_TX	12	AK3	AK4	OUTDS	GTXE1_X0Y12
MGT_RTM_TX	13	AJ1	AJ2	OUTDS	GTXE1_X0Y13
MGT_RTM_TX	14	AH3	AH4	OUTDS	GTXE1_X0Y14
MGT_RTM_TX	15	AG1	AG2	OUTDS	GTXE1_X0Y15
MGT_RTM_TX	16	AE1	AE2	OUTDS	GTXE1_X0Y16
MGT_RTM_TX	17	AC1	AC2	OUTDS	GTXE1_X0Y17
MGT_RTM_TX	18	AA1	AA2	OUTDS	GTXE1_X0Y18
MGT_RTM_TX	19	W1	W2	OUTDS	GTXE1_X0Y19
MGT_RTM_TX	20	U1	U2	OUTDS	GTXE1_X0Y20
MGT_RTM_TX	21	T3	T4	OUTDS	GTXE1_X0Y21
MGT_RTM_TX	22	R1	R2	OUTDS	GTXE1_X0Y22
MGT_RTM_TX	23	P3	P4	OUTDS	GTXE1_X0Y23
MGT_RTM_TX	24	N1	N2	OUTDS	GTXE1_X0Y24
MGT_RTM_TX	25	M3	M4	OUTDS	GTXE1_X0Y25
MGT_RTM_TX	26	L1	L2	OUTDS	GTXE1_X0Y26
MGT_RTM_TX	27	K3	K4	OUTDS	GTXE1_X0Y27

Pin name	Index	LOC+	LOC–	I/O buffer	GTX address
MGT_RTM_TX	28	J1	J2	OUTDS	GTXE1_X0Y28
MGT_RTM_TX	29	H3	H4	OUTDS	GTXE1_X0Y29
MGT_RTM_TX	30	G1	G2	OUTDS	GTXE1_X0Y30
MGT_RTM_TX	31	F3	F4	OUTDS	GTXE1_X0Y31

Table 11 RTM

DDR3 memory processor FPGA pin assignment

Pin name	Index	LOC+	LOC–	I/O buffer	I/O standard
CCE_DDR3_A	0	E24	–	OUT	SSTL15
CCE_DDR3_A	1	D22	–	OUT	SSTL15
CCE_DDR3_A	2	C24	–	OUT	SSTL15
CCE_DDR3_A	3	H23	–	OUT	SSTL15
CCE_DDR3_A	4	B23	–	OUT	SSTL15
CCE_DDR3_A	5	K20	–	OUT	vSSTL15
CCE_DDR3_A	6	C23	–	OUT	SSTL15
CCE_DDR3_A	7	J21	–	OUT	SSTL15
CCE_DDR3_A	8	B24	–	OUT	SSTL15
CCE_DDR3_A	9	K22	–	OUT	SSTL15
CCE_DDR3_A	10	F21	–	OUT	SSTL15
CCE_DDR3_A	11	A24	–	OUT	SSTL15
CCE_DDR3_A	12	B22	–	OUT	SSTL15
CCE_DDR3_A	13	L21	–	OUT	SSTL15
CCE_DDR3_A	14	D21	–	OUT	SSTL15
CCE_DDR3_BA	0	J20	–	OUT	SSTL15
CCE_DDR3_BA	1	A22	–	OUT	SSTL15

Pin name	Index	LOC+	LOC–	I/O buffer	I/O standard
CCE_DDR3_BA	2	E23	–	OUT	SSTL15
CCE_DDR3_CAS_N	–	G22	–	OUT	SSTL15
CCE_DDR3_CK	–	H20	G21	OUTDS	DIFF_SSTL15
CCE_DDR3_CKE	–	D23	–	OUT	SSTL15
CCE_DDR3_CS_N	–	H21	–	OUT	SSTL15
CCE_DDR3_DQ	–	J16	–	OUT	SSTL15
CCE_DDR3_DQ	0	K18	–	INOUT	SSTL15_T_DCI
CCE_DDR3_DQ	1	G18	–	INOUT	SSTL15_T_DCI
CCE_DDR3_DQ	2	G19	–	INOUT	SSTL15_T_DCI
CCE_DDR3_DQ	3	E18	–	INOUT	SSTL15_T_DCI
CCE_DDR3_DQ	4	H18	–	INOUT	SSTL15_T_DCI
CCE_DDR3_DQ	5	E19	–	INOUT	SSTL15_T_DCI
CCE_DDR3_DQ	6	J18	–	INOUT	SSTL15_T_DCI
CCE_DDR3_DQ	7	F19	–	INOUT	SSTL15_T_DCI
CCE_DDR3_DQS	–	G16	F16	INOUTDS	SSTL15_T_DCI
CCE_DDR3_ODT	–	F22	–	OUT	SSTL15
CCE_DDR3_RAS_N	–	K19	–	OUT	SSTL15
CCE_DDR3_RESET_N	–	L20	–	OUT	SSTL15
CCE_DDR3_WE_N	–	G23	–	OUT	SSTL15

Table 12 DDR3 memory processor

Control FPGA pin assignment

Pin name	LOC	I/O buffer	I/O standard
CTRL_100MHZ_OUT_EN	H14	OUT	LVCMOS25
CTRL_AMCTCLKA_2_FMC_CLK2_EN	N14	OUT	LVCMOS25

Pin name	LOC	I/O buffer	I/O standard
CTRL_AMCTCLKA_2_FMC2_CLK2_EN	M13	OUT	LVCMOS25
CTRL_AMCTCLKC_2_FMC_CLK3_EN	AU16	OUT	LVCMOS25
CTRL_AMCTCLKC_2_FMC2_CLK3_EN	N13	OUT	LVCMOS25
CTRL_FCLKA_HIGHZ	A15	OUT	LVCMOS25
CTRL_MGTREFCLK_125	B14	OUT	LVCMOS25
CTRL_MGTREFCLK_156	C14	OUT	LVCMOS25
CTRL_VADJ_EN	A14	OUT	LVCMOS25
CTRL_VADJ_SEL0	AV34	OUT	LVCMOS25
CTRL_VADJ_SEL1	AV35	OUT	LVCMOS25
CTRL_VADJ2_EN	E15	OUT	LVCMOS25
CTRL_VADJ2_SEL0	AC31	OUT	LVCMOS25
CTRL_VADJ2_SEL1	AC30	OUT	LVCMOS25
DAUGHTER_IO_PRESENT_N	AU34	IN	LVCMOS25
FPGA_PROG_N	M11	OUT	LVCMOS25
I2C_BUS_SEL_0	K12	OUT	LVCMOS25
I2C_BUS_SEL_1	L11	OUT	LVCMOS25
I2C_GNT	AW16	IN	LVCMOS25
I2C_REQ	F15	OUT	LVCMOS25

Table 13 Control pins

DDR3 SODIMM FPGA pin assignment

Pin name	Index	LOC+	LOC–	I/O buffer	I/O standard
DDR3_A	0	D40	–	OUT	SSTL15
DDR3_A	1	G41	–	OUT	SSTL15
DDR3_A	2	G42	–	OUT	SSTL15

Pin name	Index	LOC+	LOC–	I/O buffer	I/O standard
DDR3_A	3	F37	–	OUT	SSTL15
DDR3_A	4	D41	–	OUT	SSTL15
DDR3_A	5	F35	–	OUT	SSTL15
DDR3_A	6	F40	–	OUT	SSTL15
DDR3_A	7	E42	–	OUT	SSTL15
DDR3_A	8	G37	–	OUT	SSTL15
DDR3_A	9	G36	–	OUT	SSTL15
DDR3_A	10	B42	–	OUT	SSTL15
DDR3_A	11	F41	–	OUT	SSTL15
DDR3_A	12	H34	–	OUT	SSTL15
DDR3_A	13	B39	–	OUT	SSTL15
DDR3_A	14	F42	–	OUT	SSTL15
DDR3_A	15	F36	–	OUT	SSTL15
DDR3_BA	0	C41	–	OUT	SSTL15
DDR3_BA	1	A39	–	OUT	SSTL15
DDR3_BA	2	H36	–	OUT	SSTL15
DDR3_CAS_N	–	C40	–	OUTDS	SSTL15
DDR3_CK0	–	E39	E38	OUTDS	DIFF_SSTL15
DDR3_CK1	–	A40	A41	OUT	DIFF_SSTL15
DDR3_CKE0	–	H35	–	OUT	SSTL15
DDR3_CKE1	–	E40	–	OUT	SSTL15
DDR3_DM	0	J38	–	OUT	SSTL15
DDR3_DM	1	K33	–	OUT	SSTL15
DDR3_DM	2	F32	–	OUT	SSTL15
DDR3_DM	3	P28	–	OUT	SSTL15
DDR3_DM	4	E33	–	OUT	SSTL15

Pin name	Index	LOC+	LOC–	I/O buffer	I/O standard
DDR3_DM	5	H30	–	OUT	SSTL15
DDR3_DM	6	B17	–	OUT	SSTL15
DDR3_DM	7	P17	–	OUT	SSTL15
DDR3_DQ	0	M33	–	INOUT	SSTL15_T_DCI
DDR3_DQ	1	L37	–	INOUT	SSTL15_T_DCI
DDR3_DQ	2	H39	–	INOUT	SSTL15_T_DCI
DDR3_DQ	3	J42	–	INOUT	SSTL15_T_DCI
DDR3_DQ	4	M32	–	INOUT	SSTL15_T_DCI
DDR3_DQ	5	M34	–	INOUT	SSTL15_T_DCI
DDR3_DQ	6	H38	–	INOUT	SSTL15_T_DCI
DDR3_DQ	7	K42	–	INOUT	SSTL15_T_DCI
DDR3_DQ	8	J40	–	INOUT	SSTL15_T_DCI
DDR3_DQ	9	H40	–	INOUT	SSTL15_T_DCI
DDR3_DQ	10	L34	–	INOUT	SSTL15_T_DCI
DDR3_DQ	11	L32	–	INOUT	SSTL15_T_DCI
DDR3_DQ	12	H41	–	INOUT	SSTL15_T_DCI
DDR3_DQ	13	J37	–	INOUT	SSTL15_T_DCI
DDR3_DQ	14	K32	–	INOUT	SSTL15_T_DCI
DDR3_DQ	15	L31	–	INOUT	SSTL15_T_DCI
DDR3_DQ	16	F31	–	INOUT	SSTL15_T_DCI
DDR3_DQ	17	D32	–	INOUT	SSTL15_T_DCI
DDR3_DQ	18	B32	–	INOUT	SSTL15_T_DCI
DDR3_DQ	19	A32	–	INOUT	SSTL15_T_DCI
DDR3_DQ	20	E35	–	INOUT	SSTL15_T_DCI
DDR3_DQ	21	E32	–	INOUT	SSTL15_T_DCI

Pin name	Index	LOC+	LOC–	I/O buffer	I/O standard
DDR3_DQ	22	C33	–	INOUT	SSTL15_T_DCI
DDR3_DQ	23	B33	–	INOUT	SSTL15_T_DCI
DDR3_DQ	24	P31	–	INOUT	SSTL15_T_DCI
DDR3_DQ	25	P30	–	INOUT	SSTL15_T_DCI
DDR3_DQ	26	P27	–	INOUT	SSTL15_T_DCI
DDR3_DQ	27	R27	–	INOUT	SSTL15_T_DCI
DDR3_DQ	28	M31	–	INOUT	SSTL15_T_DCI
DDR3_DQ	29	N31	–	INOUT	SSTL15_T_DCI
DDR3_DQ	30	R29	–	INOUT	SSTL15_T_DCI
DDR3_DQ	31	N28	–	INOUT	SSTL15_T_DCI
DDR3_DQ	32	B36	–	INOUT	SSTL15_T_DCI
DDR3_DQ	33	A36	–	INOUT	SSTL15_T_DCI
DDR3_DQ	34	D36	–	INOUT	SSTL15_T_DCI
DDR3_DQ	35	E34	–	INOUT	SSTL15_T_DCI
DDR3_DQ	36	C35	–	INOUT	SSTL15_T_DCI
DDR3_DQ	37	C36	–	INOUT	SSTL15_T_DCI
DDR3_DQ	38	F34	–	INOUT	SSTL15_T_DCI
DDR3_DQ	39	D37	–	INOUT	SSTL15_T_DCI
DDR3_DQ	40	G32	–	INOUT	SSTL15_T_DCI
DDR3_DQ	41	G31	–	INOUT	SSTL15_T_DCI
DDR3_DQ	42	J30	–	INOUT	SSTL15_T_DCI
DDR3_DQ	43	L30	–	INOUT	SSTL15_T_DCI
DDR3_DQ	44	H31	–	INOUT	SSTL15_T_DCI
DDR3_DQ	45	J32	–	INOUT	SSTL15_T_DCI
DDR3_DQ	46	L29	–	INOUT	SSTL15_T_DCI
DDR3_DQ	47	M29	–	INOUT	SSTL15_T_DCI

Pin name	Index	LOC+	LOC–	I/O buffer	I/O standard
DDR3_DQ	48	D18	–	INOUT	SSTL15_T_DCI
DDR3_DQ	49	A19	–	INOUT	SSTL15_T_DCI
DDR3_DQ	50	B18	–	INOUT	SSTL15_T_DCI
DDR3_DQ	51	C18	–	INOUT	SSTL15_T_DCI
DDR3_DQ	52	A17	–	INOUT	SSTL15_T_DCI
DDR3_DQ	53	D17	–	INOUT	SSTL15_T_DCI
DDR3_DQ	54	G17	–	INOUT	SSTL15_T_DCI
DDR3_DQ	55	J17	–	INOUT	SSTL15_T_DCI
DDR3_DQ	56	M17	–	INOUT	SSTL15_T_DCI
DDR3_DQ	57	N15	–	INOUT	SSTL15_T_DCI
DDR3_DQ	58	N18	–	INOUT	SSTL15_T_DCI
DDR3_DQ	59	P16	–	INOUT	SSTL15_T_DCI
DDR3_DQ	60	M16	–	INOUT	SSTL15_T_DCI
DDR3_DQ	61	L17	–	INOUT	SSTL15_T_DCI
DDR3_DQ	62	J15	–	INOUT	SSTL15_T_DCI
DDR3_DQ	63	K17	–	INOUT	SSTL15_T_DCI
DDR3_DQS0	–	L35	L36	INOUTDS	DIFF_SSTL15_T_DCI
DDR3_DQS1	–	K35	K34	INOUTDS	DIFF_SSTL15_T_DCI
DDR3_DQS2	–	A34	A35	INOUTV	DIFF_SSTL15_T_DCI
DDR3_DQS3	–	N29	N30	INOUTDS	DIFF_SSTL15_T_DCI
DDR3_DQS4	–	B34	C34	INOUTDS	DIFF_SSTL15_T_DCI
DDR3_DQS5	–	K29	K30	INOUTDS	DIFF_SSTL15_T_DCI
DDR3_DQS6	–	C19	B19	INOUTDS	DIFF_SSTL15_T_DCI
DDR3_DQS7	–	L16	L15	INOUTDS	DIFF_SSTL15_T_DCI
DDR3_EVENT_N	–	C38	–	OUT	SSTL15

Pin name	Index	LOC+	LOC–	I/O buffer	I/O standard
DDR3_ODT	0	A37	–	OUT	SSTL15
DDR3_ODT	1	B37	–	OUT	SSTL15
DDR3_RAS_N	–	B38	–	OUT	SSTL15
DDR3_REFCLK	–	L12	M12	INDS	SSTL15
DDR3_RESET_N	–	J35	–	OUT	SSTL15
DDR3_S0_N	–	D38	–	OUT	SSTL15
DDR3_S1_N	–	C39	–	OUT	SSTL15
DDR3_SCL	–	C20	–	INOUT	SSTL15
DDR3_SDA	–	D20	–	INOUT	SSTL15
DDR3_VREF	–	D32, E22, H16, H19, J31, K15, E37, G38, J36, J41,	–	IN	SSTL15
DDR3_WE_N	–	B41	–	OUT	SSTL15

Table 14 DDR3 SODIMM

DPIO Connector FPGA pin assignment

Pin name	Index	LOC+	LOC–	I/O buffer	I/O standard
DPIO	0	AY38	AY37	INOUTDS	LVDS_25
DPIO	1	AY39	BA39	INOUTDS	LVDS_25
DPIO	2	AW37	AW38	INOUTDS	LVDS_25
DPIO	3	AV39	AV38	INOUTDS	LVDS_25
DPIO	4	AU37	AU38	INOUTDS	LVDS_25
DPIO	5	AT37	AR38	INOUTDS	LVDS_25
DPIO	6	AU36	AT36	INOUTDS	LVDS_25
DPIO	7	AR35	AT35	INOUTDS	LVDS_25
DPIO	8	AP37	AR37	INOUTDS	LVDS_25
DPIO	9	AN35	AN36	INOUTDS	LVDS_25

Pin name	Index	LOC+	LOC–	I/O buffer	I/O standard
DPIO	10	BA37	BB37	INOUTDS	LVDS_25
DPIO	11	BB39	BB38	INOUTDS	LVDS_25
DPIO	12	BB36	BA36	INOUTDS	LVDS_25
DPIO	13	AW36	AV36	INOUTDS	LVDS_25
DPIO_CLK	–	AP36	AP35	INOUTDS	LVDS_25

Table 15 DPIO connector

Backplane clocks FPGA pin assignment

Pin name	LOC+	LOC–	I/O buffer	I/O standard
FCLKA_IN	AB8	AB7	INOUTDS	BYPASS
TCLKA	AN14	AN13	INDS	LVDS_25
TCLKB	J12	J11	INOUTDS	LVDS_25
TCLKC	AM13	AM12	INDS	LVDS_25
TCLKD	AV13	AV14	INOUTDS	LVDS_25

Table 16 Backplane clocks

Flash memory FPGA pin assignment

Pin name	Index	LOC+	I/O buffer	I/O standard	Resistor
FLASH_A	0	AW13	OUT	LVCMOS25_F_8	–
FLASH_A	1	AW12	OUT	LVCMOS25_F_8	–
FLASH_A	2	BB14	OUT	LVCMOS25_F_8	–
FLASH_A	3	BB13	OUT	LVCMOS25_F_8	–
FLASH_A	4	AU13	OUT	LVCMOS25_F_8	–
FLASH_A	5	AU12	OUT	LVCMOS25_F_8	–
FLASH_A	6	AW15	OUT	LVCMOS25_F_8	–

Pin name	Index	LOC+	I/O buffer	I/O standard	Resistor
FLASH_A	7	AY15	OUT	LVCMOS25_F_8	–
FLASH_A	8	AR13	OUT	LVCMOS25_F_8	–
FLASH_A	9	AP13	OUT	LVCMOS25_F_8	–
FLASH_A	10	AU14	OUT	LVCMOS25_F_8	–
FLASH_A	11	AV15	OUT	LVCMOS25_F_8	–
FLASH_A	12	AT12	OUT	LVCMOS25_F_8	–
FLASH_A	13	AR12	OUT	LVCMOS25_F_8	–
FLASH_A	14	BA14	OUT	LVCMOS25_F_8	–
FLASH_A	15	BA15	OUT	LVCMOS25_F_8	–
FLASH_A	16	AW17	OUT	LVCMOS25_F_8	–
FLASH_A	17	AY17	OUT	LVCMOS25_F_8	–
FLASH_A	18	AR15	OUT	LVCMOS25_F_8	–
FLASH_A	19	AP15	OUT	LVCMOS25_F_8	–
FLASH_A	20	BB17	OUT	LVCMOS25_F_8	–
FLASH_A	21	BB16	OUT	LVCMOS25_F_8	–
FLASH_A	22	AT14	OUT	LVCMOS25_F_8	–
FLASH_A	23	AR14	OUT	LVCMOS25_F_8	–
FLASH_A	24	BA17	OUT	LVCMOS25_F_8	–
FLASH_A	25	BA16	OUT	LVCMOS25_F_8	–
FLASH_A	26	AT15	OUT	LVCMOS25_F_8	–
FLASH_CE_N	–	AH30	OUT	LVCMOS25	–
FLASH_DQ	0	U31	INOUT	LVCMOS25_F_12	PULLDOWN
FLASH_DQ	1	T31	INOUT	LVCMOS25_F_12	PULLDOWN
FLASH_DQ	2	AL32	INOUT	LVCMOS25_F_12	PULLDOWN
FLASH_DQ	3	AK32	INOUT	LVCMOS25_F_12	PULLDOWN
FLASH_DQ	4	R33	INOUT	LVCMOS25_F_12	PULLDOWN

Pin name	Index	LOC+	I/O buffer	I/O standard	Resistor
FLASH_DQ	5	P32	INOUT	LVCMOS25_F_12	PULLDOWN
FLASH_DQ	6	AH33	INOUT	LVCMOS25_F_12	PULLDOWN
FLASH_DQ	7	AJ33	INOUT	LVCMOS25_F_12	PULLDOWN
FLASH_DQ	8	P33	INOUT	LVCMOS25_F_12	PULLDOWN
FLASH_DQ	9	N33	INOUT	LVCMOS25_F_12	PULLDOWN
FLASH_DQ	10	AG31	INOUT	LVCMOS25_F_12	PULLDOWN
FLASH_DQ	11	AH31	INOUT	LVCMOS25_F_12	PULLDOWN
FLASH_DQ	12	R30	INOUT	LVCMOS25_F_12	PULLDOWN
FLASH_DQ	13	T30	INOUT	LVCMOS25_F_12	PULLDOWN
FLASH_DQ	14	AF31	INOUT	LVCMOS25_F_12	PULLDOWN
FLASH_DQ	15	AG32	INOUT	LVCMOS25_F_12	PULLDOWN
FLASH_OE_N	–	AJ30	OUT	LVCMOS25_F_12	–
FLASH_RST_N	–	AH29	OUT	LVCMOS25_F_12	–
FLASH_WE_N	–	V31	OUT	LVCMOS25_F_12	–

Table 17 Flash memory

200 MHz reference clock FPGA pin assignment

Pin name	LOC+	LOC–	I/O buffer	I/O standard
IODELAY_REFCLK	E14	F14	INDS	LVDS_25

Table 18 200 MHz reference clock

GTX reference clocks FPGA pin assignment

Pin name	LOC+	LOC–	I/O buffer	I/O standard
MGTAVTTRCAL	A12	–	IN	BYPASS
MGTRREF	B11	–	IN	BYPASS

Pin name	LOC+	LOC–	I/O buffer	I/O standard
MGTREFCLK_IN_150M	BA10	BA9	INDS	BYPASS
MGTREFCLK110_1_F_125M	AW10	AW9	INDS	BYPASS
MGTREFCLK111_0_F_156M25	AU10	AU9	INDS	BYPASS
MGTREFCLK1_111	AT8	AT7	INDS	BYPASS
MGTREFCLK112_F_0_156M25	AK8	AK7	INDS	BYPASS
MGTREFCLK112_F_1_125M	AH8	AH7	INDS	BYPASS
MGTREFCLK113_0_F_156M25	AF8	AF7	INDS	BYPASS
MGTREFCLK113_1_F_125M	AD8	AD7	INDS	BYPASS
FCLKA_IN	AB8	AB7	INDS	BYPASS
MGTREFCLK2_IN_100M	Y8	Y7	INDS	BYPASS
MGTREFCLK115_0_F_156M25	AF8	AF7	INDS	BYPASS
MGTREFCLK115_1_F_125M	AD8	AD7	INDS	BYPASS
MGTREFCLK116_F_0_156M25	M8	M7	INDS	BYPASS
MGTREFCLK116_F_1_125M	K8	K7	INDS	BYPASS
MGTREFCLK117_0_F_156M25	G10	G9	INDS	BYPASS
MGTREFCLK117_1_F_125M	E10	E9	INDS	BYPASS
MGTREFCLK1_118	AT8	AT7	INDS	BYPASS

Table 19 GTX reference clocks

RTM USB UART interface FPGA pin assignment

Pin name	LOC+	I/O buffer	I/O standard
FPGA_UBLAZE_RXD1	AG29	IN	LVCMOS25
FPGA_UBLAZE_TXD1	AD31	OUT	LVCMOS25

Table 20 RTM USB UART interface

2.5 FMC Connectors Pin Assignments

This section presents information specific to the Perseus611x FMC connectors.

2.5.1 FMC1 Connector Pin Assignments

Unconnected pins are not presented in the following table.

Pin name	Index	LOC+	LOC–	I/O buffer	Function
FMC_ABSENT	–	AT34	–	IN	LVCMOS25
FMC1_CLK0_M2C	–	AE30	AF30	INDS	APP/SPEC
FMC1_CLK1_M2C	–	Y30	AA30	INDS	APP/SPEC
FMC1_CLK2_BIDIR	–	AP11	AP12	INOUTDS	APP/SPEC
FMC1_CLK3_BIDIR	–	AK33	AJ32	INOUTDS	APP/SPEC
FMC1_HA	0	AH34	AJ35	INOUTDS	MRCC 14
FMC1_HA	1	AJ37	AK37	INOUTDS	MRCC 14
FMC1_HA	2	AC34	AC33	INOUTDS	APP/SPEC
FMC1_HA	3	AE40	AE39	INOUTDS	APP/SPEC
FMC1_HA	4	AG34	AF34	INOUTDS	APP/SPEC
FMC1_HA	5	AF40	AG41	INOUTDS	APP/SPEC
FMC1_HA	6	AF39	AG39	INOUTDS	APP/SPEC
FMC1_HA	7	AG42	AH41	INOUTDS	APP/SPEC
FMC1_HA	8	AH40	AJ41	INOUTDS	APP/SPEC
FMC1_HA	9	AF37	AG37	INOUTDS	APP/SPEC
FMC1_HA	10	AJ42	AK42	INOUTDS	APP/SPEC
FMC1_HA	11	AK38	AJ38	INOUTDS	SRCC 14
FMC1_HA	12	AJ36	AH35	INOUTDS	VRN/VRP 14
FMC1_HA	13	AL42	AM42	INOUTDS	APP/SPEC
FMC1_HA	14	AL41	AM41	INOUTDS	APP/SPEC

Pin name	Index	LOC+	LOC–	I/O buffer	Function
FMC1_HA	15	AF35	AF36	INOUTDS	APP/SPEC
FMC1_HA	16	AK40	AL40	INOUTDS	APP/SPEC
FMC1_HA	17	AH39	AJ40	INOUTDS	SRCC 14
FMC1_HA	18	AF32	AG33	INOUTDS	APP/SPEC
FMC1_HA	19	AK39	AL39	INOUTDS	APP/SPEC
FMC1_HA	20	AL34	AK34	INOUTDS	MRCC 13
FMC1_HA	21	AK35	AL36	INOUTDS	APP/SPEC
FMC1_HA	22	AM37	AM36	INOUTDS	APP/SPEC
FMC1_HA	23	AN38	AP38	INOUTDS	VRN/VRP 13
FMC1_HB	0	R39	P38	INOUTDS	SRCC 17
FMC1_HB	1	M36	M37	INOUTDS	APP/SPEC
FMC1_HB	2	L39	L40	INOUTDS	APP/SPEC
FMC1_HB	3	M38	M39	INOUTDS	APP/SPEC
FMC1_HB	4	L41	L42	INOUTDS	APP/SPEC
FMC1_HB	5	N38	N39	INOUTDS	APP/SPEC
FMC1_HB	6	P36	P35	INOUTDS	MRCC 17
FMC1_HB	7	N36	P37	INOUTDS	APP/SPEC
FMC1_HB	8	M41	M42	INOUTDS	APP/SPEC
FMC1_HB	9	N40	N41	INOUTDS	SRCC 17
FMC1_HB	10	R37	T37	INOUTDS	VRN/VRP 17
FMC1_HB	11	P40	P41	INOUTDS	APP/SPEC
FMC1_HB	12	P42	R42	INOUTDS	APP/SPEC
FMC1_HB	13	U36	T36	INOUTDS	APP/SPEC
FMC1_HB	14	R40	T40	INOUTDS	APP/SPEC
FMC1_HB	15	T34	T35	INOUTDS	APP/SPEC
FMC1_HB	16	T41	T42	INOUTDS	APP/SPEC

Pin name	Index	LOC+	LOC–	I/O buffer	Function
FMC1_HB	17	T39	R38	INOUTDS	MRCC 17
FMC1_HB	18	J27	J26	INOUTDS	APP/SPEC
FMC1_HB	19	D28	D29	INOUTDS	APP/SPEC
FMC1_HB	20	G28	G27	INOUTDS	APP/SPEC
FMC1_HB	21	E30	F30	INOUTDS	APP/SPEC
FMC1_LA	0	AD32	AE32	INOUTDS	MRCC 15
FMC1_LA	1	AE37	AD37	INOUTDS	MRCC 15
FMC1_LA	2	AE34	AE35	INOUTDS	APP/SPEC
FMC1_LA	3	AF42	AF41	INOUTDS	APP/SPEC
FMC1_LA	4	AE33	AD33	INOUTDS	APP/SPEC
FMC1_LA	5	AB39	AA40	INOUTDS	APP/SPEC
FMC1_LA	6	AA41	AB41	INOUTDS	APP/SPEC
FMC1_LA	7	AC41	AD41	INOUTDS	SRCC 15
FMC1_LA	8	AD42	AE42	INOUTDS	APP/SPEC
FMC1_LA	9	AC36	AB36	INOUTDS	SRCC 15
FMC1_LA	10	AA42	AB42	INOUTDS	APP/SPEC
FMC1_LA	11	AE38	AD38	INOUTDS	APP/SPEC
FMC1_LA	12	AC40	AD40	INOUTDS	APP/SPEC
FMC1_LA	13	AB32	AB33	INOUTDS	APP/SPEC
FMC1_LA	14	AC35	AB34	INOUTDS	VRN/VRP 15
FMC1_LA	15	AB37	AB38	INOUTDS	APP/SPEC
FMC1_LA	16	W37	Y37	INOUTDS	APP/SPEC
FMC1_LA	17	W32	Y33	INOUTDS	MRCC 16
FMC1_LA	18	V34	U34	INOUTDS	MRCC 16
FMC1_LA	19	Y38	AA39	INOUTDS	APP/SPEC

Pin name	Index	LOC+	LOC–	I/O buffer	Function
FMC1_LA	20	W42	Y42	INOUTDS	APP/SPEC
FMC1_LA	21	W35	V35	INOUTDS	APP/SPEC
FMC1_LA	22	Y40	Y39	INOUTDS	APP/SPEC
FMC1_LA	23	V40	W40	INOUTDS	SRCC 16
FMC1_LA	24	V38	W38	INOUTDS	APP/SPEC
FMC1_LA	25	AA35	Y35	INOUTDS	SRCC 16
FMC1_LA	26	V41	W41	INOUTDS	APP/SPEC
FMC1_LA	27	U39	V39	INOUTDS	APP/SPEC
FMC1_LA	28	U42	U41	INOUTDS	APP/SPEC
FMC1_LA	29	W36	V36	INOUTDS	APP/SPEC
FMC1_LA	30	V33	W33	INOUTDS	APP/SPEC
FMC1_LA	31	U37	U38	INOUTDS	APP/SPEC
FMC1_LA	32	U32	U33	INOUTDS	APP/SPEC
FMC1_LA	33	AA32	Y32	INOUTDS	VRN/VRP 16
FMC1_SCL	–	BA35	–	INOUT	LVCMOS25
FMC1_SDA	–	AY35	–	INOUT	LVCMOS25
FMC1_VREF_A_M2C	–	Y34/AA37 AC39/AD35 AH36/AH38	–	ANALOG	N/A
FMC1_VREF_B_M2C	–	N34/R34	–	ANALOG	N/A

Table 21 FMC1 (J5) pin assignment

2.5.2 FMC2 Connector Pin Assignments

Pin name	Index	LOC+	LOC–	I/O buffer	Function
FMC2_ABSENT	–	AD30	–	IN	LVCMOS25
FMC2_CLK0_M2C	–	W30	V30	INDS	APP/SPEC
FMC2_CLK1_M2C	–	AA31	AB31	INDS	APP/SPEC

Pin name	Index	LOC+	LOC–	I/O buffer	Function
FMC2_CLK2_BIDIR	–	AY14	AY13	INOUTDS	APP/SPEC
FMC2_CLK3_BIDIR	–	R32	T32	INOUTDS	APP/SPEC
FMC2_HA	0	AJ21	AJ20	INOUTDS	MRCC 32
FMC2_HA	1	AK20	AK19	INOUTDS	MRCC 32
FMC2_HA	2	AK18	AJ18	INOUTDS	APP/SPEC
FMC2_HA	3	AU19	AT19	INOUTDS	APP/SPEC
FMC2_HA	4	AY24	BA24	INOUTDS	APP/SPEC
FMC2_HA	5	AL19	AM19	INOUTDS	APP/SPEC
FMC2_HA	6	AV23	AU22	INOUTDS	APP/SPEC
FMC2_HA	7	AT20	AR20	INOUTDS	APP/SPEC
FMC2_HA	8	AL20	AL21	INOUTDS	APP/SPEC
FMC2_HA	9	BB24	BB23	INOUTDS	APP/SPEC
FMC2_HA	10	AN20	AP20	INOUTDS	APP/SPEC
FMC2_HA	11	AY20	BA20	INOUTDS	SRCC 32
FMC2_HA	12	AV21	AW21	INOUTDS	VRN/VRP 32
FMC2_HA	13	AV20	AW20	INOUTDS	APP/SPEC
FMC2_HA	14	AU21	AT21	INOUTDS	APP/SPEC
FMC2_HA	15	AW22	AY22	INOUTDS	APP/SPEC
FMC2_HA	16	AT22	AR22	INOUTDS	APP/SPEC
FMC2_HA	17	AM21	AN21	INOUTDS	SRCC 32
FMC2_HA	18	BB22	BB21	INOUTDS	APP/SPEC
FMC2_HA	19	AP21	AP22	INOUTDS	APP/SPEC
FMC2_HA	20	AJ25	AK25	INOUTDS	MRCC 23
FMC2_HA	21	AV33	AW33	INOUTDS	APP/SPEC
FMC2_HA	22	AU33	AU32	INOUTDS	APP/SPEC

Pin name	Index	LOC+	LOC–	I/O buffer	Function
FMC2_HA	23	AP32	AR32	INOUTDS	APP/SPEC
FMC2_HB	0	BA30	AY30	INOUTDS	SRCC 22
FMC2_HB	1	AW30	AV30	INOUTDS	APP/SPEC
FMC2_HB	2	AN26	AP27	INOUTDS	APP/SPEC
FMC2_HB	3	AW31	AV31	INOUTDS	APP/SPEC
FMC2_HB	4	AR28	AP28	INOUTDS	APP/SPEC
FMC2_HB	5	AT29	AR29	INOUTDS	APP/SPEC
FMC2_HB	6	AM26	AL26	INOUTDS	MRCC 22
FMC2_HB	7	BA32	AY33	INOUTDS	APP/SPEC
FMC2_HB	8	AT30	AR30	INOUTDS	APP/SPEC
FMC2_HB	9	AR27	AT27	INOUTDS	SRCC 22
FMC2_HB	10	AY29	BA29	INOUTDS	VRN/VRP 22
FMC2_HB	11	AT31	AU31	INOUTDS	APP/SPEC
FMC2_HB	12	AU29	AV29	INOUTDS	APP/SPEC
FMC2_HB	13	BA31	BB31	INOUTDS	APP/SPEC
FMC2_HB	14	AU28	AV28	INOUTDS	APP/SPEC
FMC2_HB	15	BB29	BB28	INOUTDS	APP/SPEC
FMC2_HB	16	AW28	AY28	INOUTDS	APP/SPEC
FMC2_HB	17	AN28	AM27	INOUTDS	MRCC 22
FMC2_HB	18	H24	G24	INOUTDS	APP/SPEC
FMC2_HB	19	E27	D27	INOUTDS	APP/SPEC
FMC2_HB	20	F25	F24	INOUTDS	APP/SPEC
FMC2_HB	21	C28	B28	INOUTDS	APP/SPEC
FMC2_LA	0	AK15	AK14	INOUTDS	MRCC 33
FMC2_LA	1	AJ16	AJ15	INOUTDS	MRCC 33
FMC2_LA	2	AL15	AL14	INOUTDS	APP/SPEC

Pin name	Index	LOC+	LOC–	I/O buffer	Function
FMC2_LA	3	BA19	AY19	INOUTDS	APP/SPEC
FMC2_LA	4	AN15	AM14	INOUTDS	APP/SPEC
FMC2_LA	5	AT16	AU17	INOUTDS	APP/SPEC
FMC2_LA	6	AT17	AU18	INOUTDS	APP/SPEC
FMC2_LA	7	AP18	AR19	INOUTDS	SRCC 33
FMC2_LA	8	BB18	BB19	INOUTDS	APP/SPEC
FMC2_LA	9	AN16	AM16	INOUTDS	SRCC 33
FMC2_LA	10	AY18	AW18	INOUTDS	APP/SPEC
FMC2_LA	11	AJ17	AK17	INOUTDS	APP/SPEC
FMC2_LA	12	AV18	AV19	INOUTDS	APP/SPEC
FMC2_LA	13	AP16	AP17	INOUTDS	VRN/VRP 33
FMC2_LA	14	AN18	AN19	INOUTDS	APP/SPEC
FMC2_LA	15	AR17	AR18	INOUTDS	APP/SPEC
FMC2_LA	16	AT26	AU27	INOUTDS	APP/SPEC
FMC2_LA	17	AP25	AP26	INOUTDS	MRCC 21
FMC2_LA	18	AK24	AL25	INOUTDS	MRCC 21
FMC2_LA	19	AT25	AR25	INOUTDS	APP/SPEC
FMC2_LA	20	AN24	AN25	INOUTDS	APP/SPEC
FMC2_LA	21	BB26	BB27	INOUTDS	APP/SPEC
FMC2_LA	22	AR24	AT24	INOUTDS	APP/SPEC
FMC2_LA	23	AP23	AR23	INOUTDS	SRCC 21
FMC2_LA	24	AM23	AN23	INOUTDS	APP/SPEC
FMC2_LA	25	AU23	AU24	INOUTDS	SRCC 21
FMC2_LA	26	AM24	AL24	INOUTDS	APP/SPEC
FMC2_LA	27	AJ23	AK23	INOUTDS	APP/SPEC

Pin name	Index	LOC+	LOC–	I/O buffer	Function
FMC2_LA	28	AM22	AL22	INOUTDS	APP/SPEC
FMC2_LA	29	AY27	AW27	INOUTDS	APP/SPEC
FMC2_LA	30	AW25	AW26	INOUTDS	APP/SPEC
FMC2_LA	31	AK22	AJ22	INOUTDS	APP/SPEC
FMC2_LA	32	AV26	AU26	INOUTDS	APP/SPEC
FMC2_LA	33	AV24	AV25	INOUTDS	VRN/VRP 21
FMC2_SCL	–	BA35	–	INOUT	LVCMOS25
FMC2_SDA	–	AY35	–	INOUT	LVCMOS25
FMC2_VREF_A_M2C	–	AL16/AM18/ AY23/BA21/ AY25/BA27	–	ANALOG	N/A
FMC2_VREF_B_M2C	–	AW32/BB32	–	ANALOG	N/A

Table 22 FMC2 (J6) pin assignment

3 Specifications

This chapter presents the main technical specifications of the Perseus611X.

Note:
The specifications presented here are subject to change without notice.

3.1 Mechanical Specifications

This section shows drawings of different views of the Perseus611x board and displays dimensions from different angles.

3.1.1 Board Dimensions

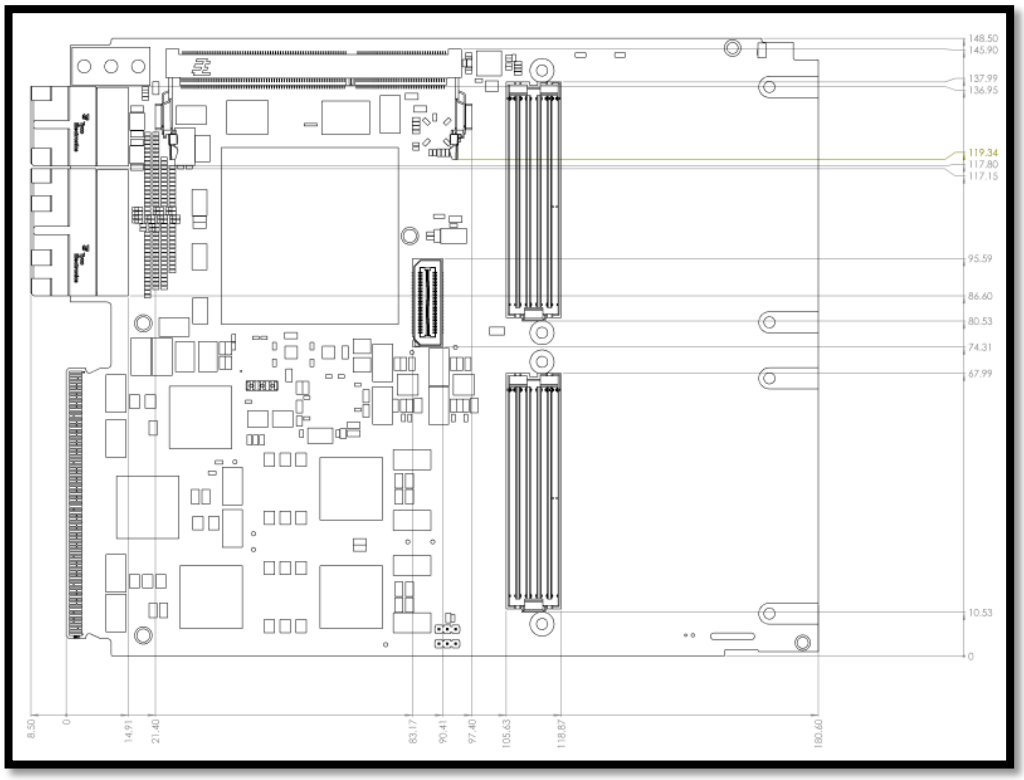

Figure 3-1 Top dimensions in mm (without added parts)

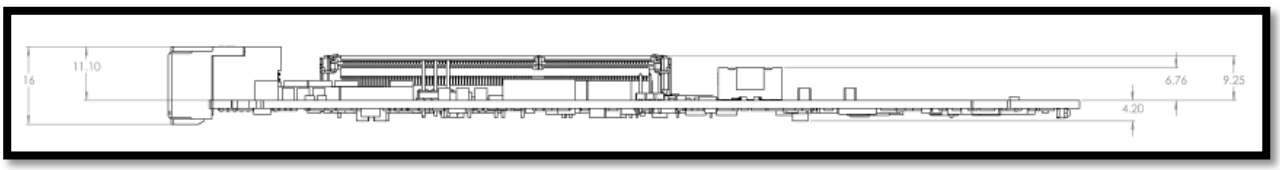

Figure 3-2 Side dimensions in mm (without added parts)

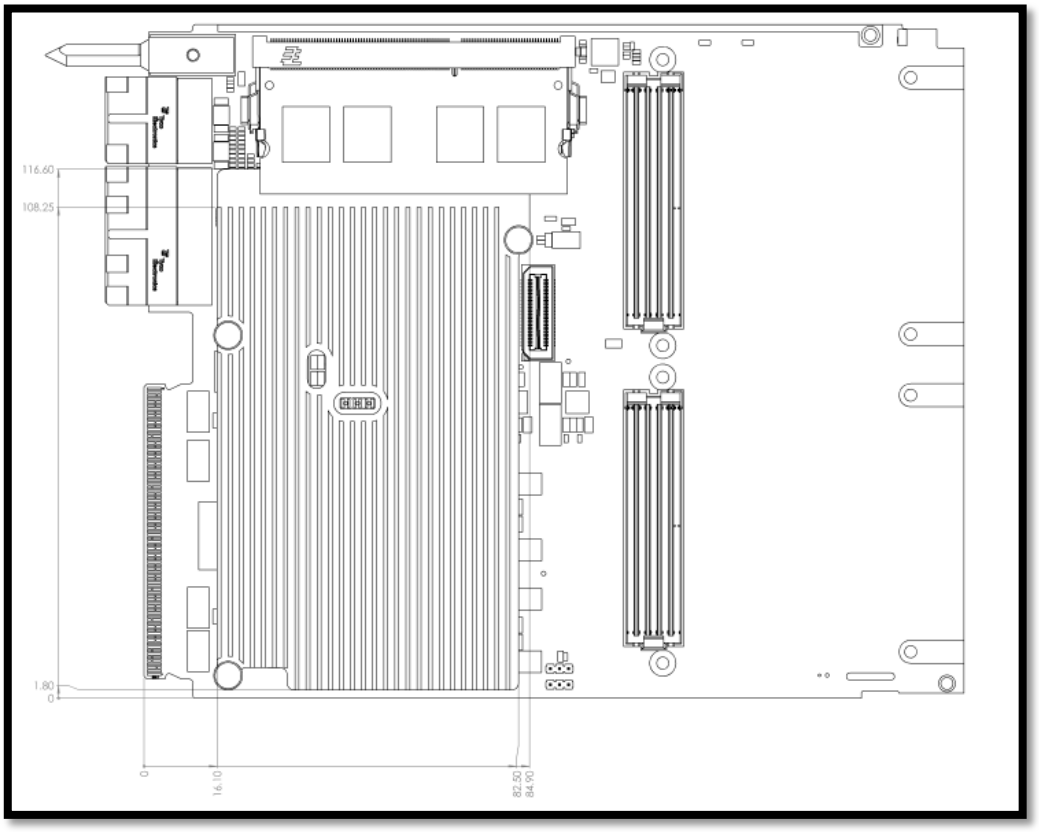

Figure 3-3 Top dimensions in mm (with added parts)

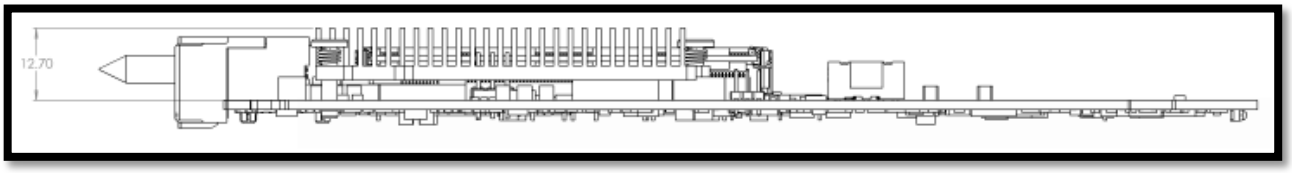

Figure 3-4 Side dimensions in mm (with added parts)

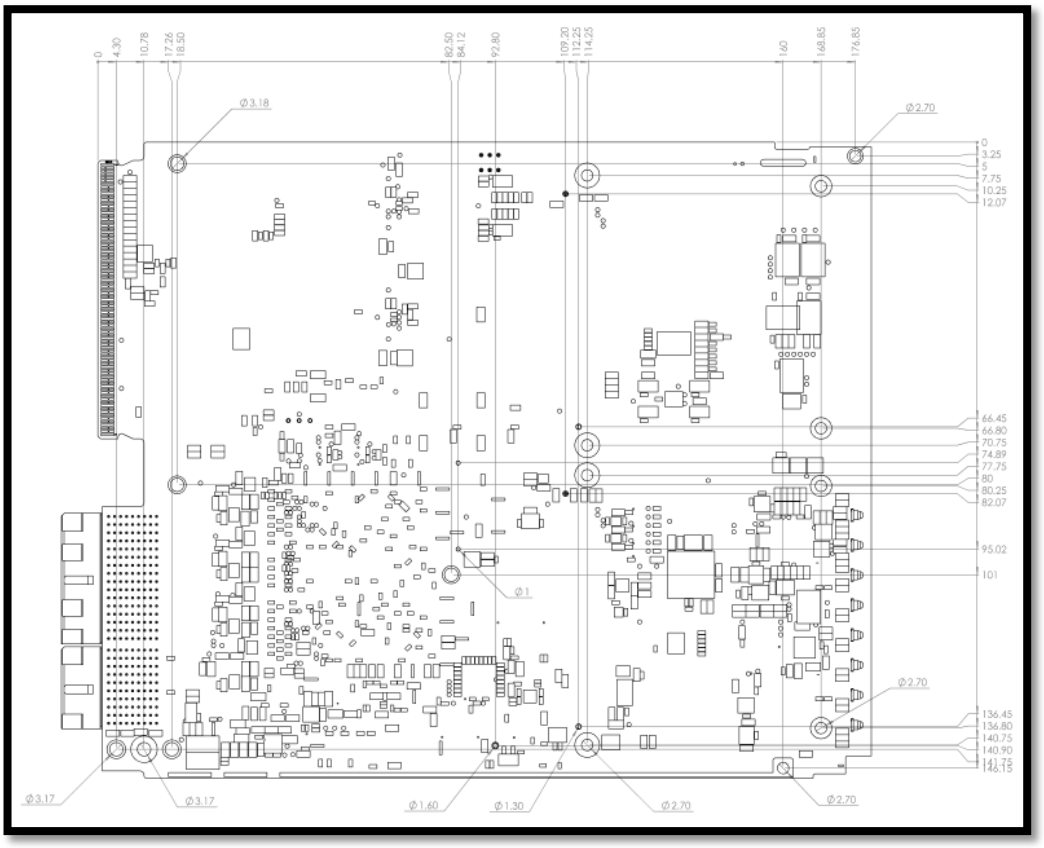

Figure 3-5 Bottom dimensions in mm