10-Bit, XX KSPS[a], SAR ADC

1 Features

- Dual Power Supply With 1.8 V, 3.3 V
- Track and Hold
- Off-chip Controller
- 10-Bit Parallel Interface
- 2.5 V Single-Ended Input Span
- SNR[b]: XX dB
- THD[b]: XX dB
- SINAD[b]: XX dB
- SFDR[b]: XX dB
- ENOB[b]: XX Bits
- Idle-Power Consumption (CLK is off):
  - 3.3-V Supply: XX mW (Typical)
  - 1.8-V Supply: XX nW (Typical)

2 Applications

- Wearable Systems
- Data Acquisition Systems
- Instrumentation and Control Systems
- DSP front ends Systems

3 Description

The EF_ADCS1001NC is a low-power, single-channel CMOS 10-bit analogue-to-digital converter with a flexible parallel interface. It has off-chip SAR controller. The converter is based on a successive-approximation register (SAR) architecture with an internal track-and-hold circuit. It can be configured to accept a 2.5 V single-ended input span. The output parallel data is binary and compatible with many common DSP parallel interfaces. The EF_ADCS1001NC operates with a dual power supply; 1.8 V and 3.3 V supply the digital and analogue IP blocks, respectively. Normal power consumption reaches XX mW in idle mode.

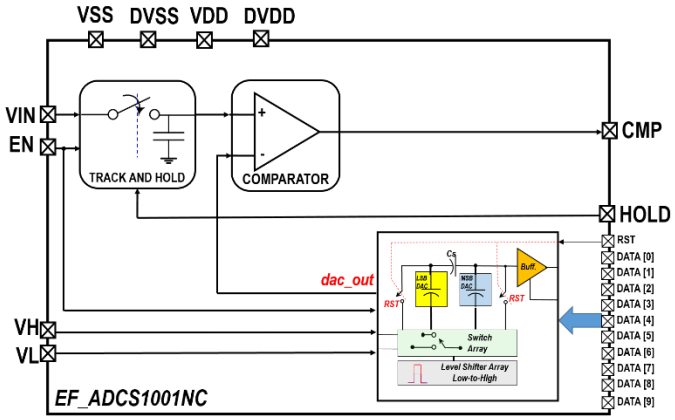


Figure 1. Functional Block Diagram

a: *Produces ENOB at ~X Bits*

b: *Input Sinusoidal of XX kHz, Clock Frequency of X , Sampling frequency of XX KHz.*

Pin Configuration and Functions

Pin's Name	I/O	Description
VDD	Supply	Positive power supply voltage for analog IP block, 3.3 V
DVDD	Supply	Positive power supply voltage for analog IP block, 1.8 V
VIN	Analog input	Single-ended analog input channel. The input range is 0 V to VDD.
EN	Digital input (1.8 V)	It is to enable track/hold and DAC operation. It would be 0V at Idle mode.
VH	Analog input	Positive terminal of reference input, typically VDD.
VL	Analog input	Negative terminal of reference input, typically 0 V.
DATA[0]-DATA[9]	Digital Input (1.8 V)	Digital data Input.
DVSS	Supply	Digital ground.
VSS	Supply	Analog ground.
CMP	Digital Output (1.8V)	Digital data output.
HOLD	Digital Input (1.8 V)	Digital data input.
RST	Digital Input (1.8 V)	Digital reset input for the split-capacitive array

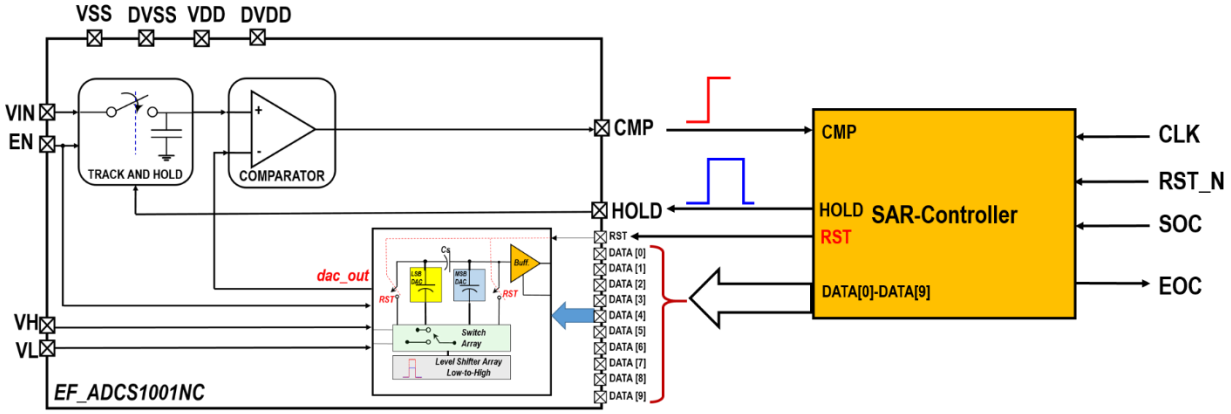


Figure 2. Typical Connection

Noted: *Typically, EN is connected to digital input of 1.8 V, VH represents the reference voltage of ADC, and VL is connected to 0V. VDD and DVDD are connected to 3.3V and 1.8V. VSS and DVSS are connected to 0 V. CLK, RST_N, SOC are set as described in the blow timing diagram.*

4 Timing Characteristics

According to Fig. 2, a controller should be connected as an interface to the EF_ADCS1001NC and satisfy the next timing diagram.

Parameters	Min	Typical	Max	Units
f_{CLK} : CLK frequency		-	1[a]	MHz
t_{CYCLE} :Cycle time	11* t_{CLK}			µs
$t_{D,RST}$:Delay time of RST_N	4.25* t_{CLK}			µs
$t_{D,SOC}$: Delay time of SOC	6.25* t_{CLK}			µs
$t_{PH,SOC}$: High time of SOC	t_{CLK}			µs
$t_{PH,EOC}$: High time of EOC		t_{CLK}		µs
t_{ACQ}: Data Acquisition time	t_{CLK}			µs
T_{CONV}: Conversion time		8* t_{CLK}		µs
T_{IDLE}: IDEL time	-	-	-	µs
t_{RST} :Delay time of RST	5* t_{CLK}			µs

[a]: *Produces ENOB at XX Bits*

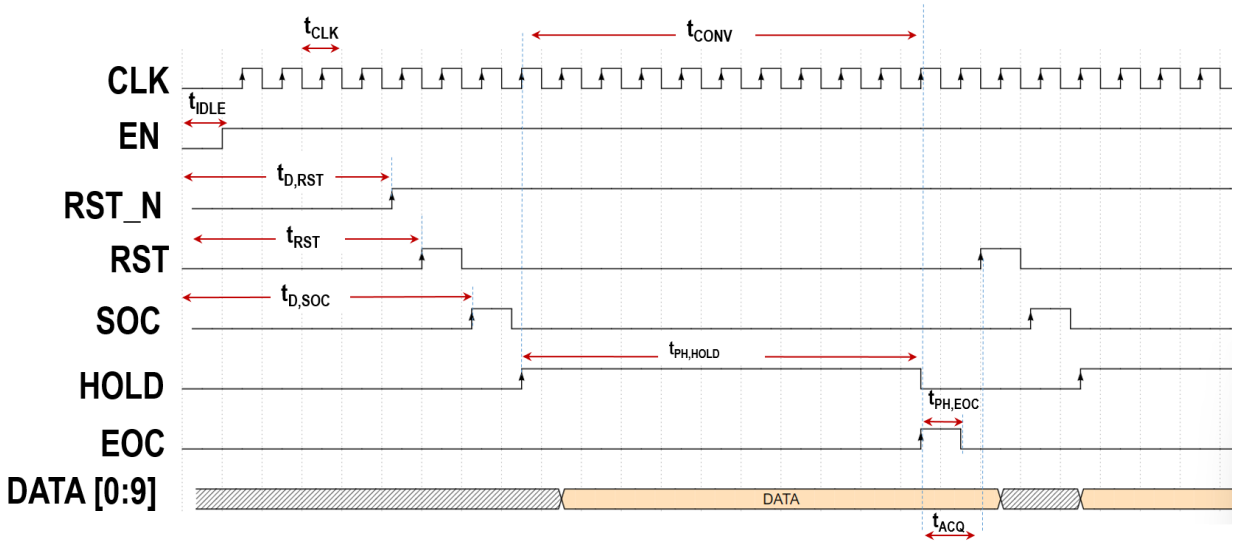


Figure 3. Timing Diagram

5 Electrical Characteristics

The listed parameters are reported at room temperature (27°C), VDD of 3.3V, and DVDD of 1.8V, EN=1.8V, *VH=2.5 V,and VL=0V.*

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
VDD	Power Supply Voltage (Analog Core)					V
DVDD	Power Supply Voltage (Digital Core)					
	Analog Input Range		0		2.5	
N	Resolution					Bits
SNR	Signal-to-Noise Ratio	CLK=XMHz, fin=XXX Hz, NFFT=XX, Ncyc=X				dB
THD	Total Harmonic Distortion					
SINAD	Signal-to-Noise and Distortion					
SFDR	Spurious-Free Dynamic Range					
	Noise Floor					
ENOB	Effective Number Of Bit					Bits
	IDL power consumption	CLK=0V, RST_N=0V, SOC=0V, EN=0V, VH=0V,VL=0V, VIN=0V,				mW
						nW
	Core Silicon Area	SKYWATER130		173x438		μm^2

6 Typical Performance Curves

6.1 Transit and FFT Result

Figure 4. Constructed signal and its spectrum.

7 SAR-ADC Layout

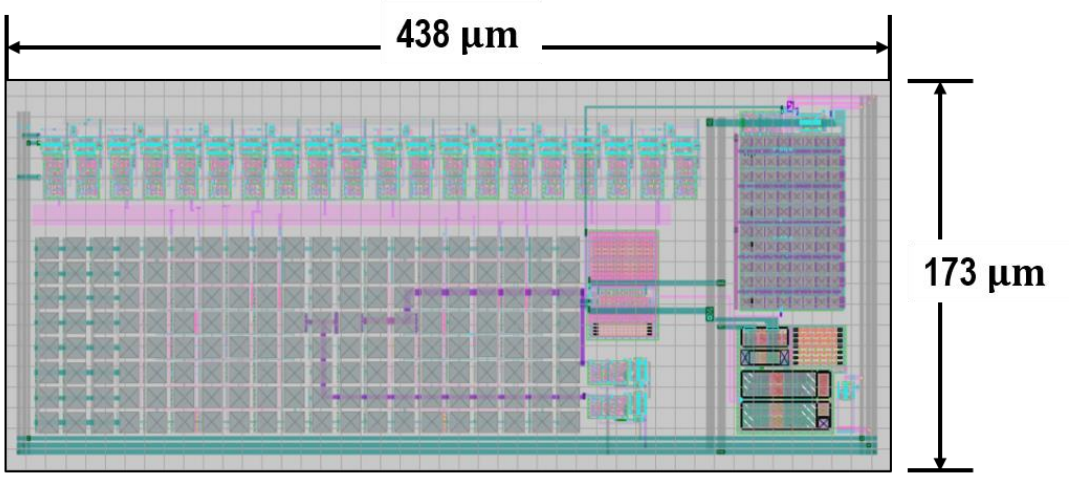
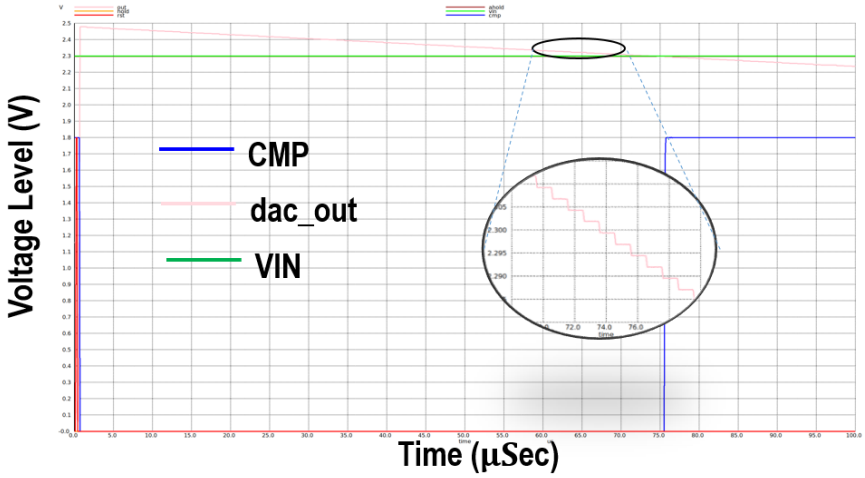


Figure 5. EF_ADCS1001NC's Layout

8 Supplementary Results

This section indicates the functionality of the EF_ADCS1001C is verified when simulating the extracted spice.



(a)

Figure 6. Post layout simulation results