# 10-Bit SAR Analog-Digital-Converter

## 1 Features

- Dual Power Supply With 1.8 V, 3.3 V
- Track and Hold
- Off-chip Controller
- 10-Bit Parallel Interface
- 2.5 V Single-Ended Input Span

## 3 Description

The EF_ADCS1001NC is a low-power, single-channel CMOS 10-bit analogue-to-digital converter with a flexible parallel interface. It has off-chip SAR controller. The converter is based on a successive-approximation register (SAR) architecture with an internal track-and-hold circuit. It can be configured to accept a 2.5 V single-ended input span. The output parallel data is binary and compatible with many common DSP parallel interfaces. The EF_ADCS1001NC operates with a dual power supply; 1.8 V and 3.3 V supply the digital and analogue IP blocks, respectively.

## 2 Applications

- Wearable Systems
- Data Acquisition Systems
- Instrumentation and Control Systems
- DSP front ends Systems

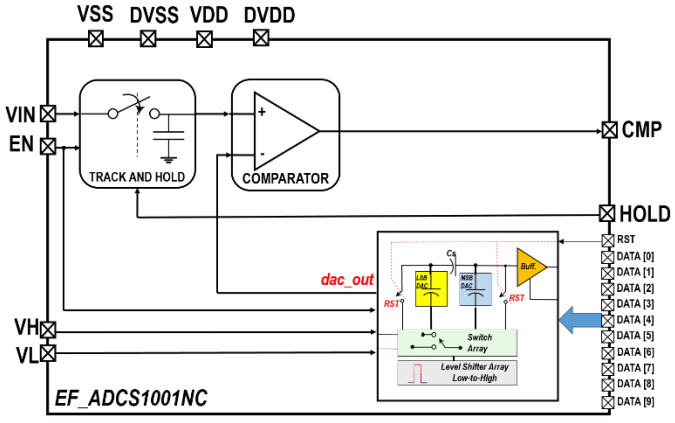


*Figure 1. Functional Block Diagram*

## Pin Configuration and Functions

| Pin's Name | I/O | Description |
|---|---|---|
| VDD | Supply | Positive power supply voltage for analog IP block, 3.3 V |
| DVDD | Supply | Positive power supply voltage for analog IP block, 1.8 V |
| VIN | Analog input | Single-ended analog input channel. The input range is 0 V to VDD. |
| EN | Digital input (1.8 V) | It is to enable track/hold and DAC operation. It would be 0V at Idle mode. |
| VH | Analog input | Positive terminal of reference input, typically VDD. |
| VL | Analog input | Negative terminal of reference input, typically 0 V. |
| DATA[0]-DATA[9] | Digital Input (1.8 V) | Digital data Input. |
| DVSS | Supply | Digital ground. |
| VSS | Supply | Analog ground. |
| CMP | Digital Output (1.8V) | Digital data output. |
| HOLD | Digital Input (1.8 V) | Digital data input. |
| RST | Digital Input (1.8 V) | Digital reset input for the split-capacitive array |

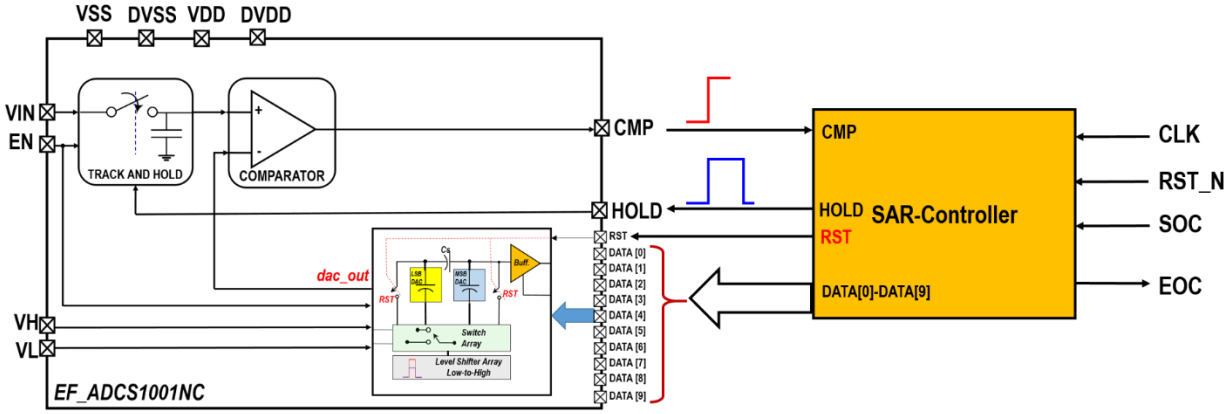


***Figure 2. Typical Connection***

***Noted:***

- *Typically, EN is connected to digital input of 1.8 V, VH represents the reference voltage of ADC, and VL is connected to 0V. VDD and DVDD are connected to 3.3V and 1.8V. VSS and DVSS are connected to 0 V. CLK, RST_N, SOC are set as described in the blow timing diagram.*
- *A 10-bit SAR controller is required. Its input signals are; CLK is the input clock signal, RST_N indicates the rest input signal, SOC stands for the input start-of-conversion, and CMP represents the input signal from the comparator's output. The output terminals of the controller are; EOC is the end-of-conversion, HOLD is an output signal to retain the sampled input voltage (VIN), RST is to reset the DAC, DATA [9]-DATA [0] are the output digital code. It is recommended to the SAR controller satisfy the next required; the SAR controller has a $T_{CLK}$, a clock period time, and a sampling time of no less than 13*$T_{CLK}$. RST_N begins at a low value and increases to a high value at 4.25*$T_{CLK}$, SOC begins at a low level and after 6.25* $T_{CLK}$ generates a pulse with an amplitude of $T_{CLK}$. HOLD becomes high after the end of the SOC's pulse and maintains high within no less than ten of the $T_{CLK}$. HOLD transits to a low level within 3* $T_{CLK}$, as a sampling time. EOC is a generated pulse signal after finishing the HOLD's pulse. RST is executed when the power is ON and after the EOC. DATA[9]-DATA[0] maintains zero however, the binary search or the first iteration begins when the HOLD signal is set to high. The timing diagram is provided as well to illustrate the description and the requirements.*

## 4 Timing Characteristics

*According to Fig. 2, a controller should be connected as an interface to the EF_ADCS1001NC and satisfy the next timing diagram.*

| Parameters | Min | Typical | Max | Units |
|---|---|---|---|---|
| $T_{D,RST}$ :Delay time of RST_N | 4.25* $T_{CLK}$ | | | µs |
| $T_{D,SOC}$ : Delay time of SOC | 6.25* $T_{CLK}$ | | | µs |
| $T_{PH,SOC}$ : High time of SOC | | $T_{CLK}$ | | µs |
| $T_{PH,EOC}$ : High time of EOC | | $T_{CLK}$ | | µs |
| $T_{CONV}$: Conversion time | 10* $T_{CLK}$ | | | µs |
| $T_{RST}$ : High time of RST | | $T_{CLK}$ | | µs |
| $T_{SAMPLE}$ : Low time of RST | 3*$T_{CLK}$ | | | µs |

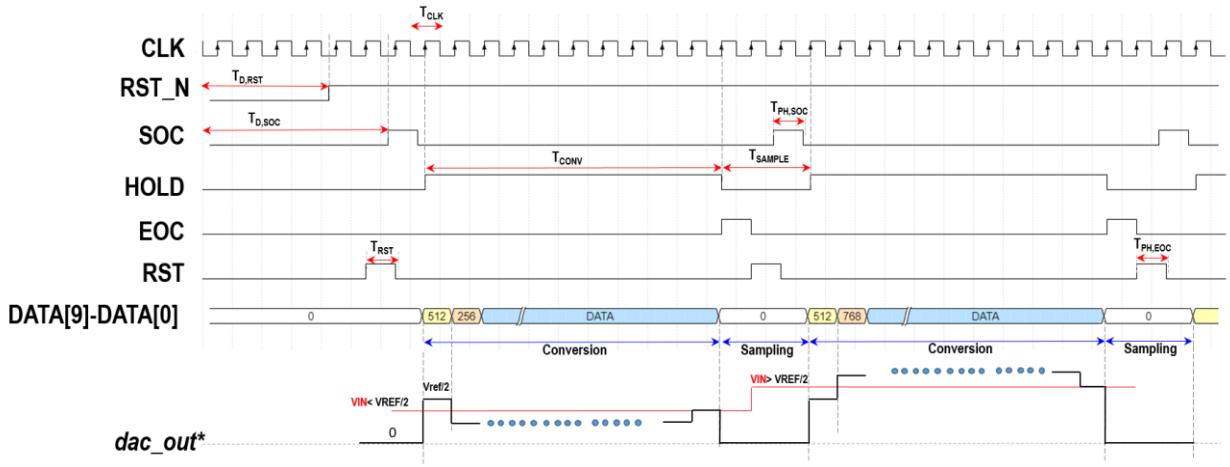


***Figure 3. Timing Diagram***

** DAC's Out Internal Net, VREF=VH-VL*

## 5 SAR-ADC Layout

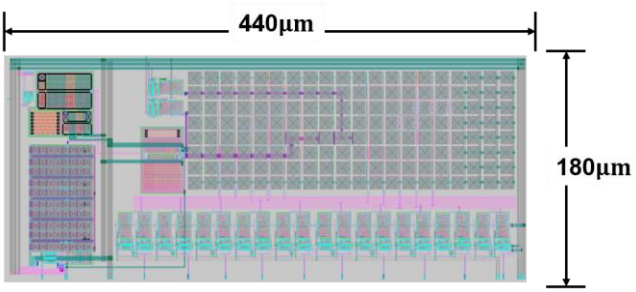


*Figure 4. EF_ADCS1001NC's Layout*

## 6 Supplementary Results

***This section indicates the functionality of the EF_ADCS1001C is verified when simulating the extracted spice.***

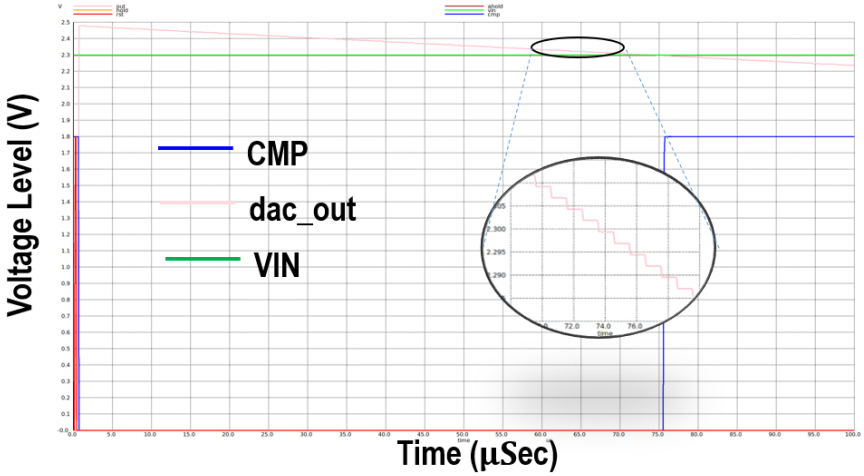


*Figure 5. Post layout simulation results*