

Open Source, 3.3 V to 1.8 V, 100 mA Full Regulator

1 Features

- 100mA Output Current Capability.
- Standard Fixed Output Voltage of 1.8 V.
- Low Dropout Voltage: 650 mV at 100 mA
- Stable with Output Capacitor^a of 47 μ F.
- Low Supply Current of 115 μ A (No Load).
- Low Temperature Coefficient 125 ppm/ $^{\circ}$ C.
- 0.016 V/V Line Regulation at 100 mA.
- 0.0083 mV/mA Load Regulation at 3.3 V.
- Power Supply Ripple Rejection of 38.9 dB.
- Startup time of 450 μ s at rising time of 100 μ s.

2 Applications

- 3.3V to 1.8V Logic Power Supply

3 Description

The LDOR01 is a positive low dropout regulator for output of 1.8 V. It is capable of supplying 100 mA of output current with a dropout voltage of 650 mV. Low operating quiescent current of 115 μ A is consumed at no load current. Moreover, it provides a standard fixed output voltage of 1.8V which is a good choice for logic power supply. The LDOR01 requires an output capacitance of 47 μ F with a wide range of ESR (0.1 Ω to 0.5 Ω) for stability. Output capacitors of this size are typically included in most regulator designs.

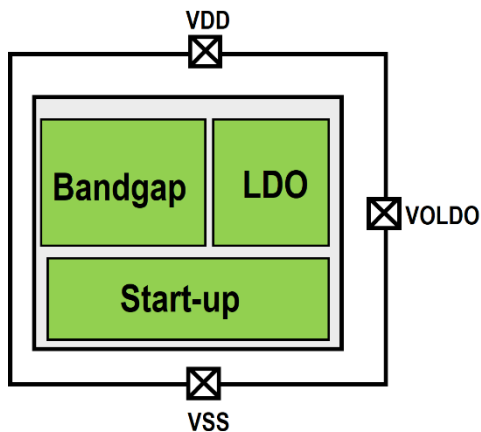


Figure 1. Functional Block Diagram

^a: CAP ALUM 47UF 20% 35V SMD

Pin Configuration and Functions

Pin's Name	I/O	Description
VDD	Supply	Positive power supply voltage, 3.3 V.
VSS	Supply	Ground.
VOLDO	Analog Output	The output of the LDO at 1.8 V.

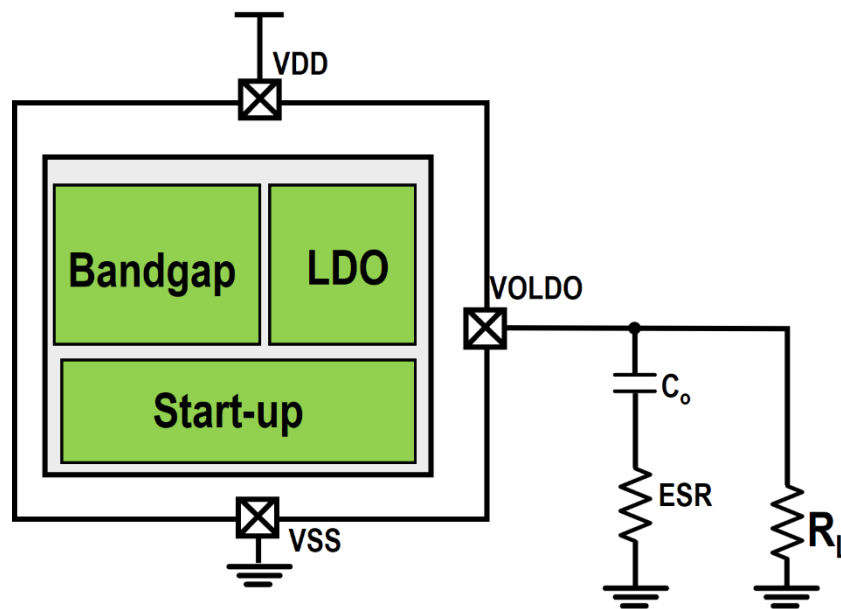


Figure 2. Typical Application

NOTE: C_o is CAP ALUM 47UF 20% 35V SMD, ESR could be in range 0.1 Ω to 0.5 Ω .

4 Electrical Characteristics

The listed parameters are reported at room temperature (27°C), Co=47μF, ESR=0.1Ω

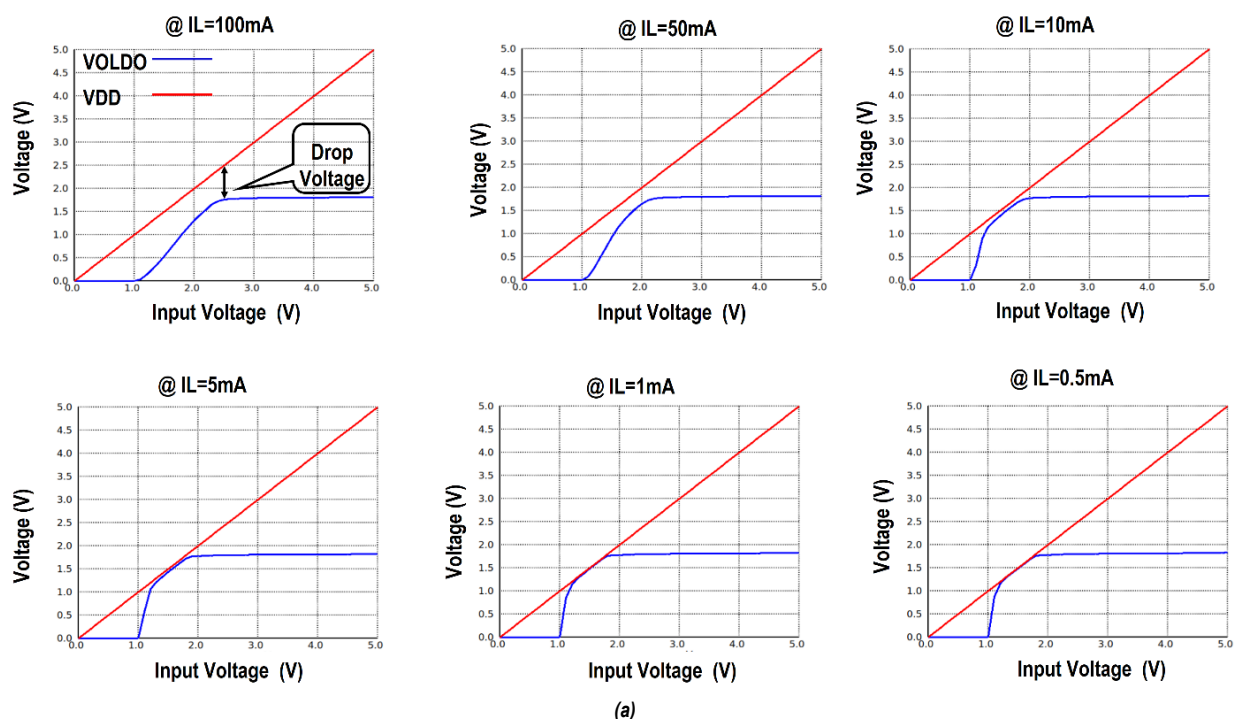
Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
VDD	Power Supply			3.3		V
VOLDO	LDO's output			1.8		V
IL	Current Load				100	mA
IQ	Quiescent Current	IL=0		0.115		mA
	Line Regulation	IL=100 mA, VDD ranges from 1.1 VDD to 0.9 VDD		0.016		V/V
		IL=0.5mA, VDD ranges from 1.1 VDD to 0.9 VDD		0.0083		
	Load Regulation	VDD=3.3 V, IL range from 0.1 mA to 100mA		0.0489		mV/mA
	Voltage Dropout	IL=0.5 mA		9		mV
		IL=100 mA		650		
	^a Temperature Range		0		70	°
TC	Temperature Coefficient	IL=1 mA		115		ppm/°C
		IL=100 mA		125		
	Startup-time	Rising time (tr)=1 μs, IL= 100 mA		335		μs
		Rising time (tr)=10 μs, IL= 100 mA		355		
		Rising time (tr)=50 μs, IL= 100 mA		400		
		Rising time (tr)=100 μs, IL= 100 mA		450		
PSRR	Power Supply Ripple Rejection	f _{ripple} = 120 Hz, (V _{in} – V _o) = 1.5 V, V _{ripple} = 0.5 V _{P-P} , IL= 100 mA		38.9		dB
		f _{ripple} = 120 Hz, (V _{in} – V _o) = 1.5 V, V _{ripple} = 1 V _{P-P} , IL= 100 mA		34		
	Output Deviation at Load Transient	IL transits from 1 mA to 100 mA, tr=tf=10 μs, VDD=3.3 V.		11.7		mV
	Output Deviation at Line Transient	VDD transits from 2.97 V to 3.63 V, tr=tf=10 μs, IL=100 mA.		52		mV
	Output noise spectral density	IL=100 mA, f=120 Hz		32		μV/√Hz
	Core Silicon area	SKYWATER 130nm		315x118		μm ²

^a: Commercial Temperature Range.

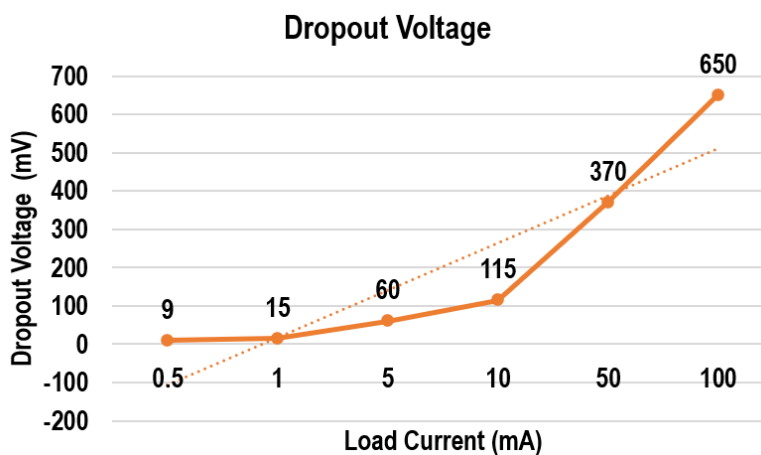
5 Typical Performance Curves

The listed parameters are reported at room temperature (27°C), $C_o=47\mu F$, $ESR=0.1\Omega$

5.1 Drop output Voltage



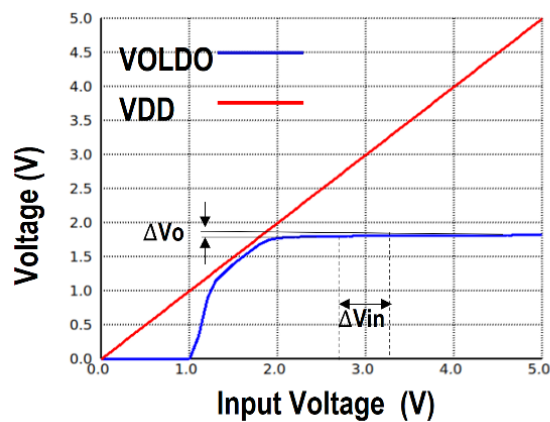
(a)



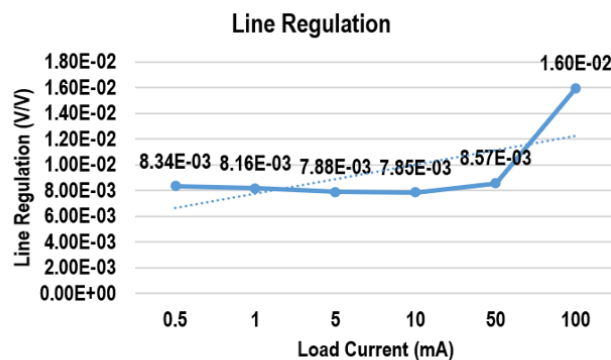
(b)

Figure 3. (a) Output Voltage vs Input Voltage, (b) Dropout Voltage vs Load Current.

5.2 Linear Regulation



(a)



(b)

Figure 4. (a) Output Voltage vs Input Voltage, (b) Line Regulation vs Load Current.

5.3 Load Regulation

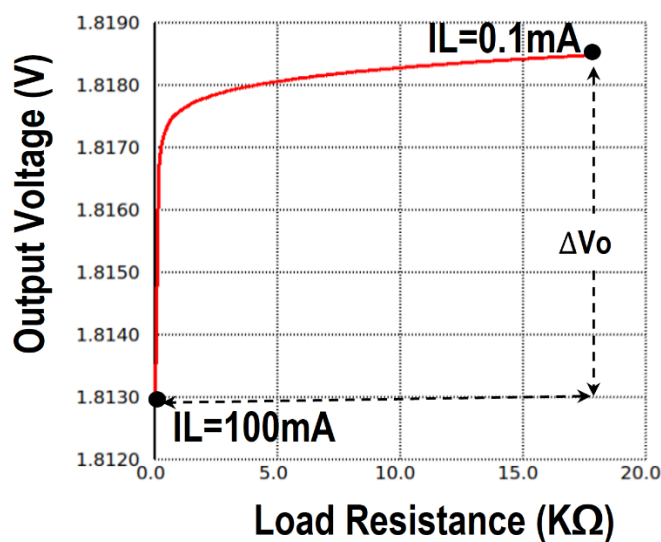


Figure 5. Output Voltage vs Load Resistance at VDD=3.3V

5.4 Startup time

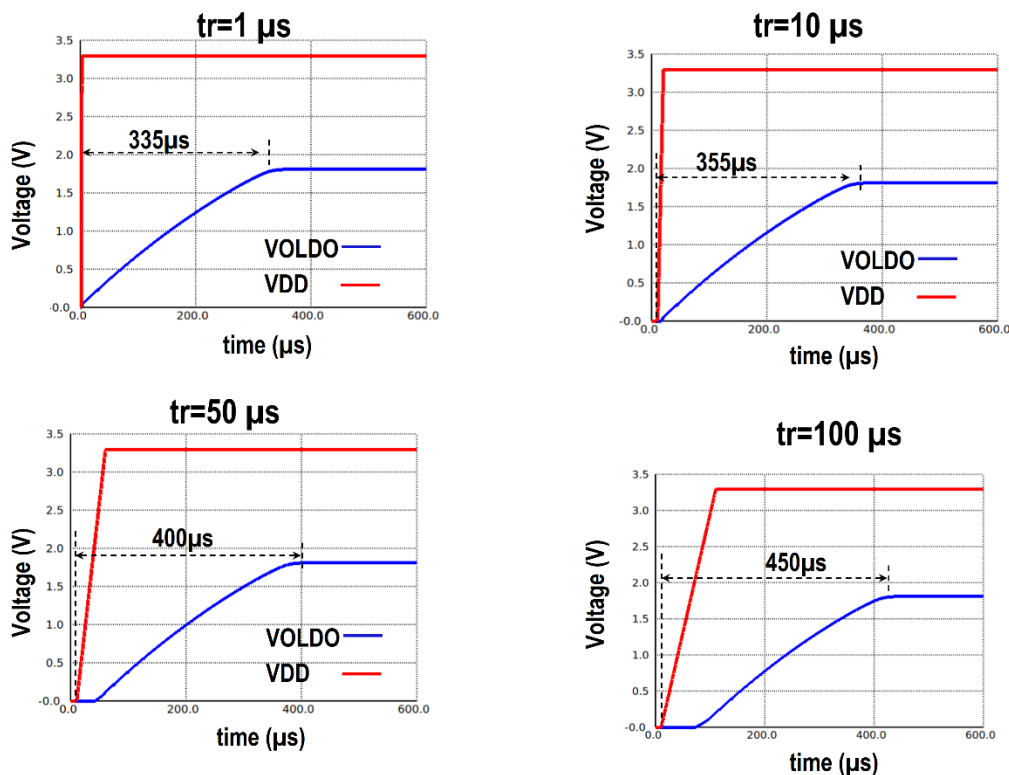


Figure 6. Startup time at different rising time of input voltage $I_L=100$ mA.

5.5 Temperature Coefficient

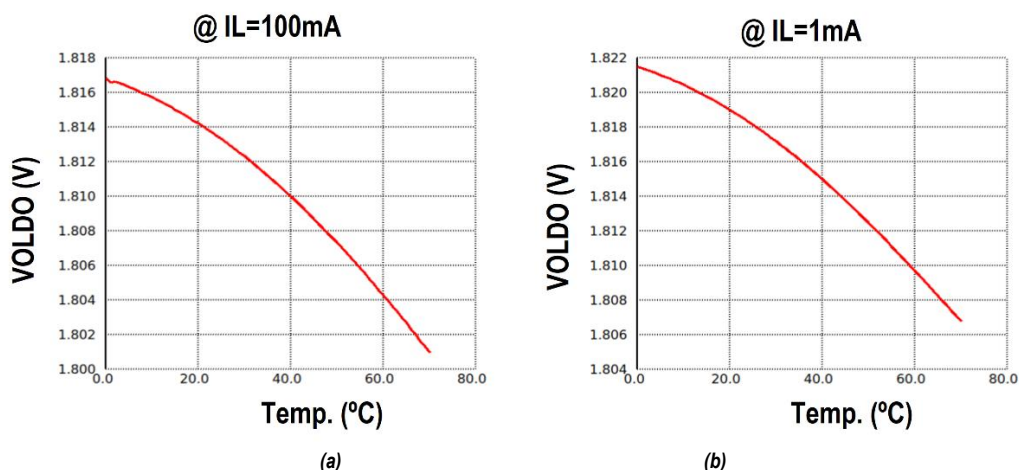


Figure 7. Temperature Coefficient of the output voltage at (a) $I_L=100$ mA, and (b) $I_L=1$ mA

5.6 Power Supply Rejection (PSR)

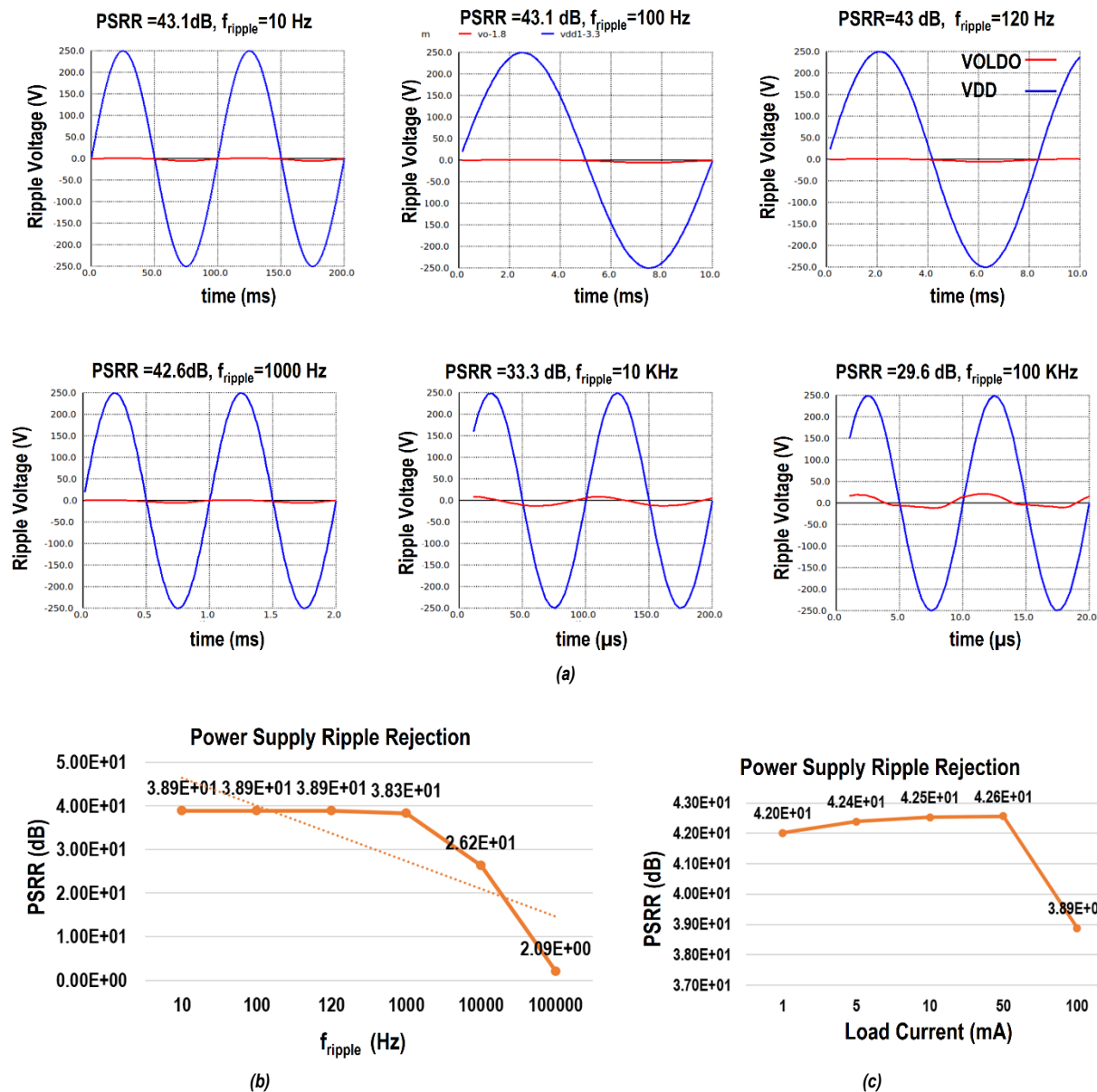


Figure 8. (a) Ripple Voltage at $V_{p-p}=0.5$ V, (b) PSRR vs Frequency at $I_L=100$ mA, (c) PSRR Vs Load current at $f_{\text{ripple}}=120$ Hz and $V_{p-p}=0.5$ V

5.7 Load Transient

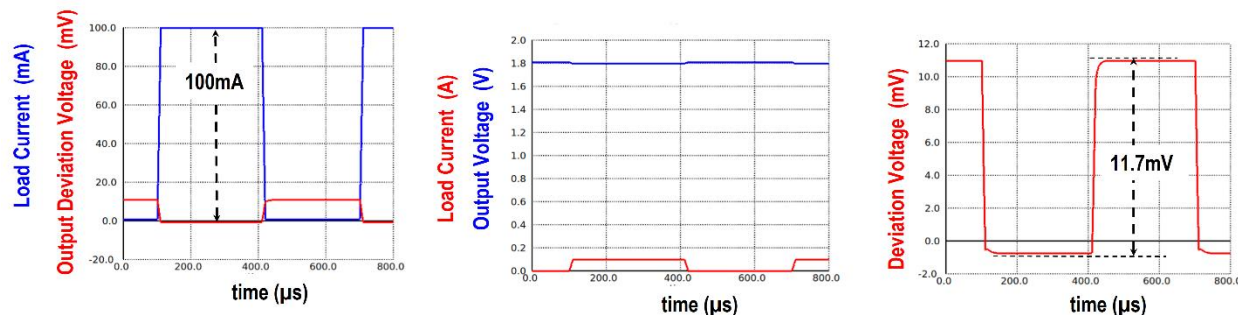


Figure 9. Load Transient Response at VDD of 3.3 V ($t_r=t_f=10\mu s$).

5.8 Line Transient

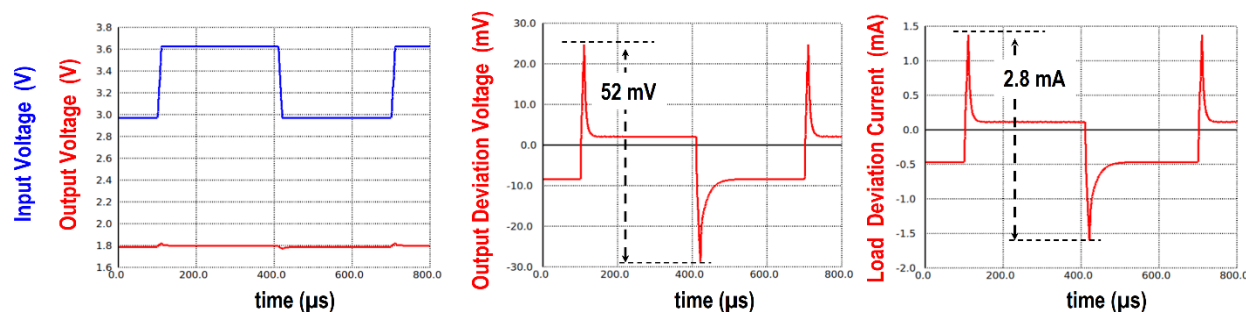


Figure 10. Line Transient Response at IL of 100 mA and VDD transits from 2.97 V to 3.63 V.

5.9 Noise Analysis

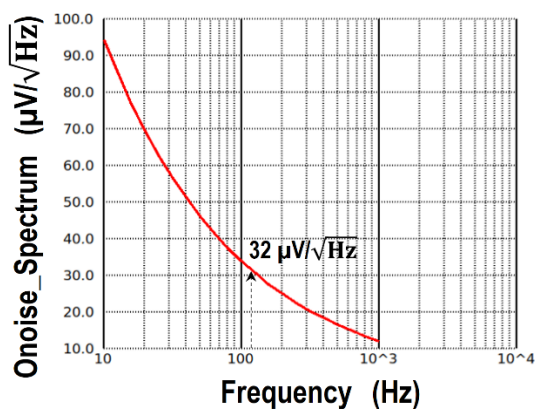


Figure 11. Output Noise Spectrum

5.10 Core Silicon area

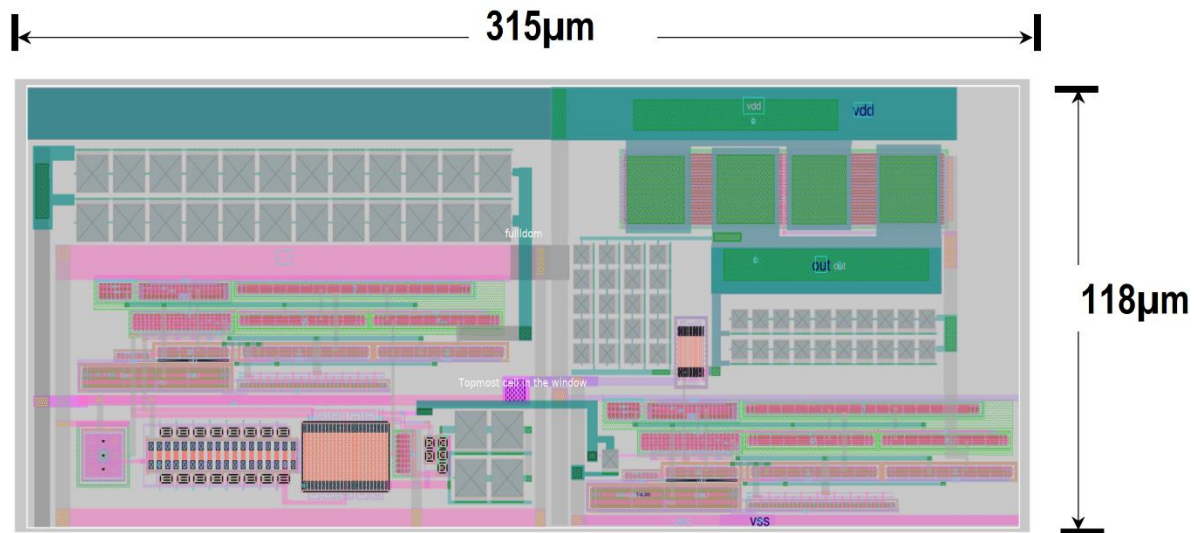


Figure 12. Full Regulator Layout