Rail-Rail Dual Channel Voltage Comparator, Dual Power Supply.

1 Features

- Rail-Rail Voltage Comparator.
- Dual Channel.
- Dual Power Supply.
- No Hysteresis.
- 12 ns Propagation Delay Input to Output.
- 371 µA Max Quiescent Current.
- Input Voltage range 0V to 3.3V.
- Output Voltage range 0 V to 1.8V.
- 5mV input offset voltage.

2 Applications

- SAR-ADC.
- Pulse Generator.
- Threshold Detector.

3 Description

The EF_R2RVC02 is a Dual channel rail-to-rail voltage comparator with a built-in reference circuit. Its input consists of an n-differential pair connected with a p-differential pair in parallel. While a class B, which is a CMOS inverter, is utilised for the comparator's output stage. The comparator operates with dual power supplies of 3.3V and 1.8V. It provides a propagation delay of 12 nA and a maximum quiescent current of 371 µA.

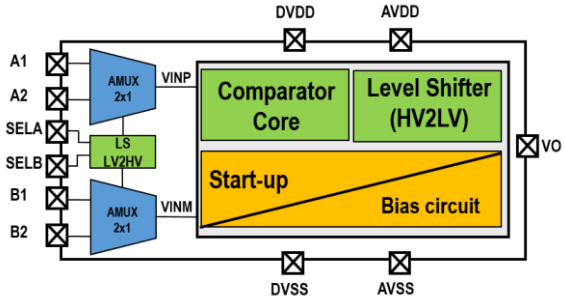


Figure 1. Functional Block Diagram

Pin Configuration and Functions

Pin's Name	I/O	Description
AVDD	Supply	Positive power supply voltage for analog IP block, 3.3 V
AVSS	Supply	Analog ground.
DVDD	Supply	Positive power supply voltage for analog IP block, 1.8 V
DVSS	Supply	Digital ground.
Vo	Digital Output	The output of the comparator
A1, A2	Analog input	Dual channel analog input for the positive terminal of the comparator
B1, B2	Analog input	Dual channel analog input for the negative terminal of the comparator
SELA	Digital Input (1.8V)	Select line for the channel A1 and A2
SELB	Digital Input (1.8V)	Select line for the channel B1 and B2

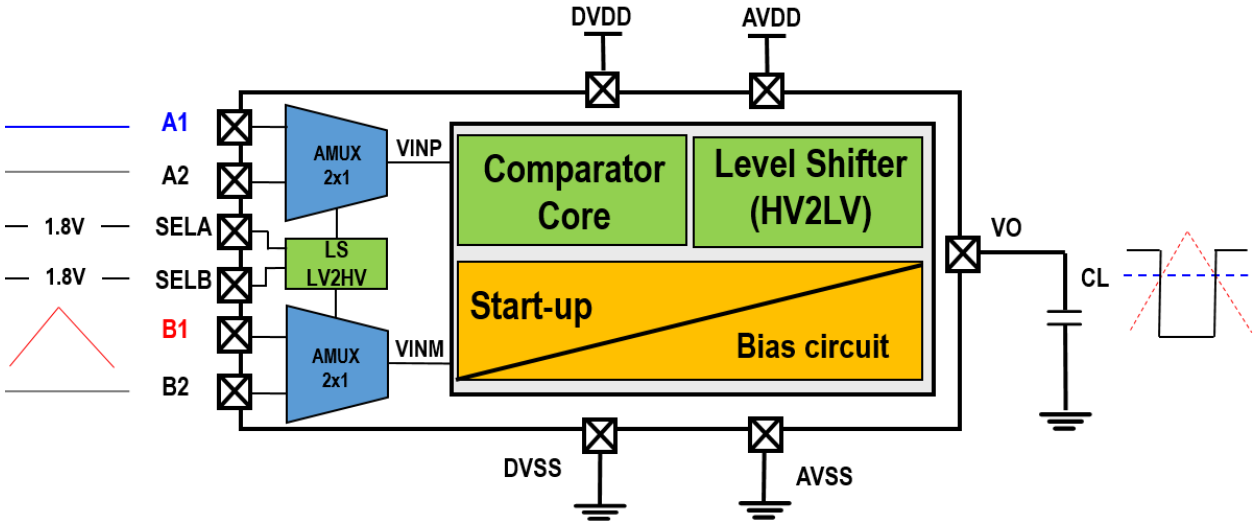


Figure 2. Typical Application

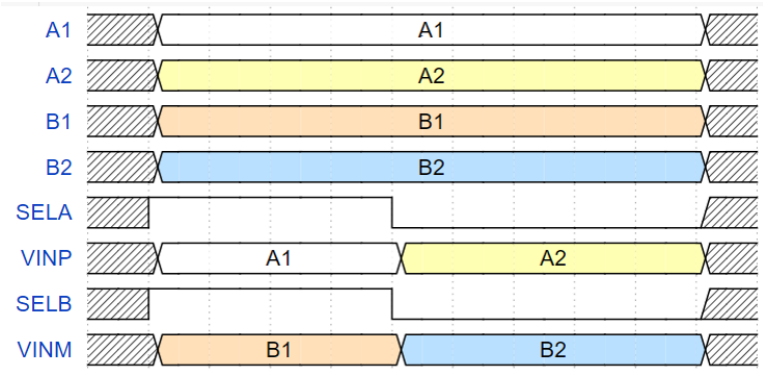


Figure 3. Timing Diagram

4 Electrical Characteristics

The listed parameters are reported at room temperature (27°C), CL=1pF, SELA=1.8V, SELB=1.8V

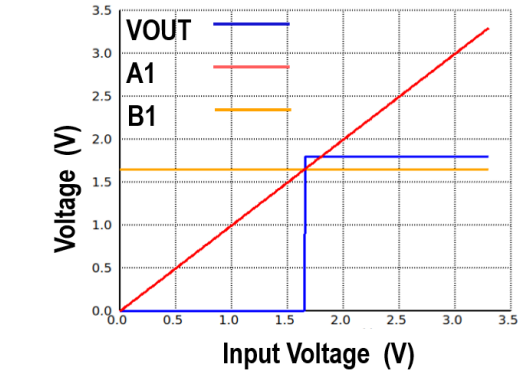
Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
AVDD	Analog Power Supply			3.3		V
AVDD	Digital Power Supply			1.8		
IQ	Total Supply Current	AVDD=3.3V, DVDD=1.8V, A1=B1=1.65		0.371		mA
		AVDD=3.3V, DVDD=1.8V, A1=0V, B1=1.65V		0.315		
		AVDD=3.3V, DVDD=1.8V, A1=1.65V, B1=0V		0.323		
		AVDD=3.3V, DVDD=1.8V, A1=3.3V, B1=3.3V		0.273		
		AVDD=3.3V, DVDD=1.8V, A1=0V, B1=0V		0.295		
V_{IL}	Low Input Voltage	AVDD=3.3V, DVDD=1.8V		0		V
V_{IH}	High Input Voltage			3.3		
V_{OL}	Low Output Voltage			0		
V_{OH}	High Output Voltage			1.8		
V_{OS}	Input Offset Voltage	AVDD=3.3V, DVDD=1.8V, A1=1.65V, VINP swept from 0V to 3.3V		4.99		mV
tr	Rise Time	@f=100KHz, CL= 1pF, A1=1.65V, B step from 0V to 3.3V		12.4		ns
tf	Fall Time			5.6		
tphl	Propagation Time (High to Low)			10.8		
tplh	Propagation Time (Low to High)			12.8		
	[a]Temperature Range		0	27	70	°C
	Core Silicon area	SKYWATER 130nm		76x96		μm^2

[a] : Commercial Temperature Range.

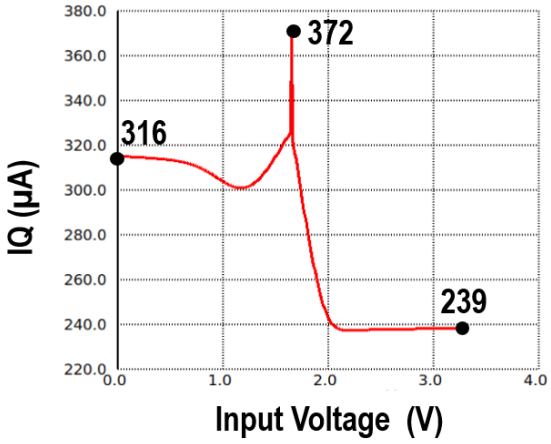
5 Typical Performance Curves

The listed parameters are reported at room temperature (27°C), CL=1pF, SELA=1.8V, SELB=1.8V

5.1 DC Sweep of VINP



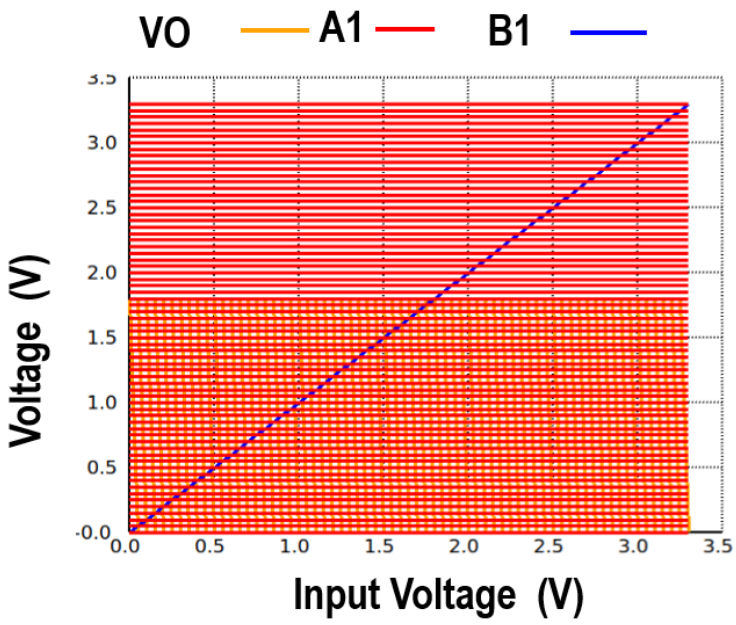
(a)



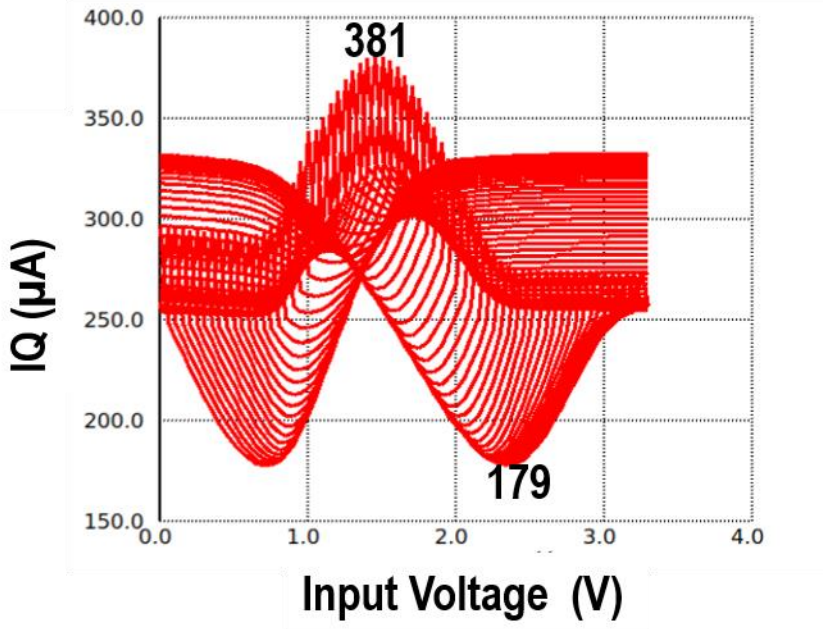
(b)

Figure 4. DC sweep simulation result, (a) input (A1) and output (Vout) voltages, (b) Quiescent current .

5.2 DC Sweep of VINP and VINM



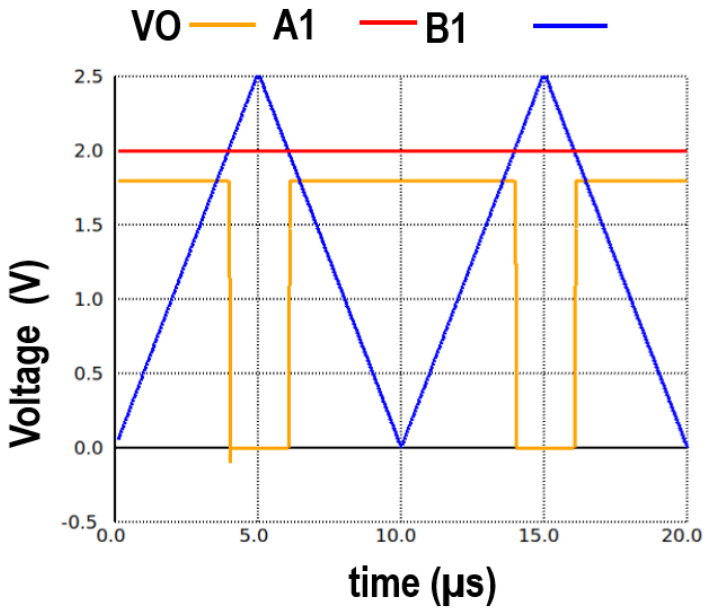
(a)



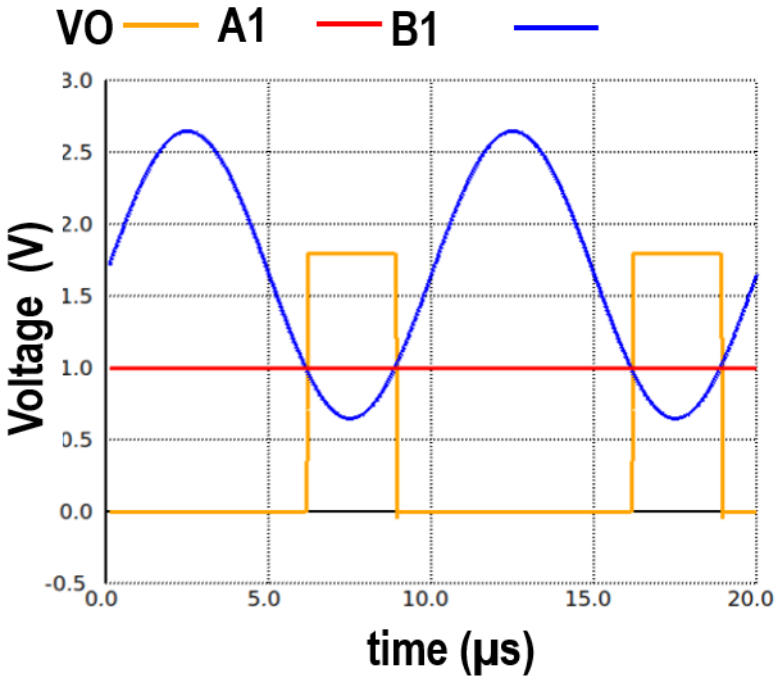
(b)

Figure 5. DC sweep simulation result, (a) inputs of A1, B1, and output (Vo) voltages, (b) Quiescent current .

5.3 Transient Ramp and Sin Signals



(a)



(b)

Figure 6. (a) Ramp, (b) Input and output voltages of the comparator.

5.4 Transient Step Signal

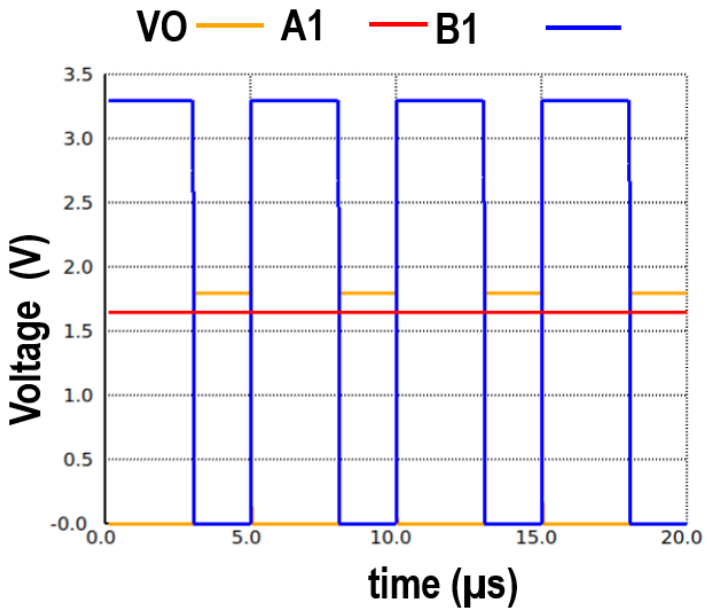


Figure 7. Step Input and output voltages of the comparator.

5.5 Core Silicon area

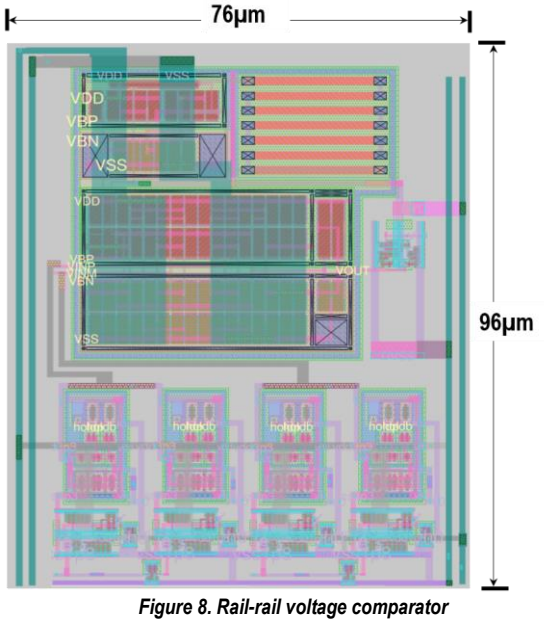


Figure 8. Rail-rail voltage comparator