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X-Ray for IP-Blocks

Ahmed Reda Mohamed

Outlines

- ❑ Motivation and Problem Statement
- ❑ X-ray Tool for Analog/Mixed Circuit
- ❑ Beyond Scene
- ❑ Case Study
- ❑ Conclusion

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Motivation and Problem Statement (1/2)

Available Open Source Analog & Mixed Signal IP

Phase Locked Loop (PLL)
Digital to Analog Converter (DAC)
Rail-to-Rail Comparators
Filters
Voltage Controlled Oscillator (VCO)
Trans-Impedance Amplifier (TIA)
Analog/Mixed Accelerator
Analog to Digital Converter (ADC)
Bandgap Voltage Reference
Amplifiers
Low Dropout Voltage Regulator (LDO)
Analog Neuron
Audio Amplifier
DC to DC converter
…

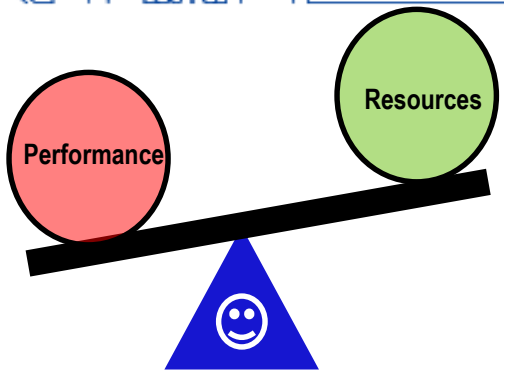
Limited Analysis/test bench, Electrical ch/cs,…etc

Pre-layout Simulation	
Analysis's types	Param.
DC	
DC sweep	
AC	
Trans	
..	
FOM	
MC	
PVT	
CP,CPK	

Layout	
Item	Checked
DRC	
Silicon Area	

Lack info. of the correct schematic/layout

Check LVS



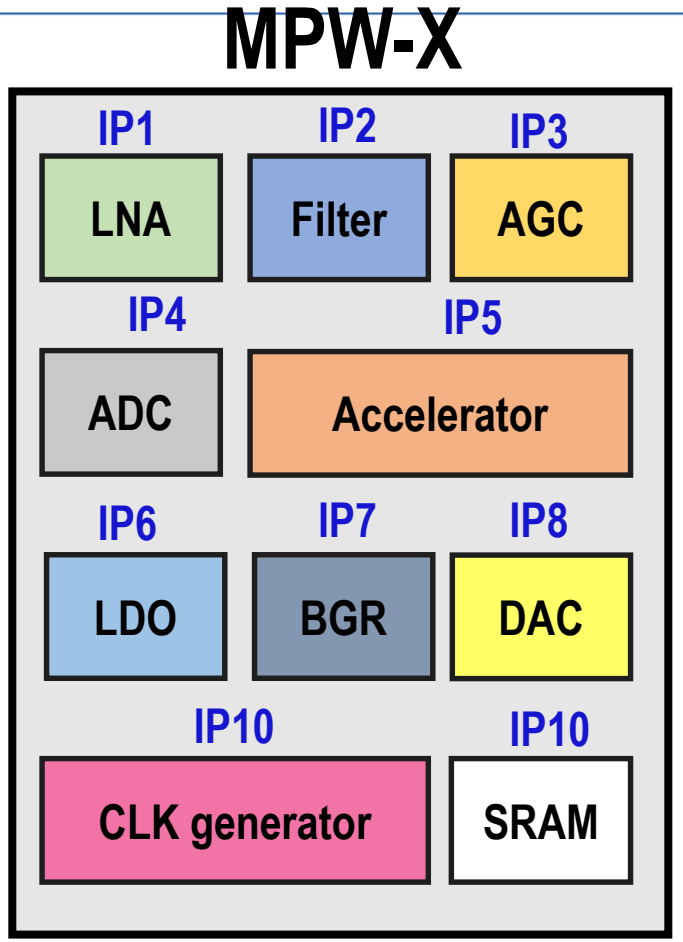
Post-layout Simulation	
Analysis's types	Param.
DC	
DC sweep	
AC	
Trans	
..	
FOM	
MC	
PVT	
CP,CPK	

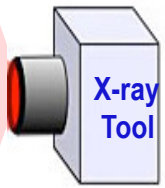
Lack info. of doing PEX/post-layout sim.

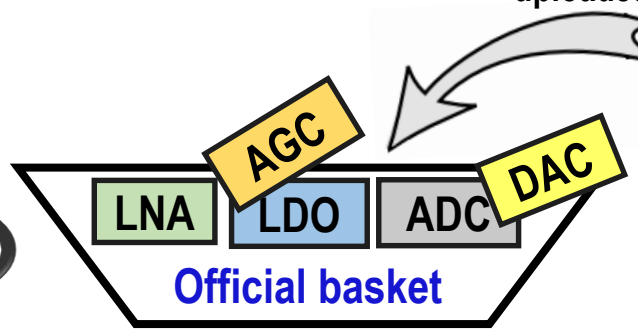
Within this process, many IP blocks are not working well Or useless economically. There is no official doc.

Waste silicon area, time, effort,…money

Motivation and Problem Statement (2/2)







stamp

Milestone (1)	
Pre-layout Simulation	**Submit**
• Testbench (Dc, Ac, Trans., Noise, THD, Monte-Carlo ,PVT, CP and CPK…)	• Testbench (*.spice and *.sch) • Simulation results/table (*.docx)
Milestone (2)	
Layout	**Submit**
• DRC check • LVS check	• Layout files (*.mag and *.gds) • Extracted files from layout_No RC (*.spice) • Corresponding spice files from XSCHEM (*.spice)
Milestone (3)	
Post-layout Simulation	**Submit**
• Re-Simulate all the testbenches in pre-layout simulation.	• Extracted files with RC (*.spice) •Simulation results/table (*.docx)
Milestone (4)	
Submit a comparison table between pre and post layout simulation results.	
Milestone (5)	
Submit a comparison table between simulation and measured results	

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X-ray Tool for Analog/Mixed Circuit

❑Features

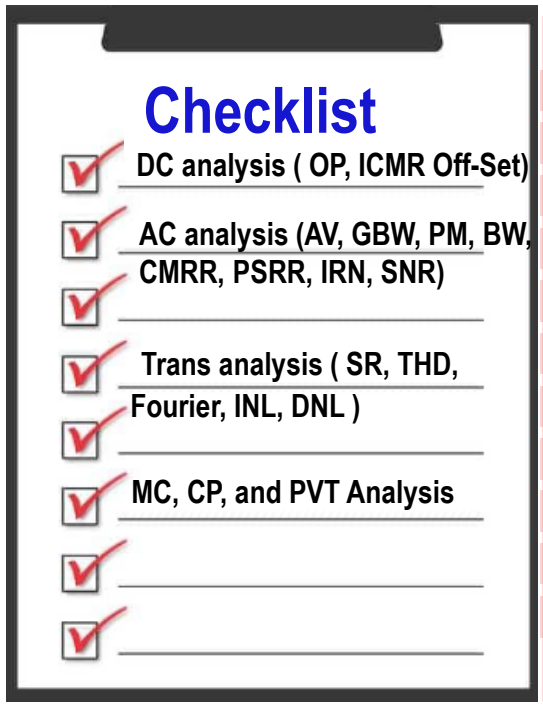
- ❑ Open Source Tool
- ❑ Deep Automated Analysis
- ❑ Fully Characterization of Analog IP Blocks
- ❑ Guaranteed Maturity Design
- ❑ Troubleshooting for Sign-off
- ❑ Improve Productivity Time
- ❑ Quasi-independent

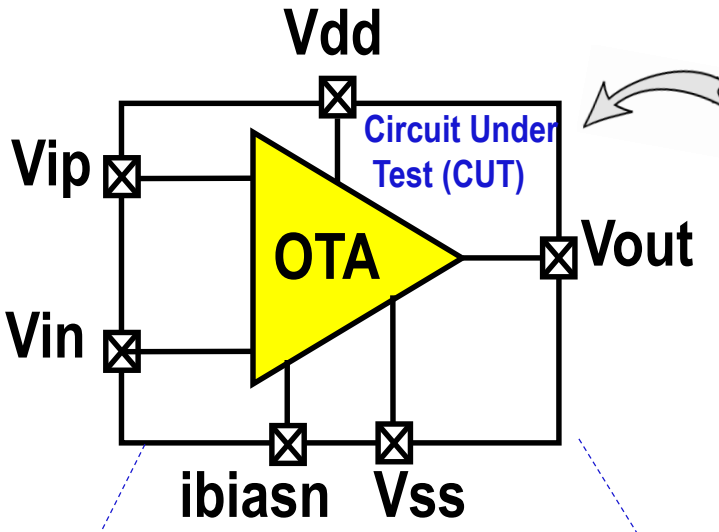
❑Need Resources

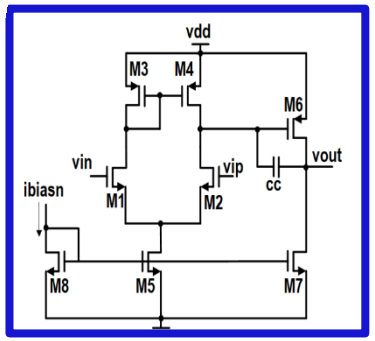
- ❑ XSCHEM
- ❑ NGSPICE
- ❑ PYTHON
- ❑ SKYWATER130nm

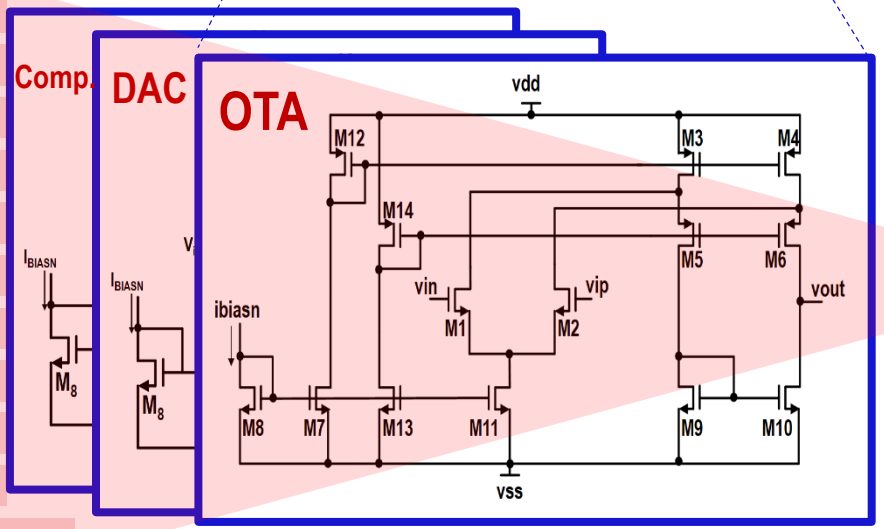
❑ User Submission

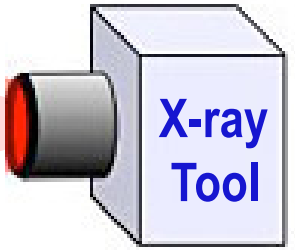
- ❑ *.spice Netlist
- ❑ *.cfg Configuration
- ❑ *.txt Design Spec.











X-ray Tool for Analog/Mixed Circuit

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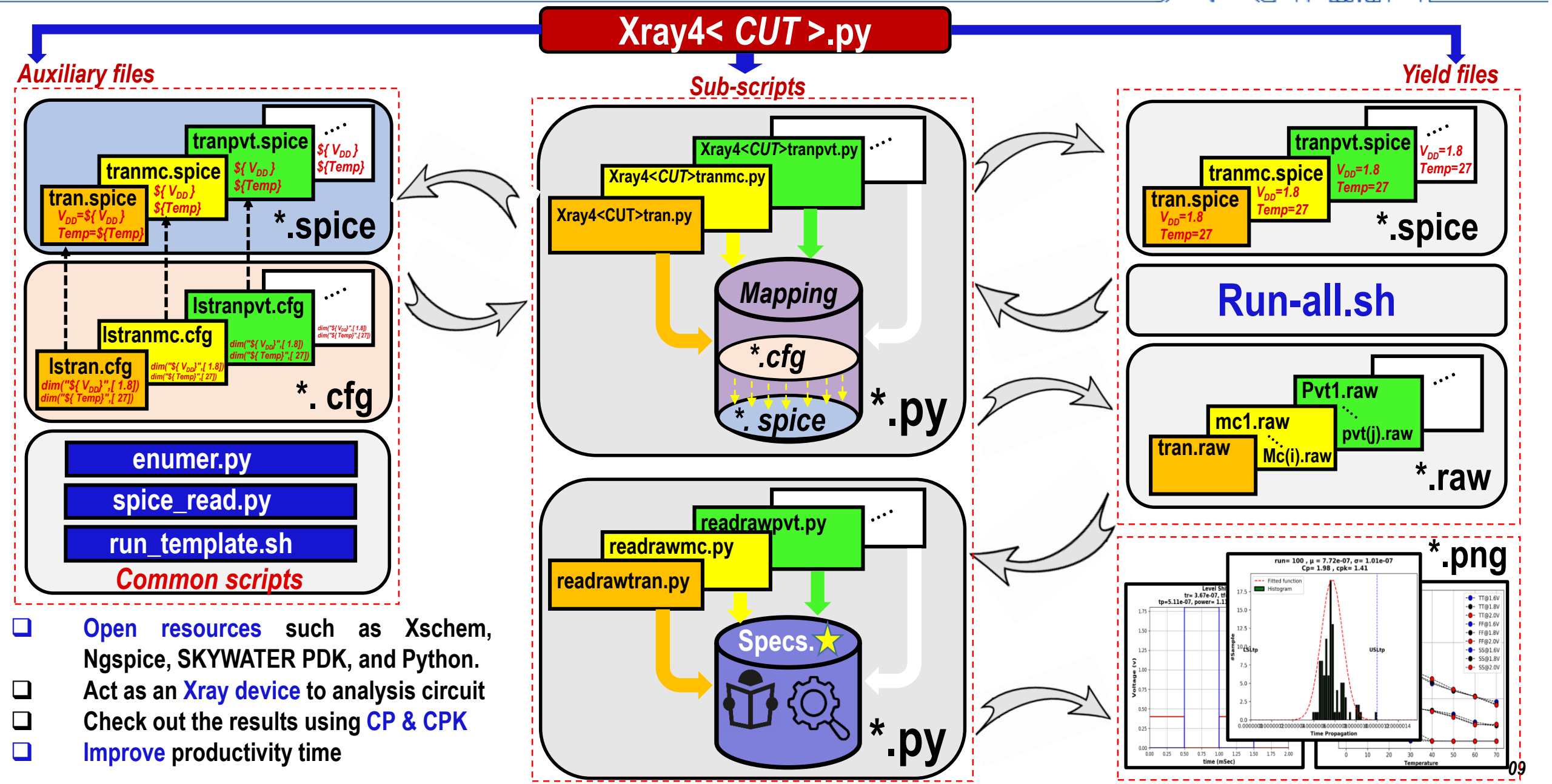
Beyond Scene



- Open resources such as Xschem, Ngspice, SKYWATER PDK, and Python.
- Act as an Xray device to analysis circuit
- Check out the results using CP & CPK
- Improve productivity time

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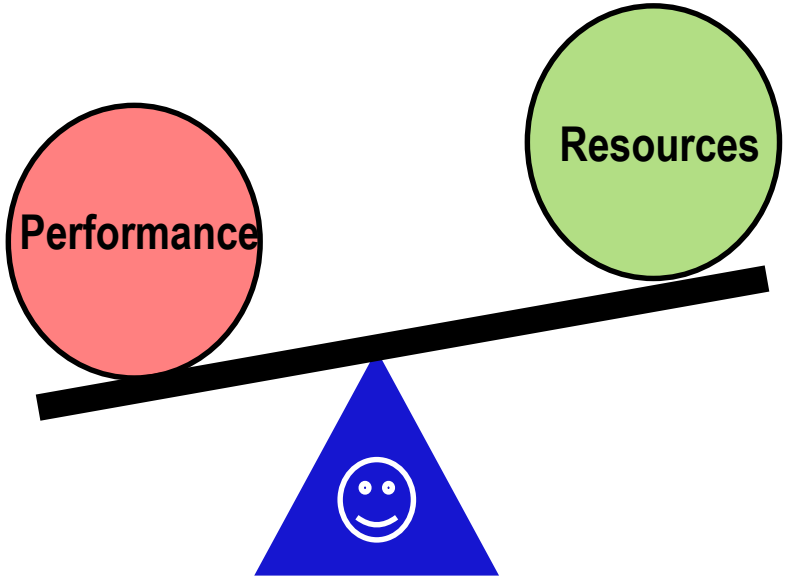
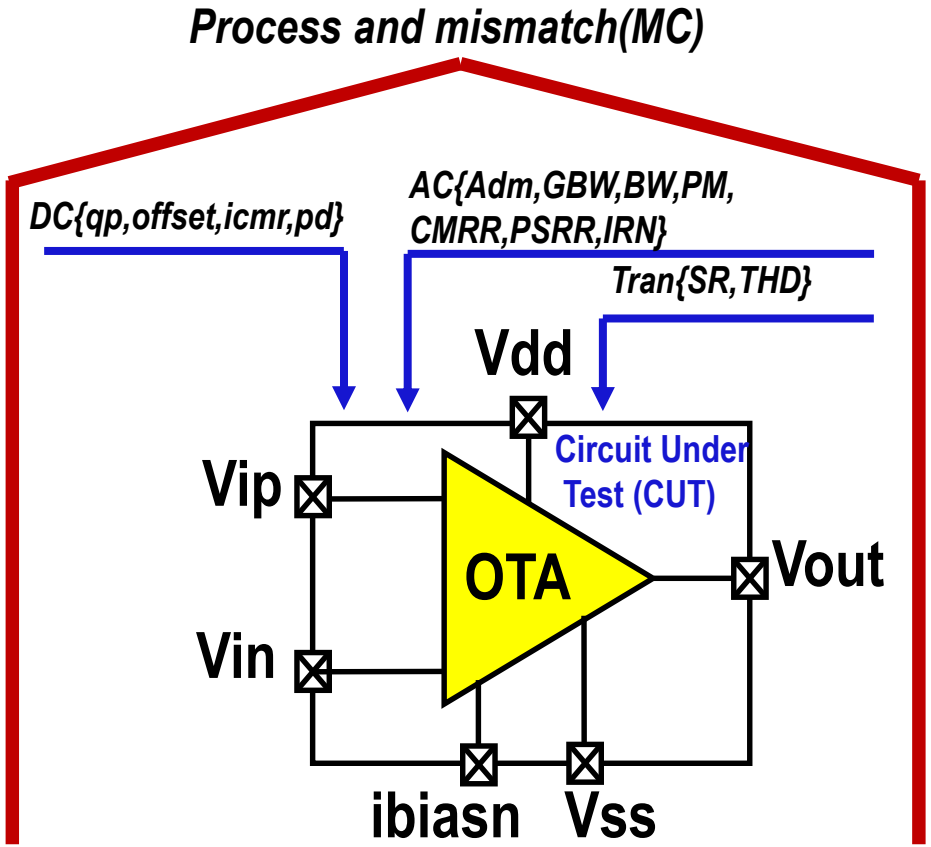
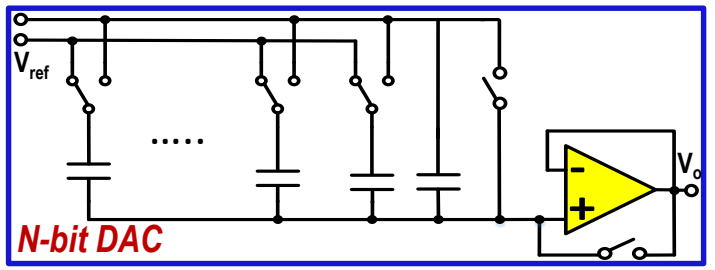
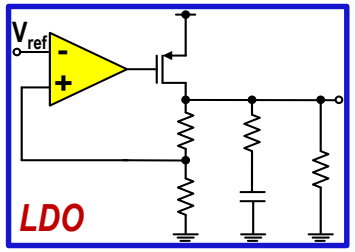
Case Study (1/8)

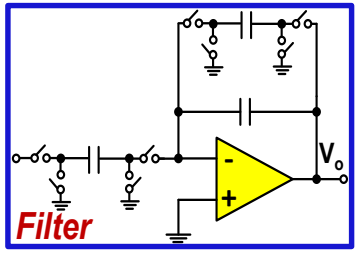
- An automated analysis of the trans-conductance amplifier (OTA)
- OTA is an universal analog building block Circuit Under Test (CUT).
- Herein, trans, dc, ac simulations are considered.MC for ac parameters such as AV and GBW considered as well.

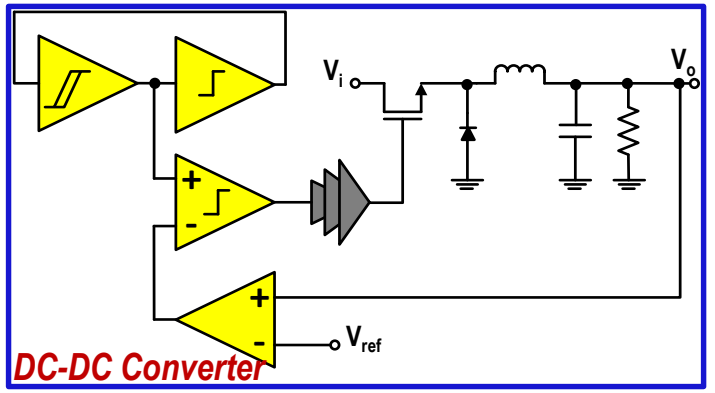


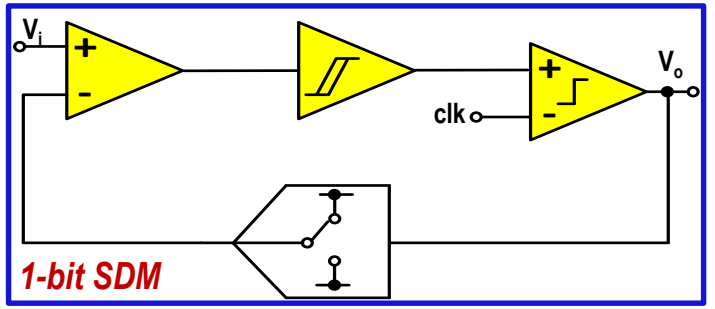










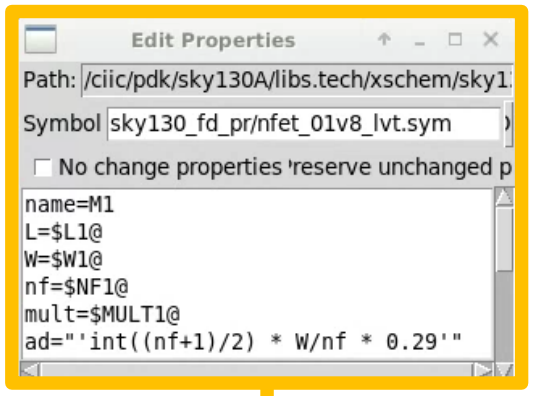


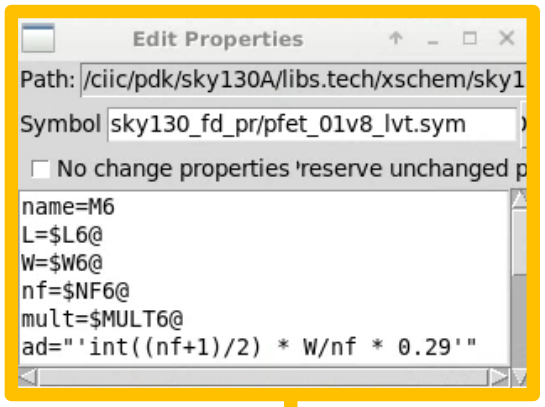
Case Study (2/8)

1- Draw the OTA circuit (Folded Cascode, Miller..etc) using XSCHEM

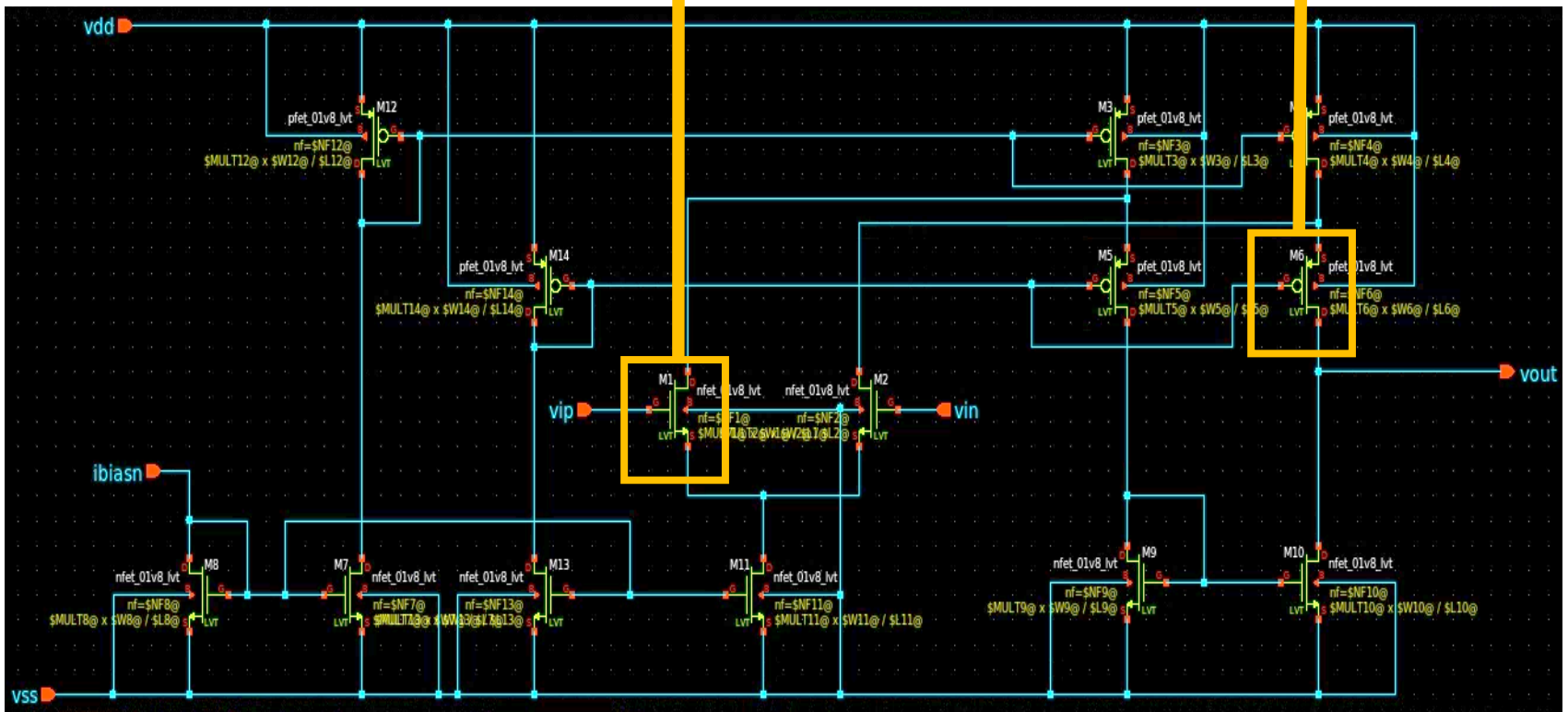
2- Set all dimensions as design parameters

- Select a device and press “q”
- Replace L, W, nf, and mult as listed



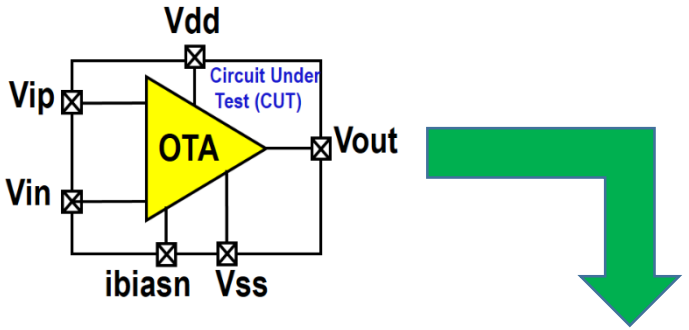


	L	W	nf	mult
M1	$L1@	$W1@	$NF1@	$MULT1@
M2	$L2@	$W2@	$NF2@	$MULT2@
M3	$L3@	$W3@	$NF3@	$MULT3@
..	..	..	..	..
Mi	$Li@	$Wi@	$NFi@	$MULTi@
C1	$LC1@	$WC1@		
C2	$LC2@	$WC2@		
..	..	..		
Ci	$LCi@	$WCi@		

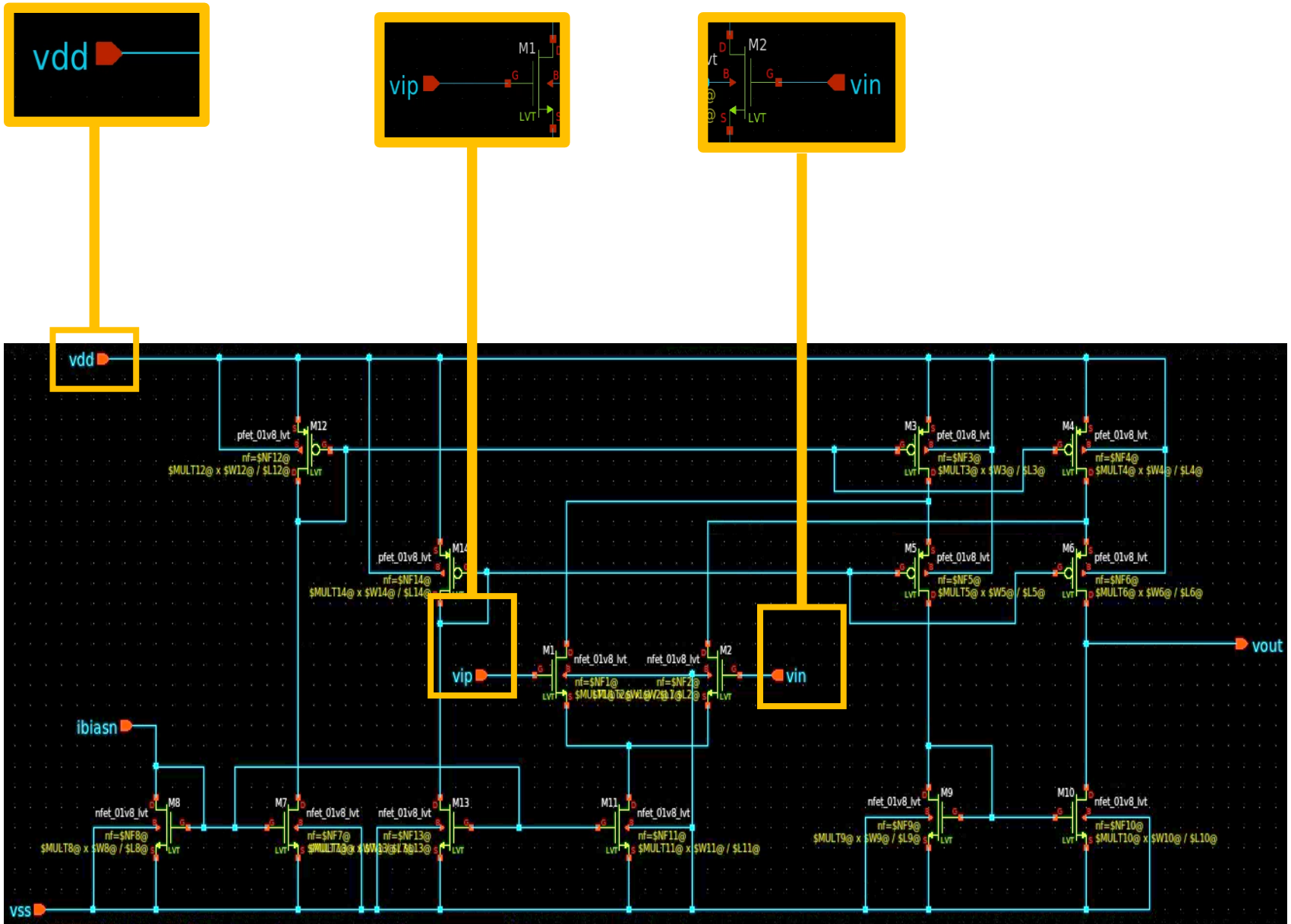


Case Study (3/8)

3- Make sure the ports' name as listed.

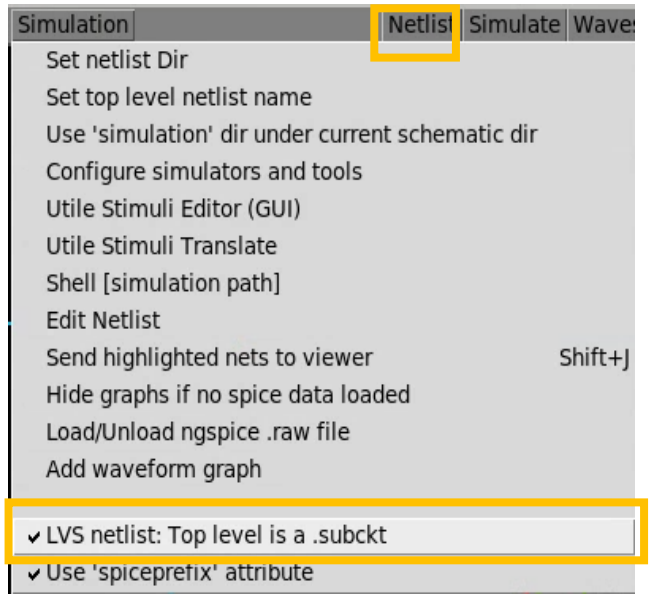


	Name
+Ve Power Supply	vdd
-Ve Power Supply	vss
Inverting Terminal	vin
Non-Inverting Terminal	vip
Output Terminal	vout
Input Bias Terminal	ibiasn



Case Study (4/8)

4- From XSCHEM, mark “LVS netlist:Top level is a .subckt”, then press “Netlist”



5- Save the netlist as “*ndiff-ota-circuit.spice*”

6-Open a file and save at as a “*ota.cfg*” to present a configuration file of the design.

7-Open “*ota.cfg*” and edit the following to configure the previous design parameters.

Typical/Common Setting

```
dim("${TOPCELLNAME}",["tb"])
dim("${CORNERS}",    ["tt"])
dim("${TEMP_VAL}",   ["27"])
dim("${TNOM_VAL}",   ["27"])
```

AC Analysis Setting

```
dim("${ND}",     ["10"])
dim("${FSTART}",["1"])
dim("${FSTOP}",  ["50MEG"])
```

ICMR Analysis Setting

```
dim("${ICMRVSTART}",  ["0"])
dim("${ICMRVSTOP}",   ["1.8"])
dim("${ICMRVSTEP}",   ["1m"])
```

Noise Analysis Setting

```
dim("${NND}",     ["10"])
dim("${NFSTART}",["1"])
dim("${NFSTOP}",  ["1MEG"])
```

THD Analysis Setting

```
dim("${VPEAKTHD}",["0.65"])
dim("${FTHD}",    ["1k"])
dim("${TSTEP}",   ["1u"])
dim("${TSTOP}",   ["2m"])
dim("${TSAVE}",   ["10u"])
dim("${FUNDFREQ}",["1k"])
```

Offset Analysis Setting

```
dim("${DCSWEEPSTART}",["0.8"])
dim("${DCSWEEPSTOP}", ["1"])
dim("${DCSWEEPSTEP}", ["100u"])
```

Slew rate Analysis Setting

```
dim("${VPULSHIGH}",   ["1.5"])
dim("${VPULSLOW}",    ["0.6"])
dim("${VPULSDELAY}",  ["0"])
dim("${VPULSDTR}",    ["10ns"])
dim("${VPULSTF}",     ["10ns"])
dim("${VPULSTH}",     ["1u"])
dim("${VPULSTPERIOD}",["2u"])
dim("${SRTSTEP}",     ["0.1n"])
dim("${SRTSTOP}",     ["2.5u"])
dim("${SRTSAVE}",     ["0.5u"])
dim("${vout20}",      ["0.6"])
dim("${vout80}",      ["1.5"])
```

Monte-Carlo Setting

```
dim("${DEV}",     ["1"])
dim("${LOT}",     ["0"])
dim("${CORNERMM}",["tt_mm"])
dim("${MC_COUNT}",["1000"])
dim("${SEED}",    ["0"])
```

Circuit Parameters

```
dim("${VDD}",    ["1.8"])
dim("${CL}",     ["2p"])
dim("${IBIASN}",["20u"])
dim("${VCOM}",   ["0.9"])
dim("${W1}",     ["5"])
dim("${L1}",     ["1"])
dim("${NF1}",    ["1"])
dim("${MULT1}",  ["11"])
dim("${W2}",     ["5"])
dim("${L2}",     ["1"])
dim("${NF2}",    ["1"])
dim("${MULT2}",  ["11"])
```

Case Study (5/8)

8- Open a file and save at as a "*specifications.txt*" to present design specs. ☺

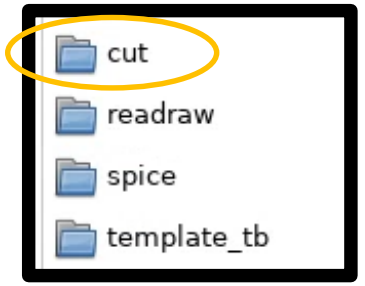
9-Open "*specifications.txt*" and edit the following upper/lower specification limits.

```
# NAME OF OTA:
folded_cascode
# MAX. VOLTAGE GAIN (dB):
100
# MIN. VOLAGE GAIN (dB) :
0
# MAX. GAIN BANDWIDTH PRODUCT (Hz):
50e6
# MIN. GAIN BANDWIDTH PRODUCT (Hz):
1e6
# MAX. PHASE MARGIN (Deg.):
90
# MIN. PHASE MARGIN (Deg.):
45
# LOAD CAPACITANCE:
1e-12
```

Noted:

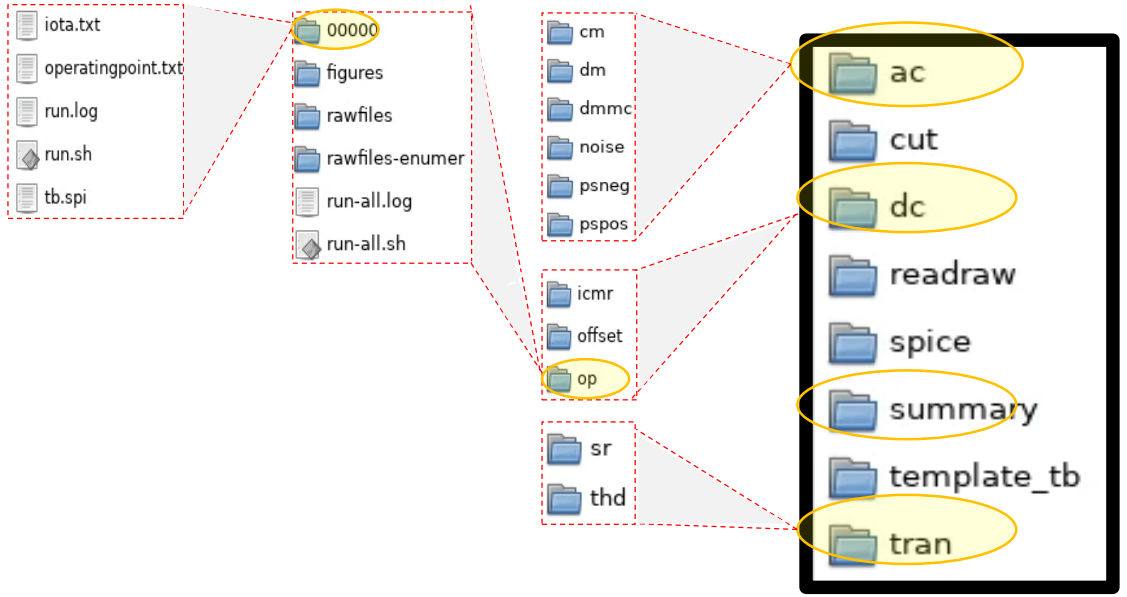
- ❑ The designer/user should submit 3X files:
  1. ndiff-ota-circuit.spice
  2. ota.cfg
  3. specifications.txt

10- Copy those files to the folder named "cut", as shown.

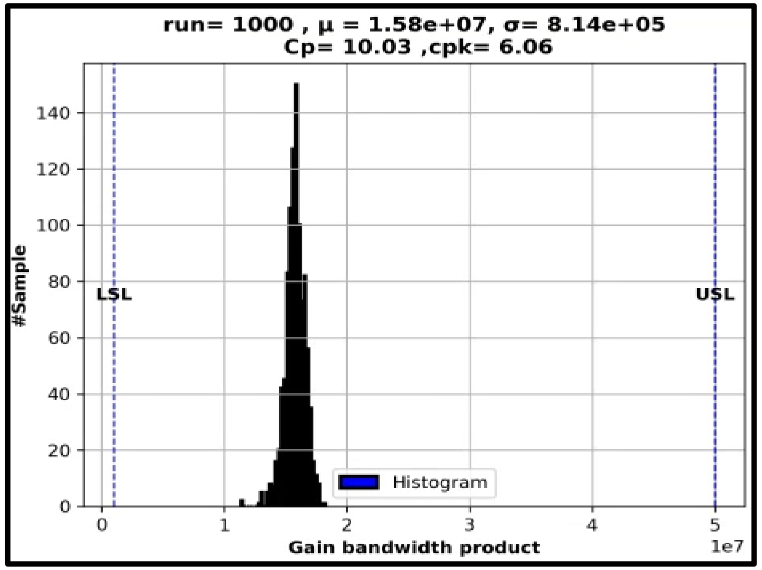


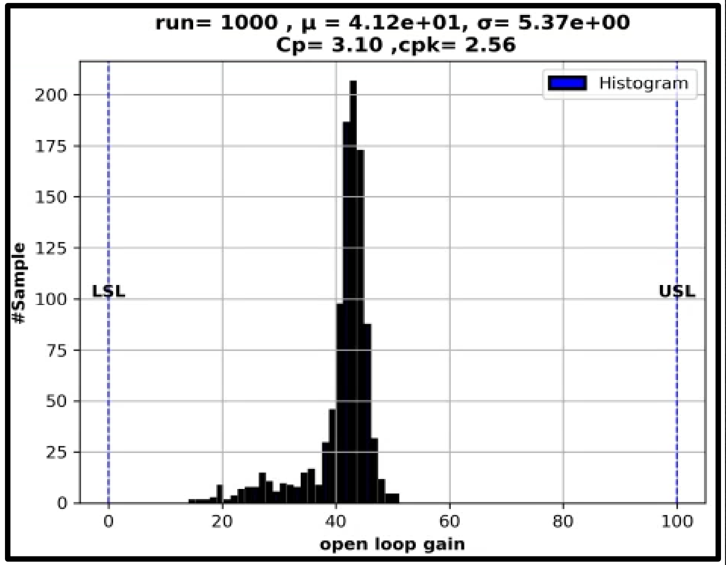
11- Using the following command, XRAY4OTA script can be executed. Several folders and files are generated as shown.

```
ahmed_reda@ciic .../xray4ota (main) $ ./xray4ota.py
```

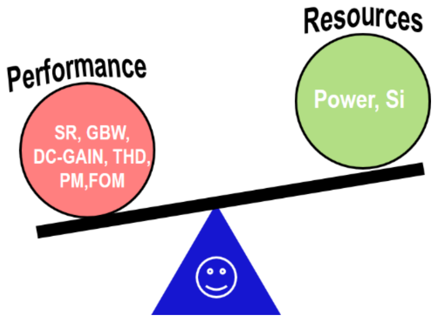


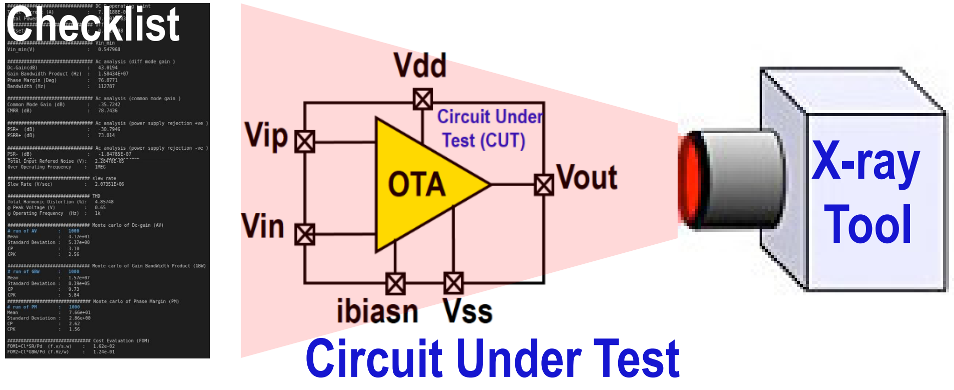
Case Study (6/8)

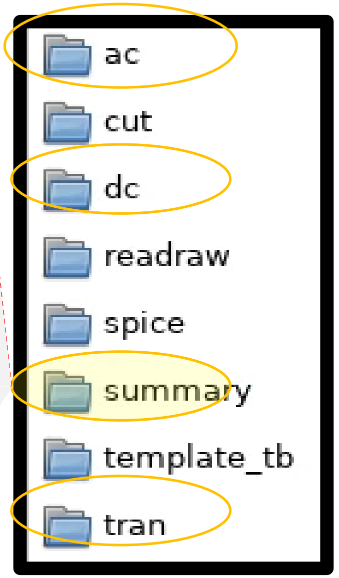





```
############################## DC Q-operating point
Total Current (A)             :  7.10188E-05
Total Power (W)               :  0.000127834
############################## Offset
Offset(V)                     :  0.0024598

############################## Vin_min
Vin_min(V)                    :  0.547968

############################## Ac analysis (diff mode gain )
Dc-Gain(dB)                   :  43.0194
Gain Bandwidth Product (Hz)   :  1.58434E+07
Phase Margin (Deg)            :  76.8771
Bandwidth (Hz)                :  112787

############################## Ac analysis (common mode gain )
Common Mode Gain (dB)         :  -35.7242
CMRR (dB)                     :  78.7436

############################## Ac analysis (power supply rejection +ve )
PSR+  (dB)                    :  -30.7946
PSRR+ (dB)                    :  73.814

############################## Ac analysis (power supply rejection -ve )
PSR- (dB)                     :  -1.84785E-07
Total Input Refered Noise (V):  2.28478E-05
Over Operating Frequency     :  1MEG

############################## slew rate
Slew Rate (V/sec)            :  2.07351E+06

############################## THD
Total Harmonic Distortion (%):  4.85748
@ Peak Voltage (V)           :  0.65
@ Operating Frequency  (Hz)  :  1k

############################## Monte carlo of Dc-gain (AV)
# run of AV        :  1000
Mean               :  4.12e+01
Standard Deviation :  5.37e+00
CP                 :  3.10
CPK                :  2.56

############################## Monte carlo of Gain BandWidth Product (GBW)
# run of GBW       :  1000
Mean               :  1.57e+07
Standard Deviation :  8.39e+05
CP                 :  9.73
CPK                :  5.84
############################## Monte carlo of Phase Margin (PM)
# run of PM        :  1000
Mean               :  7.66e+01
Standard Deviation :  2.86e+00
CP                 :  2.62
CPK                :  1.56

############################## Cost Evaluation (FOM)
FOM1=Cl*SR/Pd  (f.v/s.w)    :  1.62e-02
FOM2=Cl*GBW/Pd (f.Hz/w)     :  1.24e-01
```

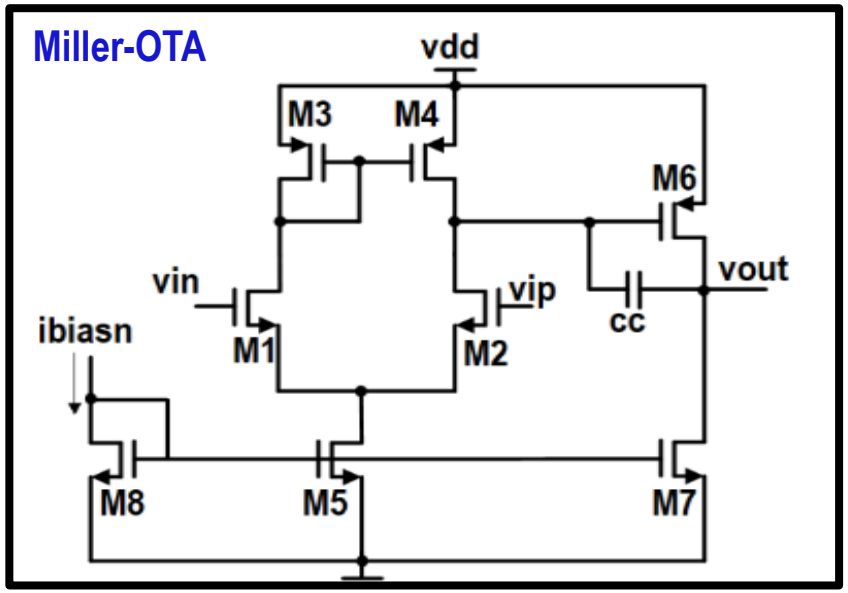


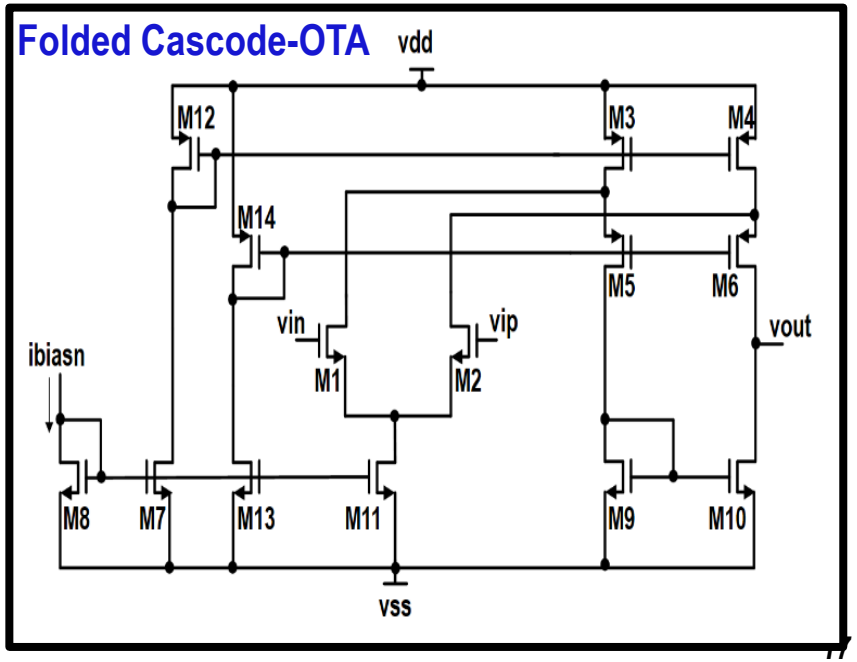




Case Study (7/8)

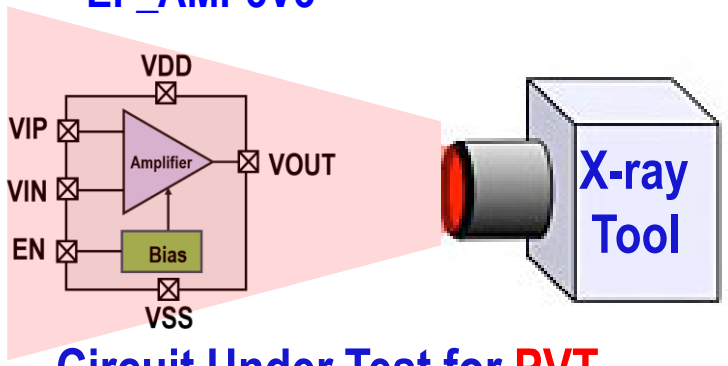
Analysis's Type	Item		Miller	Folded-Cascode
DC/DC Sweep	Total Current (A)		0.000176436	7.10188E-05
	Total Power (W)		0.000317585	0.000127834
	Offset (V)		0.0005257	0.0024598
	Vin_min (V)		0.54157	0.547968
AC Analysis	Dc-Gain (dB)		53.6652	43.0194
	Gain Bandwidth Product (Hz)		1.68395E+07	1.58434E+07
	Phase Margin (Deg)		69.1777	76.8771
	Bandwidth (Hz)		34962.6	112787
	CMRR (dB)		65.1424	78.7436
	PSRR+ (dB)		56.21563	73.814
	PSRR- (dB)		53.665	43.019
	Total Input Referred Noise (V) @ 1MEG		2.29288E-05	2.28478E-05
Transient Analysis	Slew Rate		908993	2.07351E+06
	Total Harmonic Distortion (%)@ Vpeak of 0.65 V and operating Frequency of 1kHz		0.943859	4.85748
Monte Carlo Analysis (1000 run)	DC-Gain	Mean	27.2	41.2
		Standard Deviation	15.9	5.37
		CP	1.05	3.1
		CPK	0.57	2.56
	GBW	Mean	7.74e+06	1.57e+07
		Standard Deviation	5.65e+06	8.39e+05
		CP	1.45	9.73
		CPK	0.4	5.84
FOM	FOM1=CI*SR/Pd (f.v/s.w)		2.86e-03	1.62e-02
	FOM2=CI*GBW/Pd (f.Hz/w)		5.30e-02	1.24e-01





Case Study (8/8)

EF_AMP3V3



Circuit Under Test for PVT

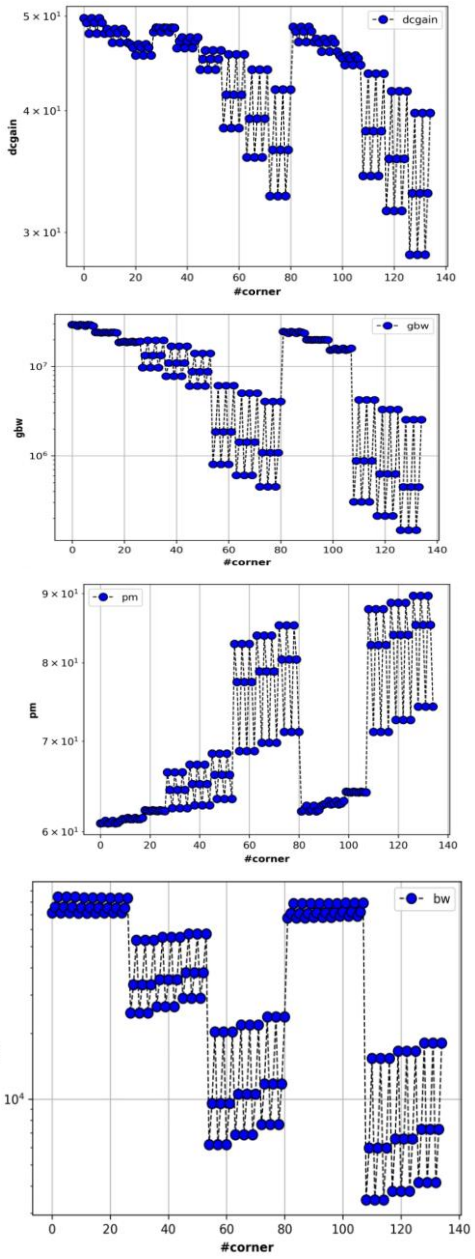
I have used my developed Xray tool to automate the simulation result, evaluate process/corner-voltage-temperature (PVT) of IP block, and report the results.

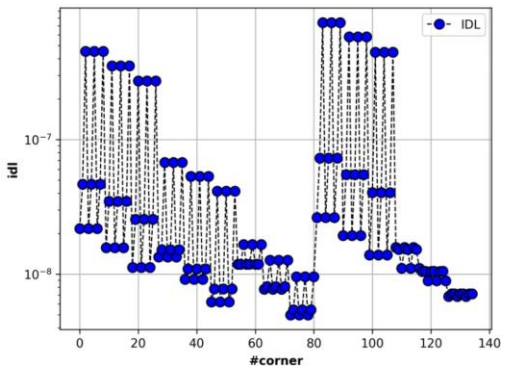
Process: tt, ff, ss,sf,fs
VDD: 3.3V,3.63V,2.97V
DVDD: 1.8V, 1.98V, 1.62V
Temp : 0°C, **25°C**, 85°C

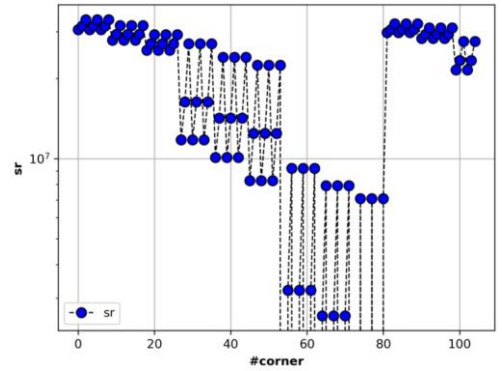
135 Corners

```
#!/usr/bin/env python3
import os
os.system('python xray4ampidlpvt.py')
os.system('python xray4ampcmpvt.py')
os.system('python xray4ampdmpvt.py')
os.system('python xray4ampcinpvt.py')
os.system('python xray4ampnoisepvt.py')
os.system('python xray4ampoffsetpvt.py')
os.system('python xray4ampsrpvt.py')
os.system('python xray4amppsrpvt.py')
os.system('python xray4ampthdpvt.py')
```

XRAY_EF_AMP3V3.py







Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
VDD	Analog Power Supply		2.97	3.3	3.63	V
IDL	Consumed Current	EN=0 V, VCM=1.65V	4.97	10.9	740	nA
IQ	Quiescent Current	EN=1.8 V, VCM=1.65V	3.81	107	370	µA
Vos	Input Offset Voltage	EN=1.8 V, Unity feedback	0.73	1.12	2.26	mV
VO	Voltage Range		0.052	1.65	1.89	V
A_V	Open Loop Gain		28.5	47.1	49.8	dB
A_{CM}	Common Mode Gain		-28.6	-8.9	-5.04	
GBW	Gain Bandwidth Product		0.147	10.9	29.5	MHz
BW	Bandwidth –3dB		3.46	35.3	84.5	KHz
PM	Phase Margin		60.9	65	89.7	°
CMRR	Common mode rejection ratio		44.4	56	57.1	dB
PSRR	Power Supply Rejection Ratio		51.7	61.8	66.2	
SR	Slew Rate	Step VIP from 0.9V to 2.4V, time rising/falling=100ns	2.5	10.1	33.3	V/µs
THD	Total Harmonic Distortion	V_{I_PEAK}=0.5V, Freq.=1KHz	0.0021	0.0027	0.89	%
		V_{I_PEAK} =1V, Freq =1KHz	0.0080	0.28	10.7	
		V_{I_PEAK} =0.5V, Freq =1000KHz	0.12	0.38	19	
		V_{I_PEAK} =1V, Freq =1000KHz	0.28	2.9	24.7	
Cin	Input capacitance		2.6	3.1	15	fF
	Input noise spectral density	Freq.=1Hz : Freq.=10KHz	96.7	115.3	163	$\mu V/\sqrt{Hz}$
		Freq.=10Hz : Freq.=10MHz	0.497	0.937	10.5	$mV/\sqrt{Hz}$
Temp	Temperature Range		0	25	85	°
	Core Silicon area	SKYWATER 130nm		37x53		μm^2

EF_AMP3V3

Outlines

- ❑ Motivation and Problem Statement
- ❑ X-ray Tool for Analog/Mixed Circuit
- ❑ Beyond Scene
- ❑ Case Study
- ❑ Conclusion

Conclusion

- An open-source script for trans., MC, and PVT analysis with process capability has been proposed.
- The script
  - relies open resources such as Xschem, Ngspice, SKYWATER PDK, and python.
  - acts as an Xray device to analysis and manage your circuits' test bench.
  - assists the designer to check of the results within process capability indices.
  - Save designer's time and increase productivity time.

Thanks!