instruction set Architecture <Risc || Cisc>

- Reduced instruction set computer ←
- Complex // // // ←

3*6

Risc (خطوات كتير / وقت سريع)	Cisc (خطوات قليله / وقت بطئ)
ADD	MulTi
3+3+3+3+3+3 = 18	3*6 = 18
10 instruction → 10 clk	3 inst → 11 clk
1 inst → 1 clk	1 inst → 3,4,5...clk
simple operations // Decoder → H.W	Complex decoder → S.W

ينفع يبقى H.W مع Cisc

وسمى super computer

	Risc (ARM)	Cisc (intel)
Performance	~	~
Cost	H.W ↓ S.W ↑ ~	H.W ↑ S.W ↓ ~
Size	Alu ↓ decoder ↑ ~	Alu ↑ decoder ↓ ~
Power	~	~

اللي يميز Risc → Pipe lining → Parrarism → 1 inst → 1 clk

Memory → Semi Conductor Memories < Voltile - non Voltile >

RAM <Voltile>

- DRAM → Based on Capacitors
- SRAM → Based on transistors

DRAM		SRAM
↓	Performance	↑ ✓
↑	Size	↓ ✓
↓ ✓	Cost	↑
↑	Power	↓ ✓

RoM < Non Voltile >

1. Maskable RoM → manufacture
2. OTP RoM → one time Program
3. EPRoM →(315) UV — erasable Programable Read only Memory
4. EEPRoM
5. Flash

	Flash	EEPRoM
Access	block Access 1B → 10ns 100B → 10ns	Byte Access 1B → 1ns 100B → 100ns
Cost	↓ ✓	↑

FGM ← عشان تكتب على الفلاش محتاج Power عالى اوى الـ Processor مبيقدرش عليه

Processor → Flash driver → Flash

← عشان اكتب على Flash محتاج Flash driver

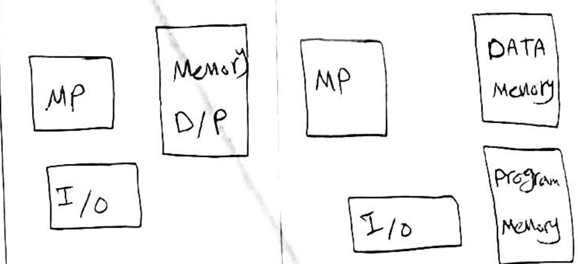
Program Memory	DATA Memory
R	R/W
Flash	SRAM → RAM

← اى سيستم لازم يبقى فيه <Flash & SRAM>

← ممكن يبقى فيه EEPRoM لما ممكن احتاج اخزن Data و SRAM ← Voltile

2 Designs

1. Von numen
2. Harvard



MC / MCu / ECu → SoC → embedded system

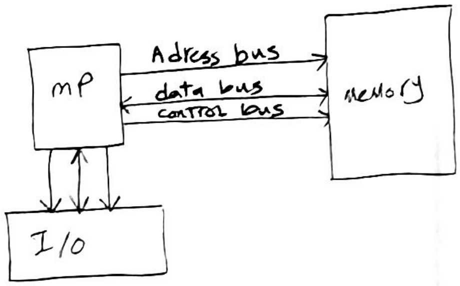
شركة design

- AVR → ابط
  - ATMeL → ATiny, ATmega 32
    - MP, SRAM 2k, DIO, ADC, Flash 32K, External Interrupt, UART, Timer, SPI
- ARM → اعقد

embeded system → computing system

Computer Functional blocks :

(1) MP (CPU) (2) Memory (3) I/O peripherals



Difference

in system
< Memory , I/O >

system on board → SOB | system on chip → SOC

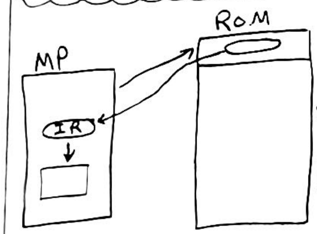
	SOB	SOC
Performance	~	~
size	↑	↓ (✓)
cost	↑	↓ (✓)
Power consumtion	↑	↓ (✓)
Configurability	↑ (✓)	↓

Configurability → امكانية التعديل و التغيير

R & D → Research and development <SOB>

Production → <SOC>

Instruction Life Cycle :



[1] Fetch :

بياخد نسخة من ال instruction الى عايز تتنفذ ويحطها فى instruction Register (IR)

[2] decode :

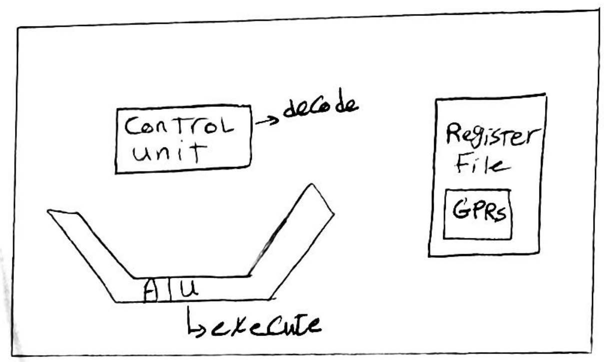
بعد كدا instruction بترجع لـ دائرة instruction Decoder علشان MP يعرف هيا بتتنفذ اى (اى output المتوقع)

[3] execute :

التنفيذ بقا

Micro processor :

Alu / Register File / Control unit



Alu <Arithmatic logic unit> :

مسئوله عن اى Arithmatic أو logic → operation

Control unit : control sequece of execution

جواه → (decoder)

Register File :

- PC (Program Counter): hold address of next inst-
- IR (Instruction register): hold instruction that will be decode <fetch>
- Stack Pointer: بيشاور على Top of stack
- GPRS: General Purpose registers → store temporary data

→ جمع ٣ ارقام جمع ٢ و تخزنهم فيهم وبعدكدا بجمعهم على التالت