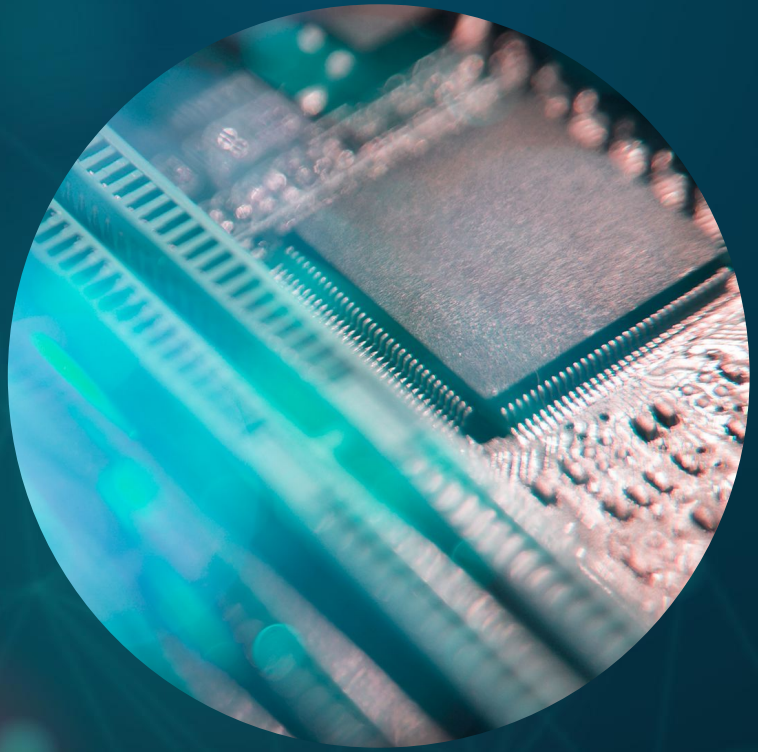
IMT SCHOOL

ARM Based Microcontroller

STP

Lecture 11



Advanced RISC Machines

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Introduction 01

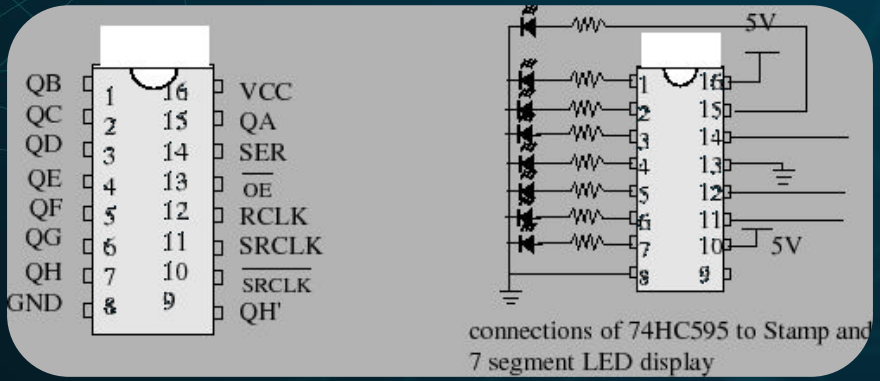
Serial To Parallel

Introduction

A serial-to-parallel device accepts a series of timed pulses and latches them onto a parallel array of output pins.

It is important to understand that the D-type flip- flop is a rising edge triggered device, and the data at its input transfers to the output only on the rising edge of the clock pulse.

The SN74HC595 devices contain an eight-bit serial- in, parallel-out shift register that feeds an 8-bit D-type storage register.

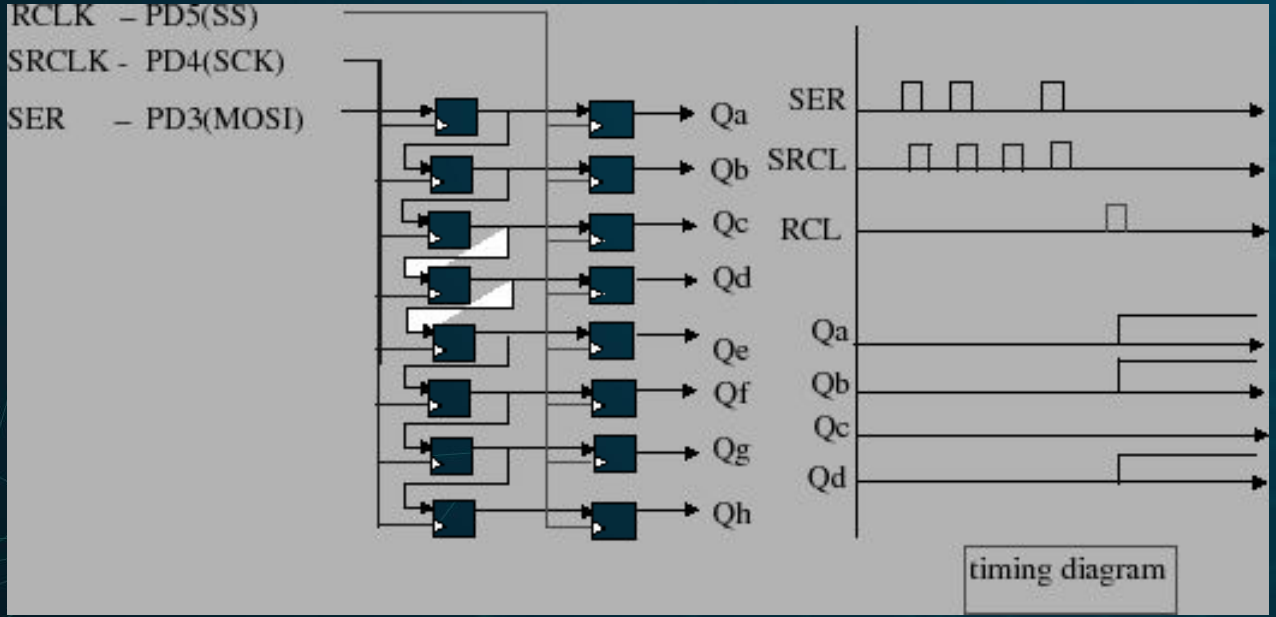


74HC595

The basic idea is to send a sequence of bits (i.e., positive pulses) down to the serial-to-parallel chip (74HC595). The 74HC595 will then convert this serial input into a parallel input and latch the output so it continues to drive the LED display until the next series of bits is received and latched. This operation, however, requires some degree of control. For instance, we need some way of telling the chip when the pulses are expected to occur and we need some way of telling the chip when to latch the data. This means that we need two control lines to the chip, in addition to the data line.

To understand how these control lines work, we need to take a closer look at how the 74HC595 functions. The 74HC595 consists of an interconnected set of simpler digital circuits known as latches. There are actually two banks (columns) of latches, each column consisting of 8 latches. Next figure shows these two columns. The first column of latches form something known as a shift register. This bank accepts the serial input and shifts each bit in the series of input pulses down into the column. The second column of latches is used to store what is in the first column. This second column is connected to the chip's output and is used to drive the LED display.
This frees up the first column to receive another series of inputs, without disrupting the actual signals delivered to the 7-segment display.

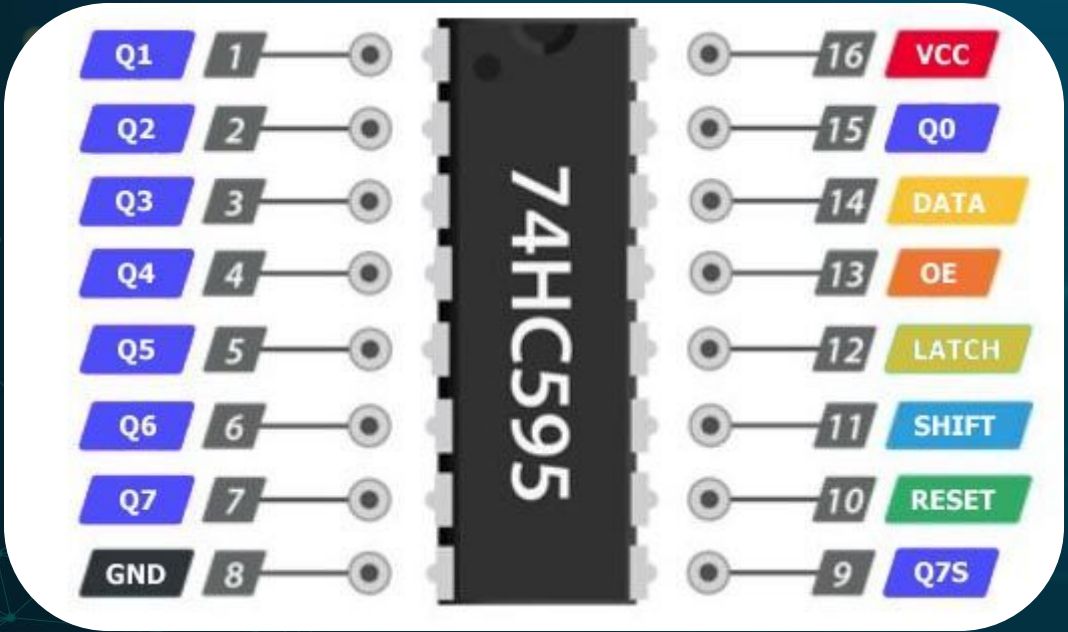
74HC595


RCLK – PD5(SS)
SRCLK - PD4(SCK)
SER – PD3(MOSI)
Qa
Qb
Qc
Qd
Qe
Qf
Qg
Qh
SER
SRCL
RCL
Qa
Qb
Qc
Qd
timing diagram

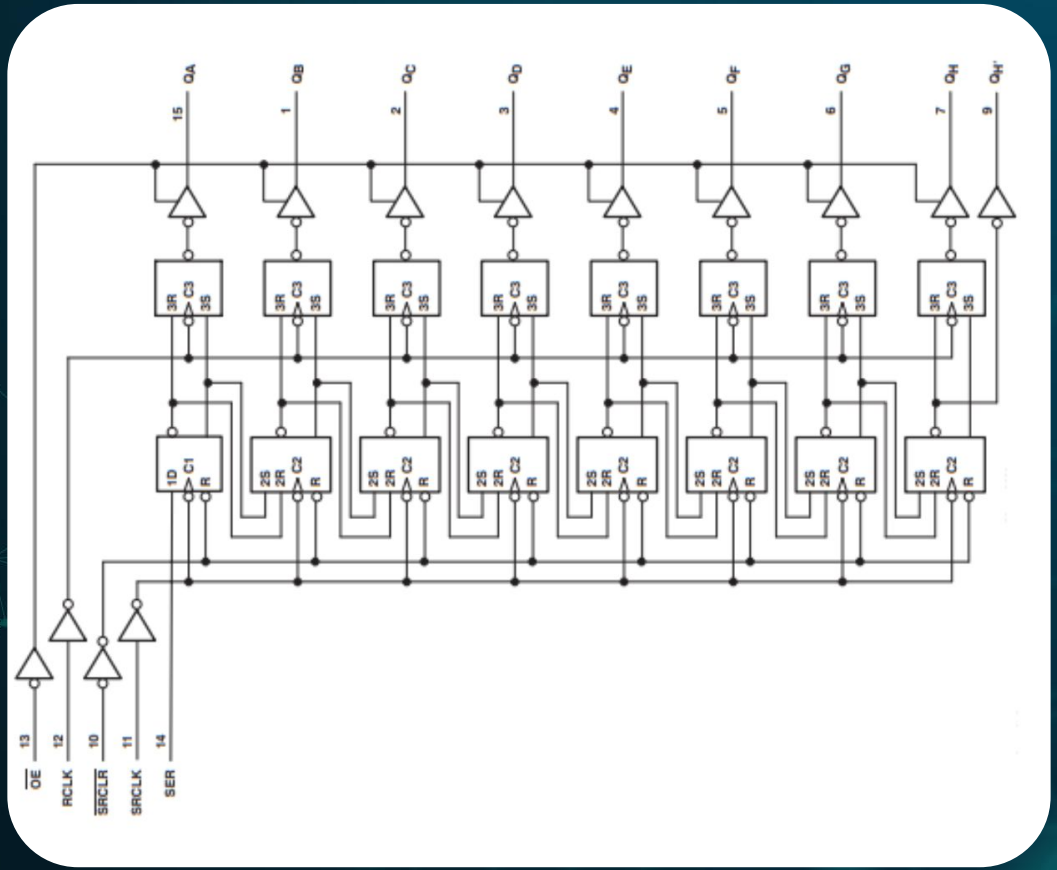
74HC595

Each latch is a digital circuit with two inputs and one output. The top input with the black arrowhead represents the data and the other input with the white arrowhead represents a control. The lines with the black arrowhead are connected to the pin marked SER (serial input) and the lines with white arrowheads are connected to the pin marked SRCLK. This line is sometimes called the clock line. When the data line (SER) is high and the control (SRCLK) is high, then the output of the latch is also high until it is reset. When the data (SER) is high and the control (SRCLK) is low, then the output does not change from its previously latched value. The first column of latches are daisy chained together so the output of the top latch is the data input to the second latch. What we do, therefore, is input a bit string into SER along with a SRCLK signal. Each time SRCLK goes high, the data in a latch is shifted to the latch below it. We can therefore enter a string of 8 bits into the first column of latches by sending each bit along the SER line and then setting the SRCLK line high for each bit of data. The timing diagram shown in figure shows how the bit string 1011 is shifted into the device. After the data has been shifted into the first column, we transfer this data in parallel to the second column of latches by setting the RCLK line high. This second column of latches will retain their value until we overwrite them with another RCLK signal.

74HC595


Q1
1
Q2
2
Q3
3
Q4
4
Q5
5
Q6
6
Q7
7
GND
8
74HC595
16
VCC
15
Q0
14
DATA
13
OE
12
LATCH
11
SHIFT
10
RESET
9
Q7S

74HC595


QA
QB
QC
QD
QE
QF
QG
QH
QH'
15
1
2
3
4
5
6
7
9
3R
C3
3S
1D
C1
R
2S
2R
C2
13
12
10
11
14
OE
RCLK
SRCLR
SRCLK
SER

74HC595

Input Pins It mainly has three pins are responsible to serial input (Data “SER_14”, Bit Latch “SRCLK_11” and Byte Latch “RCLK_14”).

Output Pins It mainly has eight pins responsible to parallel output (Bit_0 “Qa_15”, Bit_1 “Qb_1”, Bit_2 “Qc_2”, Bit_3 “Qd_3”, Bit_4 “Qe_4”, Bit_5 “Qf_5”, Bit_6 “Qg_6” and Bit_7 “Qh_7”).

Serial Output one pin responsible to serial output (Qh’_9).

Reset Pin SRCLK_10 pin is called a reset clock and is an active low pin, its function is to reset the internal circuit and clear all of stored data if this pin is connected to low signal.

Enable Pin OE_13 pin is called as an output enable pin, this pin is active low, so if you want the stored bits to appear on output pin, this pin must be connected to ground.

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74HC595 Work Summary

MSB First

Related to this method, the output will be sequentially from Qa_15 pin (which is the least significant bit) to Qh_7 (which is the most significant bit), so the arrangement of bits' Order will not affect

LSB First

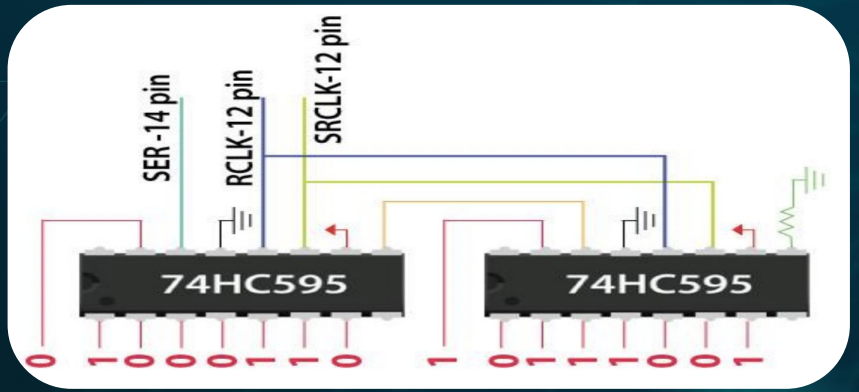
Related to the this method, the output will be reversely from Qa_15 pin (which is the least significant bit) to Qh_7 (which is the most significant bit), so the arrangement of bits' Order will be reversed

How to make unlimited O/P pins

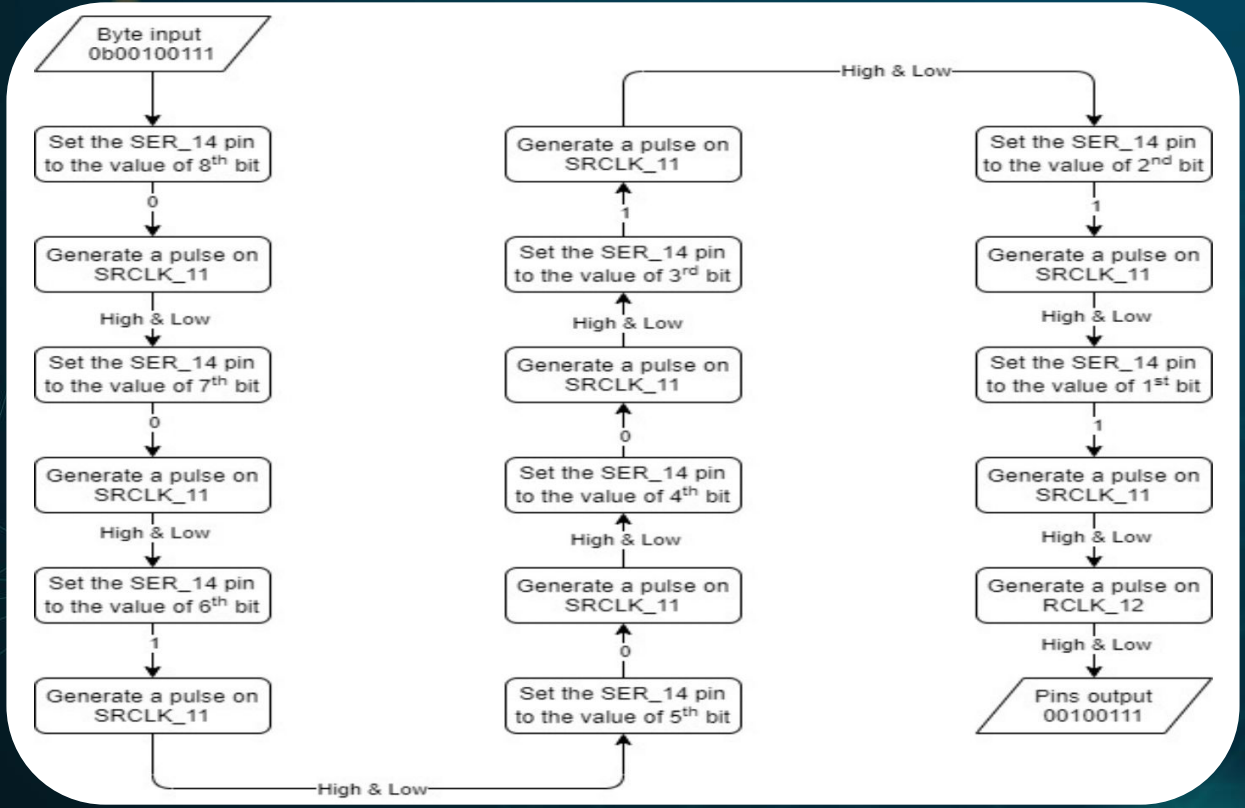
Qh'_9 pin is used to leak the additional bits, so if you want to out more than one byte, as example, two bytes, you must gian two ICs to do it and the SRCLK_11 and RCLK_12 pins must be connected in parallel and the Qh'_9 pin of the first IC must be connected to the SER_14 pin of the second IC to stored the leaked data from the first IC to the Second.

MSB order method is preferred in this case because this method doesn't affect the order arrangement of bits to be more logical and the least byte appears on the first and the highest byte on the second.

Assume that the sent data is "0b10011101011000 10" The output will be:



Shift Register Coding Diagram



STM32 Is AWESOME

Session LAb

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THANKS!

Do you have any questions?

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