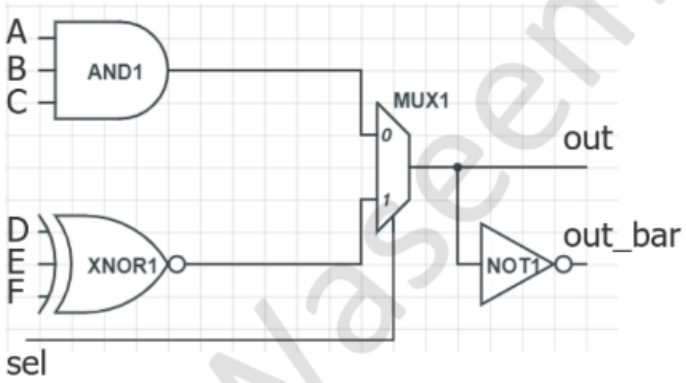
Assignment

TASK_1

- 1_Design half adder using gate-level modeling
- 2_Design full order using half _adder
- 3_Design 4_bit adder using full adder

Task_2

- The design has 7 inputs and 2 outputs
- Use assign statements to design the following



Task_3

4) Implement 2-to-4 Decoder using conditional operator (A logic decoder has n input lines and 2^n output lines. Each output line corresponds to a unique combination of the input values.)

- The design has input **A** (2 bits) and output **D** (4 bits)

A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Task_4

6) Implement a comparator that compares 2 inputs (**A, B**) and has 3 outputs using conditional operator.

- The first output **A_greaterthan_B** is high only when A is greater than B
- The second output **A_equals_B** is high only when A equals B
- The third output **A_lessthan_B is** high only when A is less than B

Inputs A and B are 4-bit bus while the 3 outputs are single bits.

- ALL TASKS YOU NEED TO WRITE THE CODE AND THEN SIMULATE IT IN THE QUESTASIM USING 5 CLOCKS TO SHOW THE WAVE AND CHECK YOUR DESIGN