Date : Subject :

Memory

- Volatile RAM
- non-Volatile ROM
- Hybrid

SRAM

Cache Memory

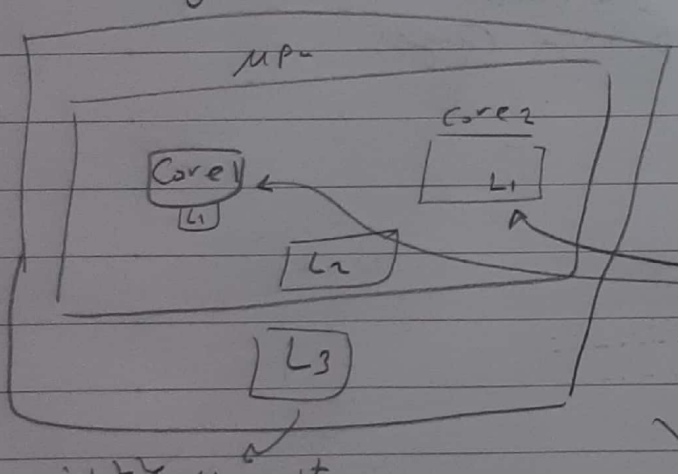
If it found the next data in the cache

hit

miss → if it didn't find it

CPU ↔ Cache ↔ RAM

it brings the address of data and the next data



is the slowest

Cache memory + Micro controller

The problem that may be the core changes the var value and core 2 didn't get the new change it's still has the old value

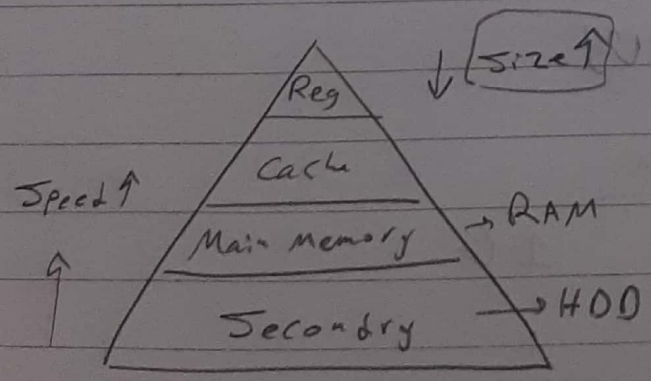
Cache Coherance

↳ it allows to change the variable in all controlers

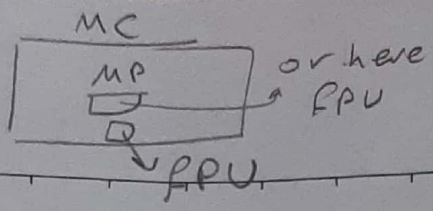
Register file → is the fastest memory

then the Cache

Hit ratio = $\frac{\#\text{ hits}}{\#\text{ total}}$



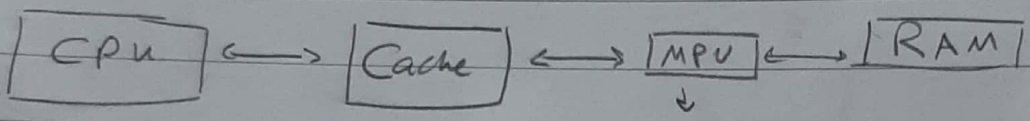
baraka



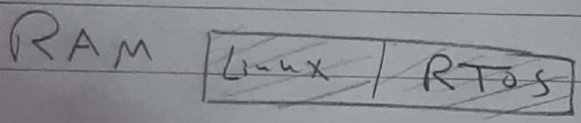
Date : Subject :

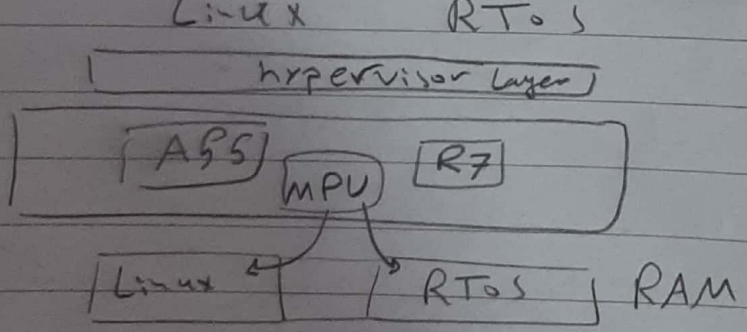
FPU & MPU & MMU

- FPU → Floating Point Unit → module to deal with float numbers
- MPU → memory protection Unit
- MMU → Memory management Unit



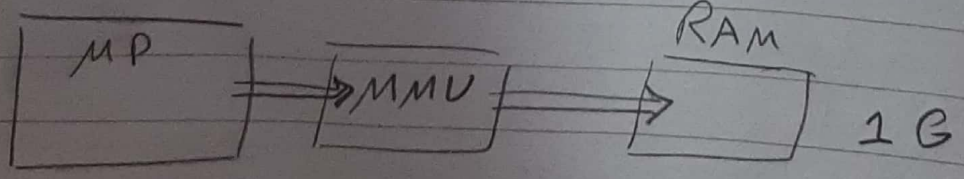
Control the RAM
divide it into ranges



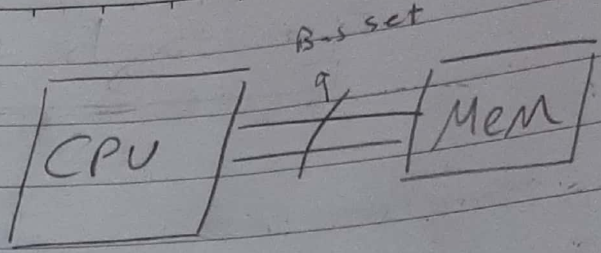


Memory management Unit (MMU)

APP → 8 GB



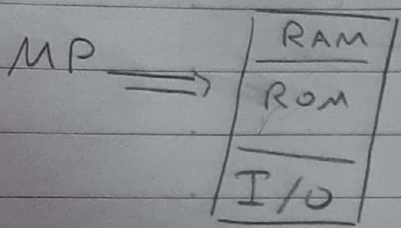
It's more related to Embedded Linux



Internal Arch

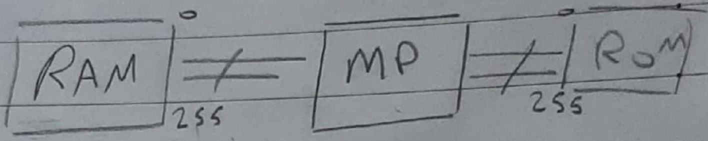
Von - neumen ⇐ Memory Mapped

One memory System



Each one has unique address

Harvard ⇒ Port Mapped



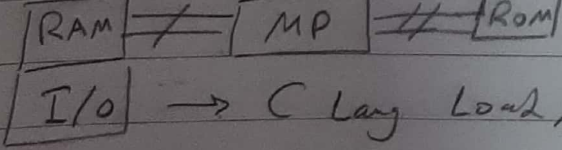
Sol ↳ SW

RAM: C Lang ⟸ Assem → Load/store (depends on Microprocessor)

ROM: R/W assem only

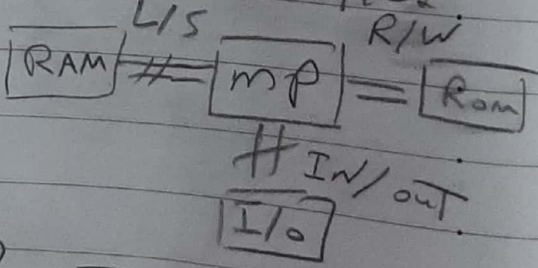
I/O (Harvard)

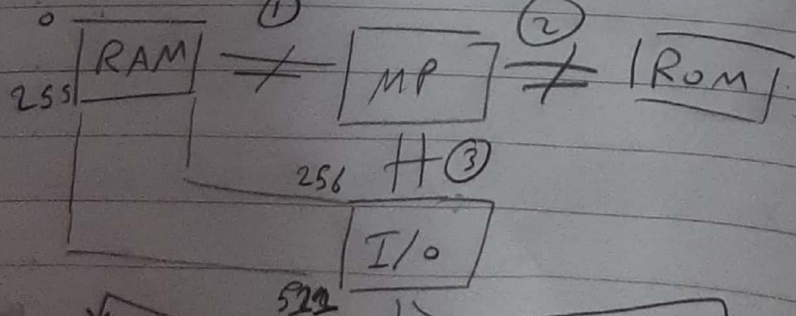
memory mapped



I/O → C Lang Load/store

Port mapped





Bus set ① ↳ C-language (Load/store)

Bus set ③ Assem I/O

Date : Subject :

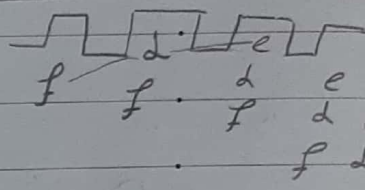
Arch

used in Computers → Von-neuman

Microprocessor take the code from the hard disk and put it in the RAM as dealing only with it.

used in MC → Harvard

its arch will be more suitable for Micro controler



⟹ Pipe Lining f d e

fetch decode execute

Von-ne ⟹ Can't support pipelinity

Harvard ⟹ support pipelinity

RISC → support pipelinity

one clock cycle finishes the instruc

CISC → ~~don't~~ don't support

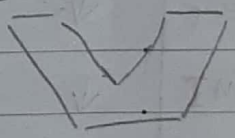
MIPS → Million instruction Per-se

ex 16 MiPS → 1 clock cycle

MC → n bit

↳ data bus

8bit 8bit

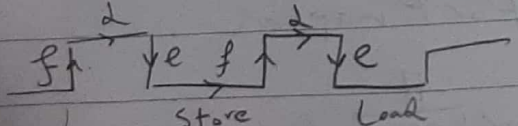


RISC → Hint → 1 cycle

8 MHz/s → 8 MIPS

clock → f, e, d

↳ square clock



$T \rightarrow f = \frac{1}{T} = 8\,MHz$

baraka

Date: Subject:

Clock System

electrical

RC Oscillator

555

Mechanical

material

ceramic crystal

electrical power

	RC	Ceramic	Crystal
Size	↓	In between	↑
Acc	↓ (x)	~	↑ ✓
Setting time	↑	~	↓ (✓)
Noise Immunity			
→ Temp	↓	↑ ✓	↑ ✓
→ EMI	↓	↑ ✓	↑ ✓
→ Vibra	↑ (✓)	↓ x	↓ x

Connection

Memory → ES → ex device (GPIO)

(Base) + (offeset) → Range

Port mapped

≠ CPU ≠

Date : Subject :

Technical Reference Manual

TRM → Tech (Ref_Man)

↓ it contains the specs.

| GPIO Base 0x0 End 0x~ | ← Memory map ↵

↳ GPIO
- DR 0x0+Base
- ODR
- IR

Ex SW to run a Led so we should put high on its pin.

① Pointer → DR → 1 (O/P)
↳ (Base+offset)
*

② Pointer → ODR → 1 (H)

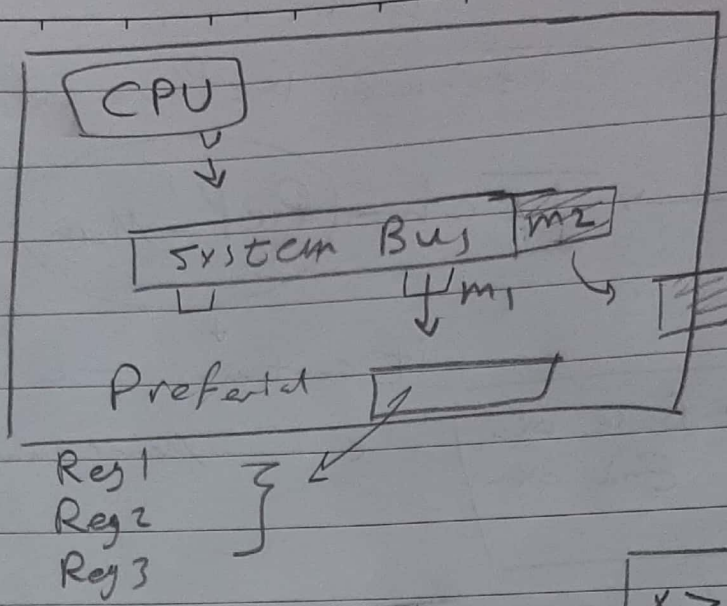
The CPU Initiate transaction
→ data (1)
→ Size (4 byte)
→ address (Base GPIO)

in master ①
→ transaction
↳ address (offset)
↳ data
Size

in the master ①

Date : Subject :

Ex



we increase the range to prevent any problem to happen

m1 → 0x0
-size (8 byte)
"12 Byte"

X > 12 B
↳ Reserved

Bus Bridge