# ASSIGNMENT 02:-
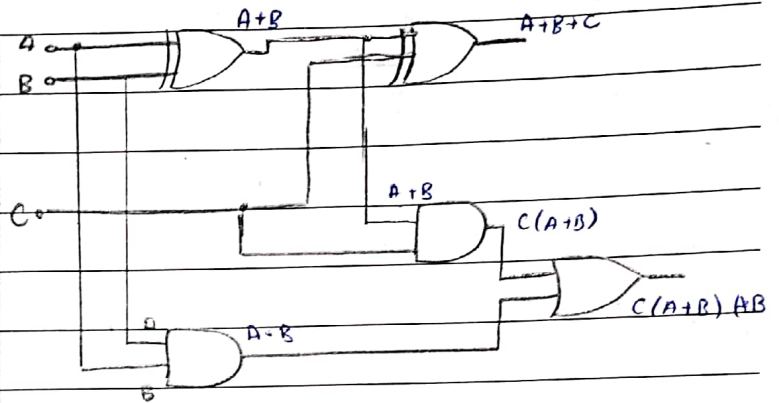
Date:____

AHMER AQEEL (15960) Bs-Cs

Question no 1: Design full adder and draw logic diagram?

| Inputs | | | Outputs | |
|---|---|---|---|---|
| A | B | C | Sum | Carry |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | ? |



GATE LEVEL DIAGRAM:-

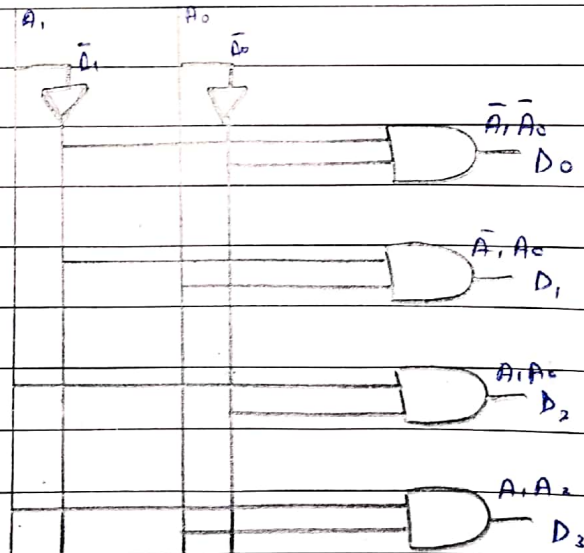Question no 2:- Design 1 to 4 line decoder with the help of Truth Table also draw gate level diagram;

| Input | | Outputs | | | |
|---|---|---|---|---|---|
| $A_1$ | $A_0$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |

$D_0 = \bar{A_1} \bar{A_0}$

$D_1 = \bar{A_1} A_0$

$D_2 = A_1 \bar{A_0}$

$D_3 = A_1 A_0$



GATE LEVEL DIAGRAM:-

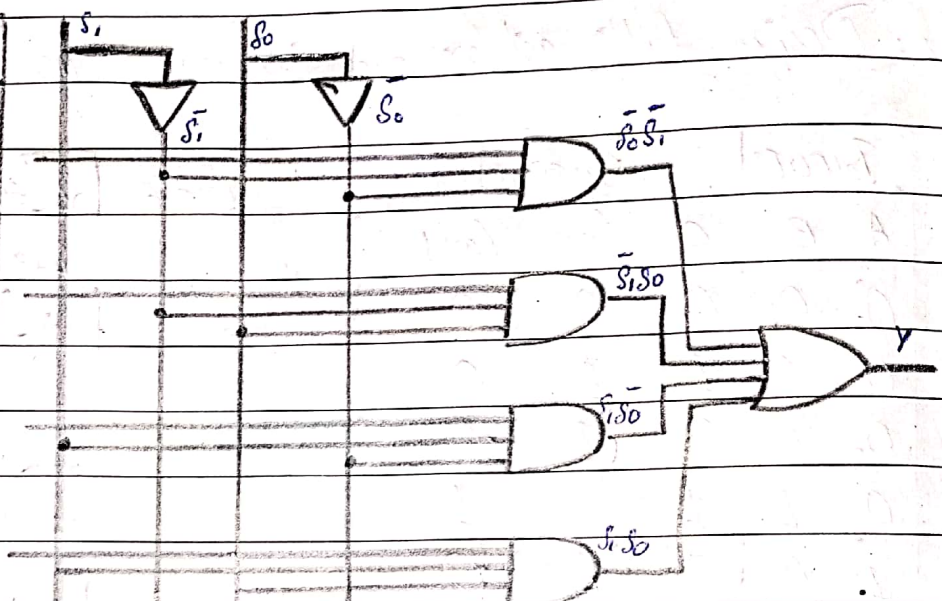**Q no 3 :** Design 4 input multiplexer and also write mathimatical equations

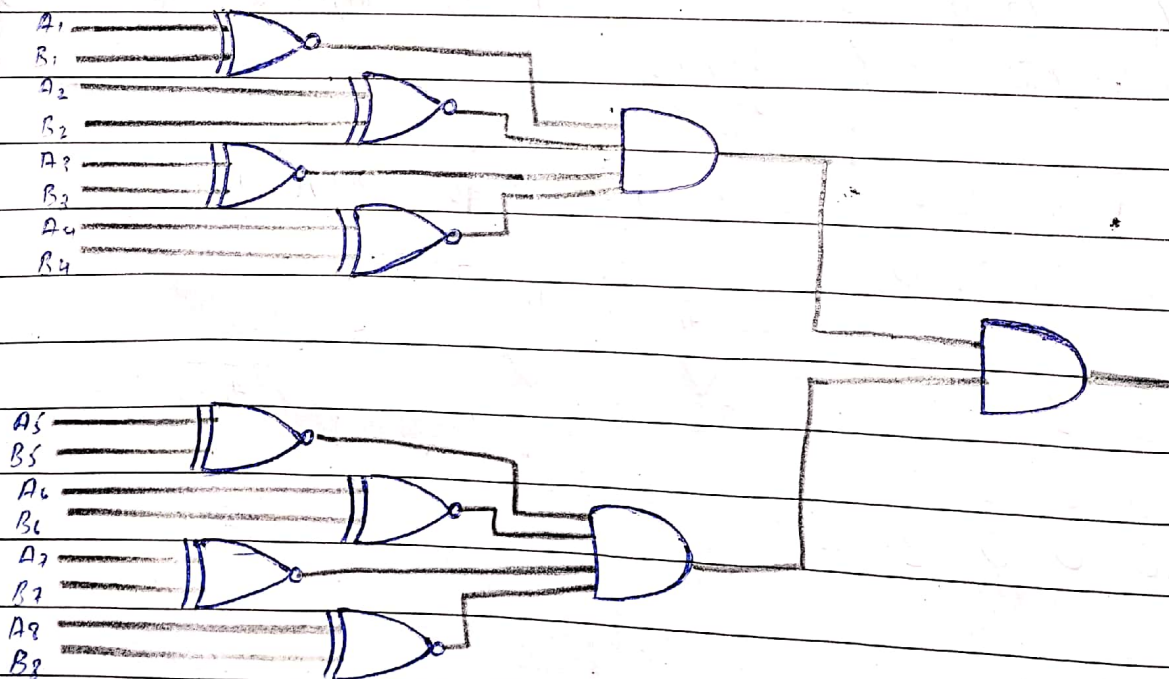| $S_1$ | $S_0$ | X |
|-------|-------|-----|
| 0 | 0 | $D_0$ |
| 0 | 1 | $D_1$ |
| 1 | 0 | $D_2$ |
| 1 | 1 | $D_3$ |

$$Y_0 = D_0 \bar{S_1} \bar{S_1}$$
$$Y_1 = D_0 \bar{S_1} S_0$$
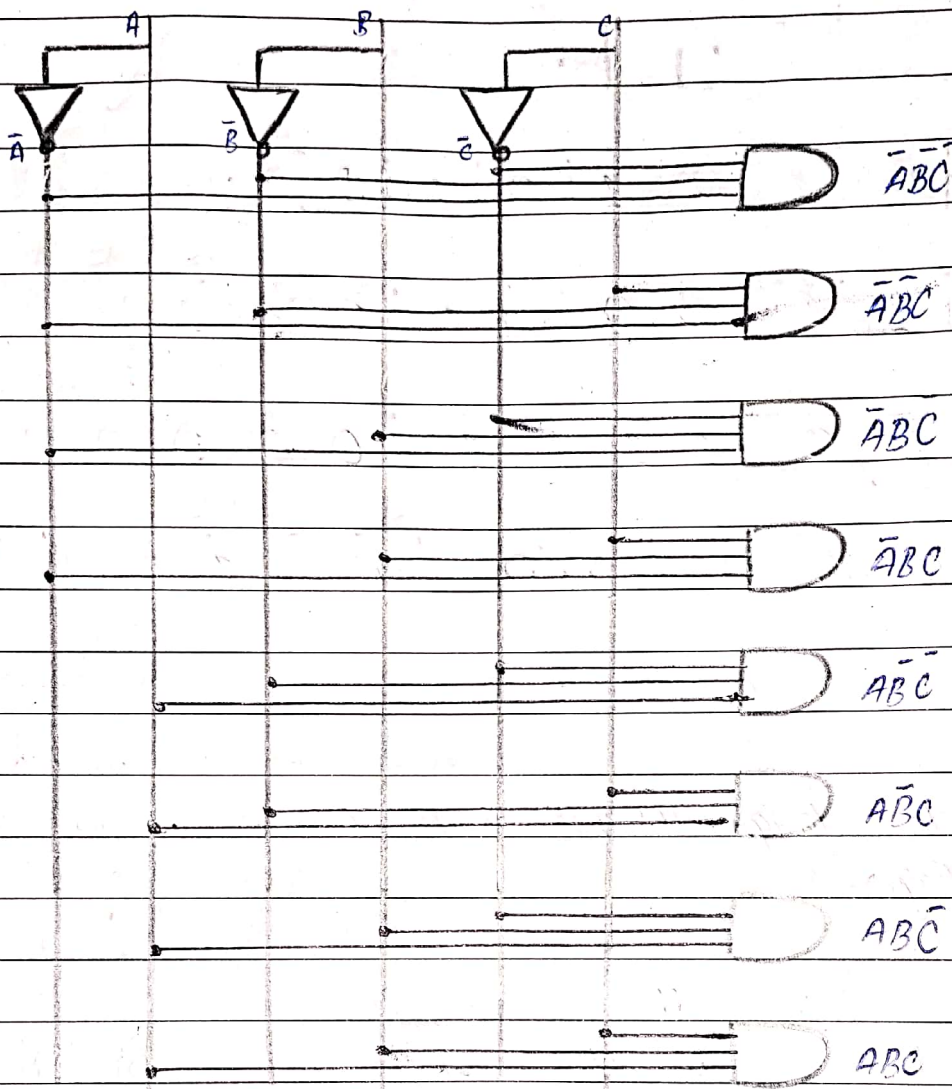$$Y_2 = D_0 S_1 \bar{S_0}$$
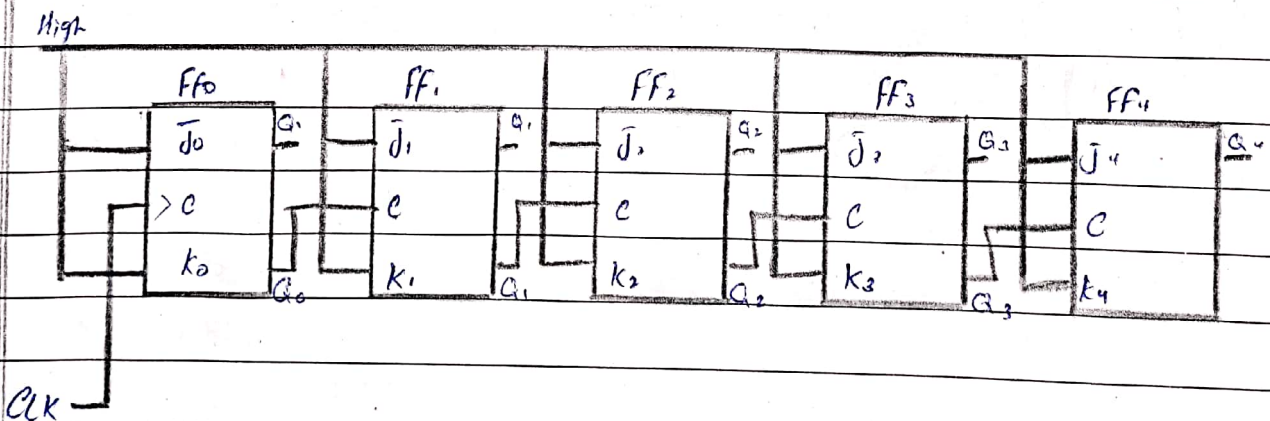$$Y_3 = D_0 S_1 S_0$$

**Q no 4 :** Design comparator to compare two 8 bit numbers with the help of gate level diagram.

Date:_____

Q no 5: Design 8 bit Demultiplexer with gate Level diagram?



A         B         C

$\bar{A}$   $\bar{B}$   $\bar{C}$

$\bar{A}\bar{B}\bar{C}$

$\bar{A}\bar{B}C$

$\bar{A}BC$

$\bar{A}BC$

$AB\bar{C}$

$A\bar{B}C$

$AB\bar{C}$

$ABC$

Q no 6: How to design 5 bit asynchronous counter? also draw wave form.

High



| FF0 | | FF1 | | FF2 | | FF3 | | FF4 | |
| $J_0$ | $Q_0$ | $J_1$ | $Q_1$ | $J_2$ | $Q_2$ | $J_3$ | $Q_3$ | $J_4$ | $Q_4$ |
| >C | | C | | C | | C | | C | |
| $k_0$ | $\bar{Q_0}$ | $K_1$ | $\bar{Q_1}$ | $k_2$ | $\bar{Q_2}$ | $k_3$ | $\bar{Q_3}$ | $k_4$ | |

CLK

VIP

WAVE FORM:

CLK :

| A | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| C | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| D | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| E | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Q NO 7 : How to design 4 bit Shift Register? Draw an complete diagram?

FF0             FF1             FF2             FF3

| $D_0$   $Q_0$ | | $D_1$   $Q_1$ | | $D_2$   $Q_2$ | | $D_3$   $Q_3$ |
|        C      | |        C      | |        C      | |        C      |

CLK :