FINALTERM EXAMINATION
Fall 2008
CS501- Advance Computer Architecture

Question No: 1 (Marks: 1) - Please choose one
Which one of the following is the memory organization of **SRC processor?**

- 2^8 * 8 bits
- 2^16 * 8 bits
- **2^32 * 8 bits (Page 46)**
- 2^64 * 8 bits

Question No: 2 (Marks: 1) - Please choose one
Type A format of SRC uses ----------instructions

- **Two (Page 47)**
- three
- four
- five

Question No: 3 (Marks: 1) - Please choose one
The instruction ----------will **load** the register R3 with the contents of the memory location M [PC+56]

- Add R3, 56
- lar R3, 56
- **ldr R3, 56 (Page 47)**
- str R3, 56

Question No: 4 (Marks: 1) - Please choose one
Which format of the instruction is called the accumulator?

- 3-address instructions
- 3-address instructions
- 2-address instructions
- **1-address instructions (Page 32)**
- 0-address instructions

Question No: 5 (Marks: 1) - Please choose one
Which one of the following are the **code size** and the **Number of memory bytes** respectively for a 2-address instruction?

- 4 bytes, 7 bytes
- **7 bytes, 16 bytes (Page 36)**
- 10 bytes, 19 bytes
- 13 bytes, 22 bytes

Question No: 6 (Marks: 1) - Please choose one
Which operator is used to name registers, or part of registers, in the Register Transfer Language?

- **:= (Page 66)**
- &
- %
- ©

Question No: 7 (Marks: 1) - Please choose one
The transmission of data in which each character is self-contained units with its own start and stop bits is ------

- **Asynchronous** Click here for detail
- Synchronous
- Parallel
- All of the given options

Question No: 8 (Marks: 1) - Please choose one
Circuitry that is used to move data is called ----------

- **Bus** click here for detail
- Port
- Disk
- Memory

Question No: 9 (Marks: 1) - Please choose one
Which one of the following is **NOT** a technique used when the CPU wants to exchange data with a peripheral device?

- Direct Memory Access (DMA).
- Interrupt driven I/O
- Programmed I/O
- **Virtual Memory (Page 268)**

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Question No: 10 (Marks: 1) - Please choose one
Every time you press a key, an interrupt is generated. **This is an example of**

- **Hardware interrupt (Page 275)**
- Software interrupt
- Exception
- All of the given

Question No: 11 (Marks: 1) - Please choose one
The interrupts which are pre-programmed and the processor automatically finds the address of the ISR using interrupt vector table are

- Maskable
- Non-maskable
- Non-vectored
- **Vectored (Page 277)**

Question No: 12 (Marks: 1) - Please choose one
Which is the last instruction of the ISR that is to be executed when the ISR terminates?

- **IRET (Page 278)**
- IRQ
- INT
- NMI

Question No: 13 (Marks: 1) - Please choose one
If NMI and INTR both interrupts occur simultaneously, then which one has the precedence over the other

- **NMI (Page 279)**
- INTR
- IRET
- All of the given

Question No: 14 (Marks: 1) - Please choose one
Identify the following type of serial communication error condition:
The prior character that was received was not still read by the CPU and is over written by a new received character.

- Framing error
- Parity error
- **Overrun error (Page 240)**
- Under-run error

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Question No: 15 (Marks: 1) - Please choose one
----------the device usually means reading its status register every so often until the device's status changes to indicate that it has completed the request.

- Executing
- Interrupting
- Masking
- **Polling** click here for detail

Question No: 16 (Marks: 1) - Please choose one
Which I/O technique will be used by a sound card that may need to access data stored in the computer's RAM?

- Programmed I/O
- Interrupt driven I/O
- **Direct memory access(DMA)** Click here for detail
- Polling

Question No: 17 (Marks: 1) - Please choose one
For increased and better performance we use _____ which are usually made of glass.

- Coaxial Cables
- Twisted Pair Cables
- **Fiber Optic Cables (Page 390)**
- Shielded Twisted Pair Cables

Question No: 18 (Marks: 1) - Please choose one
In _____ if we find some call party busy we can have provision of call waiting.

- **Delay System (Page 381)**
- Loss System
- Single Server Model
- None of the given

Question No: 19 (Marks: 1) - Please choose one
In ____ technique memory is divided into segments of variable sizes depending upon the requirements.

- Paging
- **Segmentation (Page 365)**
- Fragmentation
- None of the given

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Question No: 20 (Marks: 1) - Please choose one
For a request of data if the requested data is not present in the cache, it is called a _____

- **Cache Miss (Page 358)**
- Spatial Locality
- Temporal Locality
- Cache Hit

Question No: 21 (Marks: 1) - Please choose one
An entire _____ memory can be erased in one or a few seconds which is much faster than EPROM.

- PROM
- Cache
- EEPROM
- **Flash Memory (Page 356)**

Question No: 22 (Marks: 1) - Please choose one
_____chips have quartz windows and by applying ultraviolet light data can be erased from them.

- PROM
- Flash Memory
- **EPROM (Page 356)**
- EEPROM

Question No: 23 (Marks: 1) - Please choose one
The _____signal coming from the CPU tells the memory that some interaction is required between the CPU and memory.

- **REQUEST (Page 350)**
- COMPLETE
- None of the given

Question No: 24 (Marks: 1) - Please choose one
_____ is a combination of arithmetic, logic and shifter unit along with some multiplexers and control unit.

- Barrel Rotator
- Control Unit
- Flip Flop
- **ALU (Page 347)**

Question No: 25 (Marks: 1) - Please choose one
In Multiple Interrupt Line, a number of interrupt lines are provided between the _____ modules.

- **CPU and the I/O (Page 283)**
- CPU and Memory
- Memory and I/O
- None of the given

Question No: 26 (Marks: 1) - Please choose one
The data movement instructions _____ data within the machine and to or from input/output devices.

- Store
- Load
- Move
- **None of given (Page 141)**

Question No: 27 (Marks: 1) - Please choose one
CRC has ---------- overhead as compared to Hamming code.

- Equal
- Greater
- **Lesser (Page 329)**
- None of the given

Question No: 28 (Marks: 1) - Please choose one
The _____ is w-bit wide and contains a data word, directly connected to the data bus which is b-bit wide memory address register (MAR) .

- Instruction Register(IR)
- memory address register (MAR)
- **memory Buffer Register(MBR) (Page 350)**
- Program counter (PC)

Question No: 29 (Marks: 1) - Please choose one
In_____technique, a particular block of data from main memory can be placed in only one location into the cache memory .

- Set Associative Mapping
- **Direct Mapping (Page 360)**
- Associative Mapping
- Block Placement

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Question No: 30 (Marks: 1) - Please choose one
_____ indicate the availability of page in main memory.

- Access Control Bits
- Used Bits
- **Presence Bits** click here for detail
- None of the given

FINALTERM EXAMINATION
FALL 2006
CS501 - ADVANCE COMPUTER ARCHITECTURE

Question No: 1 (Marks: 1) - Please choose one
The _____ RTN describes the overall effect of instructions on the programmer visible registers.

- ►**Abstract** click here for detail
- ►Concrete
- ►Absolute
- ►Basic

Question No: 2 (Marks: 1) - Please choose one
The instruction set is of _____ importance in governing the structure and function of the pipeline.

- ►Least
- ►**Primary** click here for detail
- ►Secondary
- ►No

Question No: 3 (Marks: 1) - Please choose one
_____ is the most general and least useful performance metrics for RISC machines.

- ►**MIPS** click here for detail
- ►Instruction Count
- ►Number of registers
- ►Clock Speed

Question No: 4 (Marks: 1) - Please choose one
A _____ provides four functions: Select, DataIn, DataOut and Read/Write.

►ALU
►Bus
►Register
►**Memory Cell (Page 351)**

Question No: 5 (Marks: 1) - Please choose one
We can classify or partition the SRC instructions by their overall _____ behavior.

►**Register transfer** click here for detail
►Memory transfer
►Execution
►Logical

Question No: 6 (Marks: 1) - Please choose one
The _____ RTN describes detailed register transfer steps in the data path that produce the overall effect.

►Abstract
►**Concrete** click here for detail
►Absolute
►Basic

Question No: 7 (Marks: 1) - Please choose one
All members of the MC68000 family are _____ processors.

►**32-bit** click here for detail
►16-bit
►64-bit
►8-bit

Question No: 8 (Marks: 1) - Please choose one
_____ Operations refers to a processor that can issue more than one instruction simultaneously.

►Macro
►Micro
►Scalar
►**Superscalar** click here for detail

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Question No: 9 (Marks: 1) - Please choose one
Exceptions which are _____ occur in response to events that are paced by the internal processor clock.

- ► Asynchronous
- ► **Synchronous** click here for detail
- ► Internal
- ► External

Question No: 10 (Marks: 1) - Please choose one
In the hazard detection by hardware, resolved by pipeline stalls, if the instructions are in the adjoining stages, then the hazard must be detected in stage _____.

- ► 4
- ► 2
- ► **3** click here for detail
- ► 1

FINALTERM EXAMINATION
SPRING 2006
CS501 - ADVANCE COMPUTER ARCHITECTURE

Question No: 1 (Marks: 3) - Please choose one
16k x4 static RAM Chip is arranged in the form of four _____ cells.
►16x512
►32x512
►256x512
►64x256 (Page 352)

Question No: 2 (Marks: 3) - Please choose one
In a DRAM cell, the storage capacitor will discharge in around _____
►4 -15 ms (Page 354)
►2 - 10 ms
►5-20 ms
►10-25 ms

Question No: 3 (Marks: 3) - Please choose one
1-bit sign, 8-bit exponent, 23-bit fraction and a bias of 127 is used for _____ Binary Floating Point Representation
►Double precision
►**Single Precision (Page 348)**
►All of above
►Half Precision

Question No: 4 (Marks: 3) - Please choose one
The average rotational latency if the disk rotated at 20,000rpm is _____
►0.5 ms
►3.5 ms
►2.5 ms
►**1.5 ms (Page 324)**

Question No: 5 (Marks: 3) - Please choose one
A hard disk with 5 platters has 1024 tracks per platter, 512 sectors per track and 512 bytes/sector. What is the total capacity of the disk?
►1.5 GB
►**1 GB (Page 324)**
►2 GB
►3 GB

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CS501 – Final Term Quizzes

Quiz No.3 (Fall 2012)

Question # 1 of 10 (Total Marks: 1) Select correct option:
Where does the processor store the address of the first instruction of the ISR?

Interrupt vector (Page 277)
Interrupt request
Interrupt handler
All of the given options

Question # 2 of 10 (Total Marks: 1) Select correct option:
In _____, a separate address space of the CPU is reserved for I/O operations.

Isolated I/O (Page 236)
Memory Mapped I/O
All of above
None of above

Question # 3 of 10 (Total Marks: 1) Select correct option:
---------- is the time needed by the CPU to recognize (not service) an interrupt request.

Interrupt Latency (Page 279)
Response Deadline
Timer delay
Throughput

Question # 4 of 10 (Total Marks: 1) Select correct option:
_____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.

Microprogramming
Instruction pre-fetching
Pipelining
Partial decoding (Page 255)

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Question # 5 of 10 (Total Marks: 1) Select correct option:
How can you define an interrupt?

A process where an external device can speedup the working of the microprocessor
A process where memory can speed up programs execution speed
A process where an external device can get the attention of the microprocessor **click here for detail**
A process where input devices can takeover the working of the microprocessor

Question # 6 of 10 (Total Marks: 1) Select correct option:
An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.

Flip Flops
Memory
Peripheral devices (Page 234)
Multiplexers

Question # 7 of 10 (Total Marks: 1) Select correct option:
A software routine performed when an interrupt is received by the computer is called as ---------

Interrupt
Interrupt handler **click here for detail**
Exception
Trap

Question # 8 of 10 (Total Marks: 1) Select correct option:
Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?

Daisy-Chaining Priority
Asynchronous Priority
Parallel Priority (Page 281)
Semi-synchronous Priority

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Quiz No.3 (Fall 2012)

Question # 1 of 10 (Total Marks: 1) Select correct option:
In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?

Asynchronous
Daisy-Chaining Priority **Click here for detail**
Parallel
Semi-synchronous

Question # 2 of 10 (Total Marks: 1) Select correct option:
Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)?

Framing error **(Page 240)**
Parity error
Overrun error
Under-run error

Question # 3 of 10 (Total Marks: 1) Select correct option:
Identify the following type of serial communication error condition in which no character is available at the beginning of an interval.

Framing error
Parity error
Overrun error
Under-run error **(Page 240)**

Question # 4 of 10 (Total Marks: 1) Select correct option:
_____ is an electrical pathway through which the processor communicates with the internal and external devices attached to the computer.

Computer Bus **click here for detail**
Hazard
Memory
Disk

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Question # 5 of 10 (Total Marks: 1) Select correct option:
Connection to a CPU that provides a data path between the CPU and external devices, such as a keyboard, display, or reader is called----------

processer
program
Buses **click here for detail**
memory address

Question # 6 of 10 (Total Marks: 1) Select correct option:
VLIW stands for ----------

Very Lengthy Interaction Word
Very Length Instruction Width
Very Long Instruction Word **(Page 219)**
none of given options

Question # 7 of 10 (Total Marks: 1) Select correct option:
A ----------is a wiring scheme in which, for example, device A is wired to device B, device B is wired to device C, device C is wired to device D etc.

Daisy chain **click here for detail**
DMA
Interrupt driven I/O
Polling

Question # 8 of 10 (Total Marks: 1) Select correct option:
An ---------- is the memory address of an interrupt handler.

Interrupt vector **click here for detail**
Interrupt service routine
Exception
Mask

Question # 9 of 10 (Total Marks: 1) Select correct option:
The conversion of numbers from a representation in one base to another is known as_____
Radix Conversion **(Page 333)**
Number Representation
Decimal representation
Hexadecimal Representation

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Question # 10 of 10 (Total Marks: 1) Select correct option:
If an interrupt is set by the timer component or by the peripheral device then how would you categorize it?
Hardware **click here for detail**
Software
Exception
All of the given options

Quiz No.3 (Fall 2012)

Question # 1 of 10 (Total Marks: 1) Select correct option: 1
In which one of the following interrupts the device have to supply the address of the subroutine to the Microprocessor
Maskable
Non-maskable click here for detail
Non-vectored
Vectored

Question # 2 of 10 (Total Marks: 1) Select correct option:
---------- interrupts are usually associated with the software
hardware
software click here for detail
machine
internal

Question # 3 of 10 (Total Marks: 1) Select correct option:
When the address of the subroutine is already known to the Microprocessor then it is called as --------- interrupt.
Maskable
Non-maskable
Non-vectored
Vectored click here for detail

Question # 4 of 10 (Total Marks: 1) Select correct option:
How Interrupt driven I/O is better than polling because?

Interrupt driver I/O is easy to design
Interrupt driver I/O is enhanced version of polling.
Interrupt driver I/O does not waste time on checking which device is available. (Page 274)
Interrupt driven I/O is easy to program.

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