MIDTERM EXAMINATION CS302- Digital Logic Design (Session - 6)

Question No: 1 (Marks: 1) - Please choose one The maximum number that can be represented using unsigned octal system is **▶** 1 **▶** 9 ▶ 16 **Ouestion No: 2** (Marks: 1) - Please choose one If we add "723" and "134" by representing them in floating point notation i.e. by first, converting them in floating point representation and then adding them, the value of exponent of result will be _____ **▶** 0 **▶** 1 **>** 3 Question No: 3 (Marks: 1) - Please choose one The diagram given below represents _____ ► Demorgans law ► Associative law **▶** Product of sum form ► Sum of product form Question No: 4 (Marks: 1) - Please choose one The range of Excess-8 code is from _____ to ____ ► +7 to -8 \rightarrow +8 to -7 \rightarrow +9 to -8 -9 to +8**Ouestion No: 5** (Marks: 1) - Please choose one A non-standard POS is converted into a standard POS by using the rule _____

- A+A=1
- $A\overline{A} = 0$
- 1+A=1
- A+B=B+A

Question No: 6 (Marks: 1) - Please choose one

The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

- **•** 4
- **8**
- **▶** 12
- ▶ 16

Question No: 7 (Marks: 1) - Please choose one

The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

- ightharpoonup A > B = 1, A < B = 0, A < B = 1
- A > B = 0, A < B = 1, A = B = 0
- A > B = 1, A < B = 0, A = B = 0
- A > B = 0, A < B = 1, A = B = 1

Question No: 8 (Marks: 1) - Please choose one

A particular Full Adder has

- ▶ 3 inputs and 2 output
- ▶ 3 inputs and 3 output
- ► 2 inputs and 3 output
- ▶ 2 inputs and 2 output

Question No: 9 (Marks: 1) - Please choose one

The function to be performed by the processor is selected by set of inputs known as

- **►** Function Select Inputs
- ► MicroOperation selectors
- ► OPCODE Selectors
- ► None of given option

Question No: 10 (Marks: 1) - Please choose one

For a 3-to-8 decoder how many 2-to-4 decoders will be required?



► 1 ► 3
▶ 4
Question No: 11 (Marks: 1) - Please choose one
GAL is an acronym for
► Giant Array Logic
► Glant Array Logic ► General Array Logic
► Generic Array Logic
► Generic Analysis Logic
Question No: 12 (Marks: 1) - Please choose one
The Quad Multiplexer has outputs
▶ 4
▶ 8
► 12 ► 16
Question No: 13 (Marks: 1) - Please choose one
A.(B.C) = (A.B).C is an expression of
► Demorgan's Law
➤ Distributive Law
Commutative Law
► Associative Law
Question No: 14 (Marks: 1) - Please choose one
2's complement of any binary number can be calculated by
 adding 1's complement twice adding 1 to 1's complement
subtracting 1 from 1's complement.
► calculating 1's complement and inverting Most significant bit
Question No: 15 (Marks: 1) - Please choose one
The binary value "1010110" is equivalent to decimal
▶ 86
► 87
▶ 88
▶ 89
Question No: 16 (Marks: 1) - Please choose one

Tri-State Buffer is basically a/an gate.
► AND
► OR
► NOT
► XOR
Overtion No. 17 (Marker 2)
Question No: 17 (Marks: 2) For what values of A, B, C and D, value of the expression given below will be logic 1. Explain at
least one combination.
$\overline{A.\overline{B} + \overline{\overline{A.\overline{B.C.D}}}}$
7.5 7 7.5.0.5
Ans:
Question No: 18 (Marks: 2)
provide some of the inputs for which the adjacent 1s detector circuit have active high
output?
Ans:
The Adjacent 1s Detector accepts 4-bit inputs.
If two adjacent 1s are detected in the input, the output is set to high.
input combinations will be
1. 0011, 2. 0110,
3. 0111,
4. 1011,
5. 1100,
6. 1101,
7. 1110 and 8. 1111
o. 1111
the output function is a 1.
Question No: 19 (Marks: 2)
Draw the Truth-Table of NOR based S-R Latch

S	R	Action
0	0	Keep state
0	1	Q=0
1	0	Q=1
1	1	Restricted combination

Question No: 20 (Marks: 3)

For a two bit comparator circuit specify the inputs for which A > B

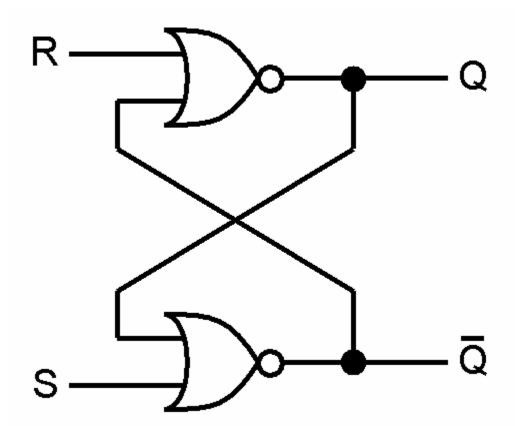
Ans:

- 1. 01 00,
- 2. 10 00,
- 3. 10 01,
- 4. 11 00,
- 5. 11 01 and
- 6. 11 10

Question No: 21 (Marks: 3)

Draw the circuit diagram of NOR based S-R Latch?

Ans:



Question No: 22 (Marks: 5)

One of the ABEL entry methods uses logic equations; explain it with at least a single example.

Ans:

In ABEL any letter or combination of letters and numbers can be used to identify variables.

ABEL however is case sensitive, thus variable 'A' is treated separately from variable 'a'.

All ABEL equations must end with ';'

Boolean expression F = AB' + AC + (BD)' is written in ABEL as F = A & !B # A & C # !B & !D;

Question No: 23 (Marks: 5)

Explain Carry propagation in Parallel binary adder?

Ans:

Parralel binary adder:

A binary adder circuit is described using dynamic transistor logic in which for high speed carry propagation the adder stages are grouped in pairs or larger numbers and additional dynamic logic means is provided in each group to control a single transistor connected in series in the carry propagation path over the group.

The transistors used in the specific embodiments are MOS transistors, but some or all of these could be replaced by junction FET's or bipolar transistors.

was my CS302 DLD paper. Total 23 questions out of which 16 MCQ's.

2 questions of two marks each were from the topic Adder. A boolian expression wes given and had to find a logic 1 for it. One 5 marks question from parity method.

2day was my 2nd paper of cs302 this was my papers

SOP to POS conversion 3mark
S-R latch Diagram 5mark
Nor gate table 3mark
8 to 3 bit encoder 5mark
Tri-stuff diagram 3mark

mcqz zyda tar start lec mn say aye thay binary additin 2's complemnt k-map

Assalam o Alaikum

Today I attempted CS302 paper

Paper was of 38 marks.

16 MCQs and 22 marks paper comprised of long questions.

2 marks question was "Write the uses of multiplexer".

2 marks question was "Write any two advantages of boolean expressions".

2 marks question was "Draw the diagram of odd parity generator circuit".

3 marks question was "What does a 8-bit adder/subtracter circuit do"?

3 marks question was "Draw the function table of 3 to 8 decoder".

5 marks question was "Describe 16 bit ALU".

5 marks question was "Describe in your own words about latches".