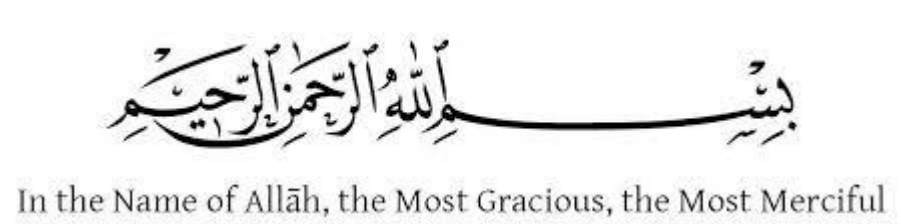

Final-Term Papers Solved MCQs CS501- Advance Computer Architecture

1. What is the instruction length of the FALCON-A processor?

   - 8 bits
   - **16 bits** **PG # 91**
   - 32 bits
   - 64 bits

2. What is the working of **Processor Status Word** (PSW)?

   - **To hold the current status of the processor.** **PG # 25**
   - To hold the address of the current process
   - To hold the instruction that the computer is currently processing
   - To hold the address of the next instruction in memory that is to be executed

3. What functionality is performed by the instruction "**str R8, 34"** of SRC?

   - it will load the register R8 with the contents of the memory location M [PC+34]
   - It will load the register R8 with the relative address itself (PC+34).
   - **It will store the register R8 contents to the memory location M [PC+34]** **PG # 48**
   - No operation

4. FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is _____ wide.

   - 8-bits
   - 24-bits
   - **32-bits** **PG # 157**
   - 64-bits

5. **op<4..0>:= IR<15..11>:**
   The above RTL instruction presents the _____ of the FALCON-A Instructions.

   - **operation code field** **PG # 105**
   - target register field
   - operand or address index
   - second operand

6. Which one of the following register holds the address of the next instruction to be executed?

   - Accumulator
   - Address Mask
   - Instruction Register
   - **Program Counter** **PG # 151**

7. Which one of the following register holds the instruction that is being executed?

   - Accumulator
   - Address Mask
   - **Instruction Register** **PG # 152**
   - Program Counter

8. _____ operation is required to change the processor's state to a known, defined value.

   - Change
   - **Reset** **PG # 194**
   - Update
   - Halt

9. Type B format of SRC uses ----------instructions

- Two
- **Three** **PG # 47**
- Four
- Five

10. _____ control signal enable the CON circuitry to operate, and instruct it to check for the appropriate condition (whether it is branch if zero, or branch if not equal to zero, etc.)

- ECON
- BCON
- **LCON** **PG # 184**
- VCON

11. In which one of the following addressing modes, data is the part of the instruction itself, and so there is no need of address calculation?

- Direct Addressing Mode
- **Immediate addressing mode** **PG # 40**
- Indirect Addressing Mode
- Register (Direct) Addressing Mode

12. _____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.

- **Partial decoding** **PG # 255**
- Full encoding
- Partial multiplexing
- Half encoding

13. Every time you press a key, an interrupt is generated; this is an example of _____.

- Hardware interrupt
- Compile time error
- Run time error
- Internal interrupt

14. _____ refers to the situation in which all I/O operations are performed under the direct control of a program running on the CPU.

- Direct memory access
- Virtual memory
- Partial decoding
- **Programmed I/O** **PG # 268**

15. CPU can exchange data with a peripheral device using _____ technique.

- Memory Contention
- **Direct Memory Access** **PG # 269**
- Pre-fetching
- Pipelining

There are three main techniques using which a CPU can exchange data with a peripheral device, namely
• Programmed I/O
• Interrupt driven I/O
• Direct Memory Access (DMA).

16. ---------- is the time needed by the CPU to recognize (not service) an interrupt request

- **Interrupt Latency** **PG # 279**
- Response Deadline
- Timer delay
- Throughput

17. In which one of the following methods, does the CPU poll to identify the interrupting module and branch to an interrupt service routine on detecting an interrupt?

- Multiple interrupt lines
- **Software Poll** **PG # 283**
- Daisy Chain
- Parallel Priority

18. Which one of the following is a fixed size structure that stores the address of the first instruction of ISR?

- **Interrupt vector** **PG # 277**
- Interrupt request
- Interrupt handler
- Boot Sector

19. In Multiple Interrupt Lines approach, a number of interrupt lines are provided between the _____ modules.

- External and Internal
- **CPU and I/O** **PG # 283**
- CPU and Memory
- Memory and I/O

20. In FALCON-A assembler and simulator (FALSIM), variables are defined by using the _____ directive.

- .bin
- .equ
- .iret
- **.end** **PG #9**

دنیا کی سب سے بڑی فتح نفس پر قابو رکھنا ہے

21. _____ allows a peripheral device to read from and/or write to memory without intervention by the CPU.

- Programmed I/O
- Interrupt driven I/O
- **Direct memory access** **PG # 316**
- Polling

22. Taking control of the system bus for a few bus cycles is known as _____.

- Bus Scheduling
- **Cycle Stealing** **PG # 317**
- Cycle Transferring
- CPU Scheduling

23. A Hard Disk sector has the _____ parts.

- Header only
- Data section and a trailer
- Data section only
- **Header, data section and a trailer** **PG # 323**

24. Raid Level ____ is not a true member of the RAID family.

- **0** **PG # 330**
- 2
- 3
- 4

25. The conversion of numbers from a representation in one base to another is known as_____

- **Radix Conversion** **PG # 333**
- Number Representation
- Decimal Representation
- Hexadecimal Representation

26. A _____signal decides whether the input word should be shifted or bypassed.

- Control Read
- **Shift/bypass** **PG # 346**
- Control Write
- Control Transfer

27. In Single-Precision Binary Floating Point Representation the size of exponent is _____.

- **8-bits** **PG # 348**
- 11-bits
- 1-bits
- 23-bits

28. In Double-Precision Binary Floating Point Representation the size of fraction is _____.

- 23-bits
- **52-bits** **PG # 348**
- 11-bits
- 1-bits

29. For a request of data if the requested data is not present in the cache, it is called a _____

- **Cache Miss** **PG # 358**
- Spatial Locality
- Temporal Locality
- Cache Hit

30. For a request for data, if the data is available in the cache it results in a ____.

- Cache Miss
- Spatial Locality
- Temporal Locality
- **Cache Hit** **PG # 358**

31. For write to complete in Write through, the CPU has to wait. This wait state is called _____.

- Write Through
- Write Back
- Write Allocate
- **Write Stall** **PG # 363**

32. _____ contains permanent pattern of data that cannot be changed.

- RAM
- Hard Disk
- Cache
- **ROM** **PG # 356**

33. In Control Field of page table, _____ indicate the availability of page in main memory.

- Access Control Bits
- Used Bits
- **Presence Bits** **PG # 367**
- Redundant Bits

34. _____ are formed by concatenating the page number with the word number.

- Memory chips
- Protocols
- Hazards
- **Virtual addresses** **PG # 366**

35. In _____technique memory is divided into segments of variable sizes depending upon the requirements.

- Multiplexing
- **Segmentation** **PG # 365**
- Hamming code
- Partial decoding

36. _____ depends upon the average number of calls and the service time taken by a particular server.

- **Through put** **PG # 380**
- Latency
- Poisson Distribution
- Response Time

37. _____ is the maximum rate at which data can be transmitted through networks.

- Transmission Time
- Latency
- Transport Latency
- Bandwidth **PG # 388**

38. The time for the message to pass through the network, except the time of flight is called _____.

- **Transmission Time** **PG # 388**
- Latency
- Transport Latency
- Bandwidth

39. In physical media of networks, for increased and better performance we use _____ which are usually made of glass.

- Coaxial Cables
- Twisted Pair Cables
- **Fiber Optic Cable** **PG # 390**
- Shielded Twisted Pair Cables

40. What does the instruction “ldr R3, 58” of SRC do?

- **it will load the register R3 with the contents of the memory location M [PC+58]**
- It will load the register R3 with the relative address itself (PC+58).
- It will store the register R3 contents to the memory location M [PC+58]
- No operation

41. What functionality is performed by the instruction “lar R3, 36” of SRC?

- It will load the register R3 with the contents of the memory location M [PC+36]
- **It will load the register R3 with the relative address itself (PC+36).** **PG # 48**
- It will store the register R3 contents to the memory location M [PC+36]
- No operation

42. What is the instruction length of the FALCON-E processor?

- 8 bits
- 16 bits
- **32 bits** **PG # 124**
- 64 bits

43. Type A format of SRC uses ----------instructions

- **two** **PG # 47**
- three
- four
- five

44. Which instruction is used to store register to memory using relative address?

- ld instruction
- ldr instruction
- lar instruction
- **str instruction** **PG # 48**

45. There are _____ types of reset operations in SRC

- **Two** **PG # 195**
- Three
- Four
- Five

46. Which one of the following is a bi-stable device, capable of storing one bit of Information?

- Decoder
- **Flip-flop** **PG # 76**
- Multiplexer
- Diplexer

47. Execution time of a program with respect to the processor is calculated as:

- Execution Time = IC x CPI x MIPS
- **Execution Time = IC x CPI x T** **PG # 44**
- Execution Time = CPI x T x MFLOPS
- Execution Time = IC x T

48. Which one of the following register stores a previously calculated value or a value loaded from the main memory?

- **Accumulator**
- Address Mask
- Instruction Register
- Program Counter

Accumulator
Accumulator is located in CPU. Accumulator stores a previously calculated value or a value loaded from the main memory. Without an accumulator it would be necessary to write the result of each calculation to main memory and read them back. Access to main memory is slower than access to the accumulator which usually has direct paths to and from the ALU.

جھوٹ انسان اور ایمان دونوں کا دشمن ہے

49. Which one of the following is called 0-address machine?

- General purpose register machines
- RISC machines
- Accumulator based machines
- **Stack based machines** **PG # 31**

50. Which one of the following type of error occurs when a character is not available at the beginning of an interval?

- Framing error
- Parity error
- Over-run error
- **Under-run error** **PG # 240**

51. Which one of the following type of error occurs when a 0 is received instead of a stop bit (which is always a 1)?

- **Framing error** **PG # 240**
- Parity error
- Over-run error
- Under-run error

52. An interface that is used to connect the computer bus with I/O devices is called _____.

- Buffer
- **I/O port** **PG # 245**
- Memory mapping
- Processor

53. Consider Falcon A, with 16 address lines, the total address space is _____ Kbytes.

- **2 ^ 16** **PG # 256**
- 2 ^ 10
- 2 ^ 6
- 2 ^ 8

2^{16} = 64 Kbytes.

54. _____ is the process of periodically checking the status of a device to see if it is ready for the next I/O operation.

- **Polling** **PG # 270**
- Snooping
- Data Bus Multiplexing
- Pipelining

55. Which one of the following is **NOT** a technique used when the CPU wants to exchange data with peripheral device?

- Direct Memory Access
- Interrupt driven I/O
- Programmed I/O
- **Virtual Memory** **PG # 268**

There are three main techniques using which a CPU can exchange data with a peripheral device, namely
• Programmed I/O
• Interrupt driven I/O
• Direct Memory Access (DMA).

56. Which one is the last instruction of the ISR that is to be executed when the ISR terminates?

- IRET PG # 278
- IRQ
- INT
- NMI

57. Which one of the following is a fixed size structure that stores the address of the first instruction of ISR?

- Interrupt request
- Interrupt handler
- Boot Sector
- **Interrupt vector** **PG #277**

58. Falcon-A Simulator loads a FALCON-A binary file with a _____ extension and presents its contents into different areas of the simulator.

- .bin
- **.binfa** **PG # 2**
- .fa
- .asmfa

59. In Direct memory access (DMA), a _____ is needed to control the total activity and to synchronize the transfer of data.

- DMA memory unit
- **DMA controller** **PG 313**
- Control software
- Programmed I/O

60. _____ allows a peripheral device to read from and/or write to memory without intervention by the CPU.

- **Direct memory access** **PG # 316**
- Polling
- Programmed I/O
- Interrupt driven I/O

جو شخص ناکامیوں سے ڈر کر بھاگتا ہے کامیابی اُس سے ڈر کر بھاگتی ہے

61. A component connected to the system bus and having control of it during a particular bus cycle is called _____.

- Address decoder
- BIOS
- **Master component** **PG # 317**
- Slave component

62. When it is required to read data from a particular location of the disk, the head moves towards the selected track and this process is called_____.

- **Seek** **PG # 322**
- Encoding
- Fragmentation
- Defragmentation

63. CRC has _____overhead as compared to Hamming code.

- Equal
- Greater
- **Lesser** **PG # 329**
- Absolutely no

64. _____ is the simplest form for representing a signed number.

- **Sign Magnitude Form** **PG # 330**
- Radix Complement Form
- Biased Representation
- Diminished Radix Compliment Form

65. In _____ adder circuit we feed carry out from the previous stage to the next stage and so on.

- **Ripple Carry Adder** **PG # 335**
- Carry Look Ahead Adder
- Complement Adder
- 2's Complement Adder

66. _____ are computed by the ALU and stored in processor status register.

- **Condition Codes** **PG # 344**
- Control Signals
- Flip Flops
- Multiplexers

67. In computers, floating-point representation uses _____to encode significant, exponent and their sign in a single word.

- Decimal Numbers
- **Binary Numbers** **PG # 341**
- Octal Numbers
- Hexadecimal Numbers

68. In floating point representations _____ is also called mantissa.

- Sign
- Base
- **Significant** **PG # 341**
- Exponent

69. A _____signal decides whether the input word should be shifted or bypassed.

- Control Read
- **Shift/bypass** **PG # 340**
- Control Write
- Control Transfer

70. For a request of data if the requested data is not present in the cache, it is called a _____.

- **Cache Miss** **PG # 349**
- Spatial Locality
- Temporal Locality
- Cache Hit

71. Randomly replacing any older page to bring in the desired page is known as _____.

- Always Replacement
- LFU (Least Frequently Used)
- **Random Replacement** **PG # 356**
- Fragmentation

72. In Control Field of page table, _____ indicate the availability of page in main memory.

- Access Control Bits
- Used Bits
- **Presence Bits** **PG # 356**
- Redundant Bits

73. A set of rules followed by different components in a network is called _____.

- Host
- Connectivity
- Resource Sharing
- **Protocol** **PG # 373**

74. In _____ topology, all the computers are connected in the form of a circle.

- Bus
- **Ring** **PG # 381**
- Mesh
- Star

75. SPARC (Scalable Processor Architecture) is an example of _____architecture.

- CISC
- **RISC** **PG # 148**
- SRC
- FALCON

76. Which one of the following is the memory organization of EAGLE processor?

- 2^8 * 8 bits
- **2^16 * 8 bits** **PG # 120**
- 2^32 * 8 bits
- 2^64 * 8 bits

Memory organization is 2^16 x 8 bits. This means that there are 216 memory cells, each one byte long

77. Which one of the following is the memory organization of **SRC processor**?

- 2^8 * 8 bits
- 2^16 * 8 bits
- **2^32 * 8 bits** **PG # 46**
- 2^64 * 8 bits

78. _____ is a collection of binary digits or bits that the computer reads and interprets.

- Assembly language
- Higher level language
- English language
- **Machine language** **Click Here For Reference Detail**

79. In which one of the following addressing modes, the value to be stored in memory is obtained by directly retrieving it from another memory location?

- **Direct Addressing Mode** **Click Here For Reference Detail**
- Immediate addressing mode
- Indirect Addressing Mode
- Register (Direct) Addressing Mode

جو لوگوں کے سامنے فخر کرتا ہے وہ لوگوں کی نظروں سے گر جاتا ہے

80. The external interface of FALCON-A consists of a _____address bus and _____a data bus.

- 8-bit, 8-bit
- **16-bit, 16-bit** **Click Here For Reference Detail**
- 16-bit, 24-bit
- 16-bit, 32-bit

81. In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?

- Arithmetic/logic
- **Load/store** **PG # 141**
- Test/branch
- None of the given

82. The _____ instruction is completed once memory access has been made and the memory location has been written to.

- **Store** **PG # 208**
- Branch
- Load
- Control

83. Which type of instructions enables mathematical computations?

- **Arithmetic** **PG # 92**
- Control
- Data transfer
- Miscellaneous

84. _____ Control signal allows the bus to read from the selected register.

- RBE
- RCE
- LCON
- **R2BUS** **PG # 182**

85. For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.

- Registers
- **Control signals** **Page # 171**
- Memory
- DMA controllers

86. Every I/O port has a unique identifier associated with it, which is called its _____.

- **Address** **PG # 244**
- Access point
- Interval Identifier
- Device Driver

87. Partial decoding is an attractive choice in _____.

- **Small system** **PG # 255**
- Large system
- Medium system
- All of the above

88. Maskable Interrupts are applied to the _____ pin of the processor.

- **INTR** **PG # 275**
- NMI
- IRET
- INT

89. Non-maskable Interrupts are detected using the _____ pin of the processor.

- INTR
- **NMI** **PG # 275**
- IRET
- INT

90. In Multiple Interrupt Line, a number of interrupt lines are provided between the ____ modules.

- External and Internal
- **CPU and the I/O** **Page # 283**
- CPU and Memory
- Memory and I/O

91. In ____ recording, bits are encoded in pairs so there are only ' n/2' additions instead of 'n'.

- Booth Recording
- **Bit-Pair Recording** **Page # 343**
- Fraction Division
- Integer Division

92. _____ is nonvolatile i.e. it retains the information in it when power is removed from it.

- RAM
- DRAM
- **ROM** **PG # 356**
- SRAM

93. Based on the statistical results, the block which has been least used in the recent past, is replaced with a new block. This technique is called _____.

- Always Replacement
- Random Replacement
- **LFU (Least Frequently Used)** **Page # 362**
- Write Allocate

94. _____ acts as a cache between main memory and secondary memory.

- Read Only Memory
- Flash Memory
- **Virtual Memory** **PG # 364**
- Magnetic Tape

95. _____is also called traffic intensity and its value must be between 0 and 1.

- Little's Law
- Poisson Distribution
- **Server Utilization** **PG # 381**
- SPEC

96. What is the instruction length of SRC processor?

- 8 bits
- 16 bits
- **32 bits** **PG # 134**
- 64 bits

EAGLE	FALCON-A	FALCON-E	SRC
Variable 8 bits or 16 bits	Fixed 16 bits	Fixed 32 bits	Fixed 32 bits

97. What does the word 'D' in the 'D-flip-Flop' stands for?

- **Data** **PG # 76**
- Digital
- Dynamic
- Double

98. Almost every commercial computer has its own particular ---------- language

- **assembly language** **PG # 25**
- English language
- Higher level language
- 3GL

عقل مند آدمی اس وقت تک نہیں بولتا جب تک خاموشی نہیں ہو جاتی

99. Which field of the machine language instruction is the "**type of operation**" that is to be performed?

- **Op-code (or the operation code)** **PG # 33**
- CPU registers
- Memory cells
- I/O locations

100. _____ is/are defined as the time required to process a single instruction.

- **Latency & throughput** **PG # 203**
- Latency
- Throughput
- Hazards

101. In pipelining _____ is increased by overlapping the instruction execution

- Latency
- **Throughput** **PG # 220**
- Execution time
- Clock speed

102. Which of the following register(s) takes input from the ALSU as the address of the memory location to be accessed and transfers the memory contents on that location onto memory sub-system?

- Instruction Register
- **Memory address register** **PG # 151**
- Memory Buffer register
- Registers A and C

103. _____ occurs when the exponent is too large and can not be represented in the exponent field.

- Underflow
- **Overflow** **PG # 348**
- Rounding off
- Normalize

104. The _____ is w-bit wide and contains a data word, directly connected to the data bus which is b-bit wide memory address register (MAR).

- Instruction Register(IR)
- memory address register (MAR)
- **memory Buffer Register(MBR)** **PG # 350**
- Program counter (PC)

105. The_____is m-bits wide and contains memory address generated by the CPU directly connected to the m-bit wide address bus.

- **memory address register (MAR)** **PG # 350**
- Accumulator register
- Program counter register
- Instruction register

106. _____ is a place for safe storage and provides the fastest possible storage after the registers.

- Hard Disk
- **Cache** **PG # 356**
- Compact Disk
- Floppy Disk

107. _____ refers to the interconnection of machines in a building or a campus.

- SAN
- **LAN** **PG # 387**
- WAN
- MAN

108. What is the size of the memory space that is available to **SRC processor**?

- 2^8 bytes
- 2^16 bytes
- **2^32 bytes** **PG # 46**
- 2^64 bytes

109. Which operator is used to name registers, or part of registers, in the Register Transfer Language?

- **:=** **PG # 66**
- &
- %
- ©

110. Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?

- **Processor-Memory-Switch level (PMS level)** **PG # 22**
- Instruction Set Level
- Register Transfer Level
- None of the given

111. Which one of the following design levels is called the gate level?

- **Logic Design Level** **PG # 22**
- Circuit Level
- Mask Level
- None of the given

112. _____ Instructions usually involve calculating the target address and evaluating a condition.

- Add
- **Branch** **PG # 209**
- Load
- Store

113. Which of the instruction is used to load register from memory using a relative address?

- la
- nop
- **ldr** **PG # 47**
- str

114. We represent e^ instead of e to show _____.

- Sign Magnitude Form
- Radix Complement Form
- Diminished Radix Complement Form
- **Biased Representation** **PG # 347**

115. _____ is a combination of arithmetic, logic and shifter unit along with some multiplexers and control unit.

- Computer Bus
- CPU Register
- Flip Flop
- **ALU** **PG # 347**

116. Connection Oriented Communication reserves the _____until the transfer is complete.

- **Bandwidth** **PG # 394**
- Error
- Checksum
- Protocol

117. In Connection-less Communication message is divided into _____.

- Tracks
- Sectors
- Platters
- **Packets** **PG # 394**

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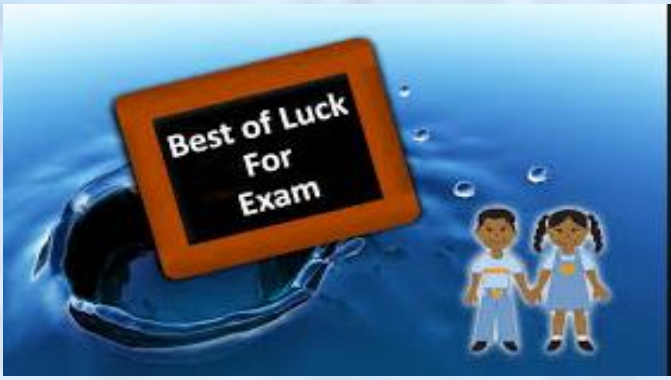

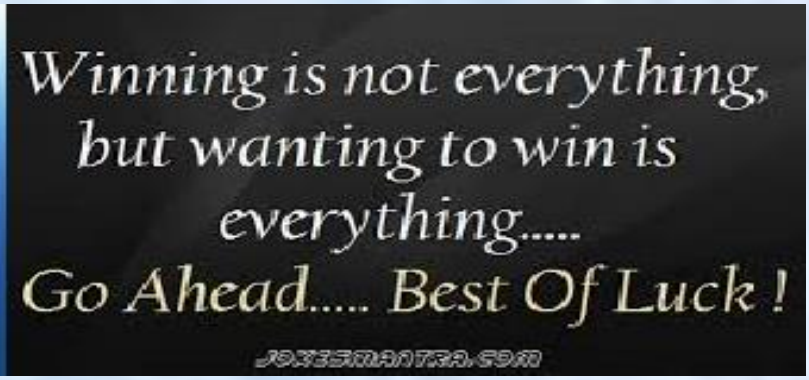

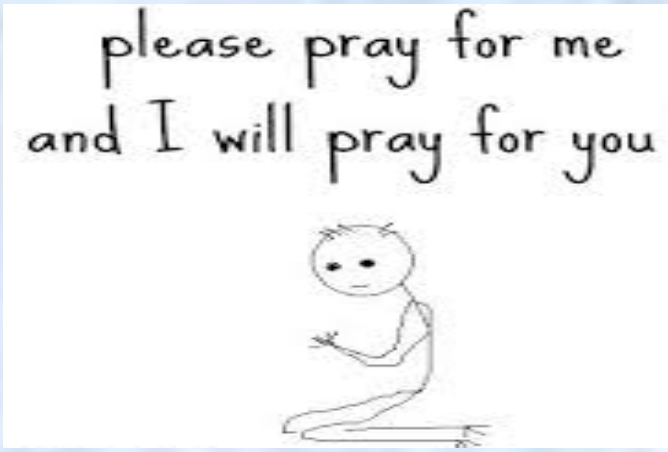

THE END

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