MIDTERM EXAMINATION CS302- Digital Logic Design

Question No: 1	(Marks: 1)	- Please choose one

A SOP expression is equal to 1 _____

- ► All the variables in domain of expression are present
- ► At least one variable in domain of expression is present.
- ▶ When one or more product terms in the expression are equal to 0.
- ▶ When one or more product terms in the expression are equal to 1.

Question No: 2 (Marks: 1) - Please choose one

The output A < B is set to 1 when the input combinations is _____

- ► A=10, B=01
- ► A=11, B=01
- ► A=01, B=01
- ► A=01, B=10

Question No: 3 (Marks: 1) - Please choose one

Two 2-bit comparator circuits can be connected to form single 4-bit comparator

- ► True
- ► False

Question No: 4 (Marks: 1) - Please choose one

High level Noise Margins (V_{NH}) of CMOS 5 volt series circuits is

- ▶ 0.3 V
- ► 0.5 V
- ► 0.9 V
- ► 3.3 V

Question No: 5 (Marks: 1) - Please choose one
If we multiply "723" and "34" by representing them in floating point
notation i.e. by first, converting them in floating point representation and
then multiplying them, the value of mantissa of result will be
▶ 24.582
▶ 2.4582
▶ 24582
▶ 0.24582
Question No: 6 (Marks: 1) - Please choose one
The output of the expression F=A+B+C will be Logic when A=0,
B=1, C=1. the symbol'+' here represents OR Gate.
Undefined
One
► Zero
► 10 (binary)
Question No: 7 (Marks: 1) - Please choose one
If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input
and then the R input goes to 0, the latch will be
and then the R input goes to o, the laten win be
► SET
► RESET
► Clear
► Invalid
Invand
Question No: 8 (Marks: 1) - Please choose one
3.3 v CMOS series is characterized by andas
compared to the 5 v CMOS series.

- ► Low switching speeds, high power dissipation
- ► Fast switching speeds, high power dissipation
- ► Fast switching speeds, very low power dissipation

► Low switching speeds, very low power dissipation

Question No: 9 (Marks: 1) - Please choose one
The binary value "1010110" is equivalent to decimal
▶ 86
► 87
▶ 88
▶ 89
Question No: 10 (Marks: 1) - Please choose one
The Encoder is used as a keypad encoder.
► 2-to-8 encoder
► 4-to-16 encoder
► BCD-to-Decimal
➤ Decimal-to-BCD Priority
Question No: 11 (Marks: 1) - Please choose one
How many data select lines are required for selecting eight inputs?
▶ 1
▶ 2
▶ 2▶ 3
▶ 2
 ▶ 2 ▶ 3 ▶ 4 Question No: 12 (Marks: 1) - Please choose one
 ▶ 2 ▶ 3 ▶ 4
 ▶ 2 ▶ 3 ▶ 4 Question No: 12 (Marks: 1) - Please choose one
 ▶ 2 ▶ 3 ▶ 4 Question No: 12 (Marks: 1) - Please choose one The property of the diagram above shows the general implementation of form
Destion No: 12 (Marks: 1) - Please choose one Ouestion No: 12 (Marks: 1) - Please choose one Ouestion No: 12 (Marks: 1) Oues

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► POS

► SOP Question No: 13 (Marks: 1) - Please choose one		
The Quad Multiplexer has outputs		
 ▶ 4 ▶ 8 ▶ 12 ▶ 16 Question No: 14 (Marks: 1) - Please choose one 		
Demultiplexer has		
 ➤ Single input and single outputs. ➤ Multiple inputs and multiple outputs. ➤ Single input and multiple outputs. ➤ Multiple inputs and single output. Question No: 15 (Marks: 1) - Please choose one		
The expression is an example of Commutative Law for		
Multiplication.		
 ▶ AB+C = A+BC ▶ A(B+C) = B(A+C) ▶ AB=BA ▶ A+B=B+A 		
Question No: 16 (Marks: 1) - Please choose one		
"Sum-of-Weights" method is used		
► to convert from one number system to other		
to encode data		
 to decode data to convert from serial to parralel data 		
P to convert from serial to partator data		
Question No: 17 (Marks: 2)		
Why a 2-bit comparator is called parallel comparator?		
Question No: 18 (Marks: 2)		

Explain at least two advantages of the circuit having low power consumption

Question No: 19 (Marks: 2)

Name the four OLMC configurations

Question No: 20 (Marks: 3)

Explain "Test Vector" in context of ABEL

Question No: 21 (Marks: 3)

For a two bit comparator circuit specify the inputs for which the output A < B is set to 1

Question No: 22 (Marks: 5)

Explain Tri-State Buffers with the help of block diagram

Question No: 23 (Marks: 5)

Explain the Operation of Odd-Parity Generator Circuit with the help of timing diagram