**MIDTERM  EXAMINATION**
**CS302- Digital Logic Design**
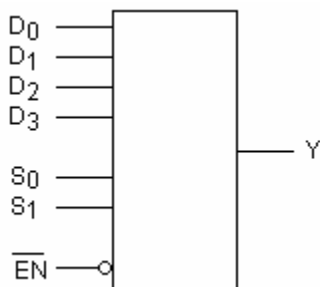
## Question No: 1    ( Marks: 1 )    - Please choose one

GAL can be reprogrammed because instead of fuses _____ logic is used in it

► **$E^2$CMOS**
► TTL
► CMOS+
► None of the given options

## Question No: 2    ( Marks: 1 )    - Please choose one

The device shown here is most likely a



► Comparator
► **Multiplexer**
► Demultiplexer
► Parity generator

## Question No: 3    ( Marks: 1 )    - Please choose one

If "1110" is applied at the input of BCD-to-Decimal decoder which output pin will be activated:

► 2nd
► 4th
► 14th
► **No output wire will be activated**

## Question No: 4    ( Marks: 1 )    - Please choose one

Half-Adder Logic circuit contains 2 XOR Gates
► True
► **False**

## Question No: 5    ( Marks: 1 )    - Please choose one

A particular Full Adder has
► **3 inputs and 2 output**

► 3 inputs and 3 output
► 2 inputs and 3 output
► 2 inputs and 2 output

**Question No: 6    ( Marks: 1 )    - Please choose one**

$Sum = A \oplus B \oplus C$

$CarryOut = C(A \oplus B) + AB$

are the Sum and CarryOut expression of
► Half Adder
► **Full Adder**
► 3-bit parralel adder
► MSI adder cicuit

**Question No: 7    ( Marks: 1 )    - Please choose one**

A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

► **True**
► False

**Question No: 8    ( Marks: 1 )    - Please choose one**

The output A < B is set to 1 when the input combinations is _____

► A=10, B=01
► A=11, B=01
► A=01, B=01
    ► **A=01, B=10**
**Here output combination should A < B**

**Question No: 9    ( Marks: 1 )    - Please choose one**

The 4-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► 8
► 12
    ► **16**

**Question No: 10    ( Marks: 1 )    - Please choose one**

Generally, the Power dissipation of _____ devices remains constant throughout their operation.

    ► **TTL**
► CMOS 3.5 series

► CMOS 5 Series
► Power dissipation of all circuits increases with time.

## Question No: 11    ( Marks: 1 )   - Please choose one

The decimal "8" is represented as _____ using Gray-Code.

► 0011
   ► **1100**
► 1000
► 1010

## Question No: 12    ( Marks: 1 )   - Please choose one

(A+B).(A+C) =  _____

► B+C
   ► **A+BC**
► AB+C
► AC+B

## Question No: 13    ( Marks: 1 )   - Please choose one

A.(B + C) = A.B + A.C is the expression of _____

► Demorgan's Law
► Commutative Law
► **Distributive Law**
► Associative Law

## Question No: 14    ( Marks: 1 )   - Please choose one

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

► **FALSE**
► TRUE

## Question No: 15    ( Marks: 1 )   - Please choose one

In ANSI/IEEE Standard 754 "Mantissa" is represented by ___32-bits_____ bits

► 8-bits
► 16-bits
► **32-bits**
► 64-bits

## Question No: 16    ( Marks: 1 )   - Please choose one

Caveman number system is Base _5_____ number system

► 2
  ► **5**
► 10
► 16

**Question No: 17    ( Marks: 1 )**

Briefly state the basic principle of **Repeated Multiplication-by-2** Method.
**Repeated Multiplication-by-2 method allows decimal fractions of any magnitude to be easily converted into binary.**

**Question No: 18    ( Marks: 1 )**

How standard Boolean expressions can be converted into truth table format.
**Standard Boolean expressions can be converted into truth table format using binary values for each term in the expression. Standard SOP or POS expressions can also be determined from a truth table.**

**Question No: 19    ( Marks: 2 )**



What will be the out put of the diagram given below
A.B + A.B.C.D
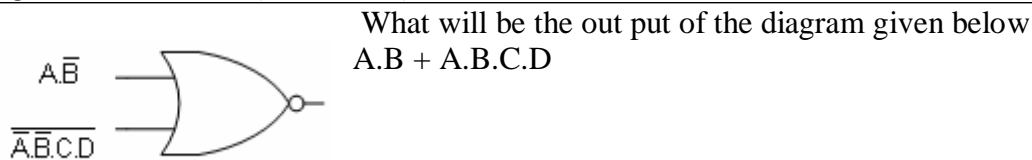
**Question No: 20    ( Marks: 3 )**

When an Input (source) file is created in ABEL a module is created which has three sections. Name These three sections.

**Answer:**

The three sections are:
• Boolean Equations
• Truth Tables
• State Diagrams

**Question No: 21    ( Marks: 5 )**

Explain "AND" Gate and some of its uses

**AND gates are used to combine multiple signals, if all the signals are TRUE then the output will also be TRUE. If any of the signals are FALSE, then the output will be false. ANDs aren't used as much as NAND gates; NAND gates use less components and have the advantage that they be used as an inverter.**

For Registration on www.virtualinspire.com u can use Firefox or chrome or latest Internet Explorer.......

**Question No: 22   ( Marks: 10 )**

 **Write down different situations where we need the sequential circuits.**

Digital circuits that use memory elements for their operation are known as Sequential circuits. Thus Sequential circuits are implemented by combining combinational circuits with memory elements.