Jun. 2

CS501_Current Mid term whole paper Solved with references by MASOOM FAIRY

Total Questions: 26

MCQs: 20

Subjective: 6

Whole Paper is given below:

Question No: 1 (Marks: 1)
FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC _____wide.
8-bits
16-bits
32-bits (Page 157)
64-bits

Question No: 2 (Marks: 1) - Please choose one
Which one of the following is a bi-stable device, capable of storing one bit of information?
Decoder
Flip-Flop (Page 76)
Multiplexer
Diplexer

Question No: 3 (Marks: 1) - Please choose one
Which instruction is used to store register to memory using relative address?
ld instruction
ldr instruction
lar instruction
str instruction (Page 48)

Question No: 4 (Marks: 1) - Please choose one
The instruction _____ will load the register R3 with the contenets of the m\emory location M [PC+56]
Add R3, 56
lar R3, 56
ldr R3, 56 (Page 56)
str R3, 56

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Question No: 5 (Marks: 1)
_____ oeaini eurdt hnetepoesrssaet nw,dfndvle
Change
Reset (Page 194)
Update
None of the given

Question No: 6
which type of instructions help in changing the flow of the program as and when required?
Arithmetic
Control (Page 137)
Data transfer
Floating point

Question No: 7 (Marks: 1) - Please choose one
Which one of the following registers holds the address of the next instruction to be executed? Accumulator
Address Mask
Instruction
Register
Program Counter (Page 151)

Question No: 8 (Marks: 1) - Please choose one
The external interface of FALCON-A consists of a _____address bus and _____a data bus. 8-bit. 8-bit
16-bit. 16-bit Click here for detail
16-bit. 24-bit
16-bit. 32-bit

Question No: 9 (Marks: 1) - Please choose one
What is the instruction length of the SRC processor?
► 8 bits
► 16 bits
► 32 bits (Page 134)
► 64 bits

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Question No: 10 (Marks: 1) - Please choose one
P: R3 ¬ R5
MAR ¬ IR
These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?
► Arrow ¬
► Colon :
► **Comma , (Page 69)**
► Parentheses ()

Question No: 11 (Marks: 1) - Please choose one
The processor must have a way of saving information about its state or context so that it can be restored upon return from the ---------- □
► □ **Exception Click here for detail**□
►□Function □
►□Stack □
►□Thread

Question No: 12 (Marks: 1) - Please choose one
Which one of the following register holds the instruction that is being executed?
► Accumulator
► Address Mask
► **Instruction Register (Page 152)**
► Program Counter

Question No: 13 (Marks: 1) - Please choose one
The code size of 2-address instruction is _____.
► 5 bytes
► **7 bytes (Page 36)**
► 3 bytes
► 2 bytes

Question No: 14 (Marks: 1) - Please choose one
An “assembler” that runs on one processor and translates an assembly language program written for another processor into the machine language of the other processor is called a ----------
►compiler
►**cross assembler (Page 26)**
►debugger
►linker

Question No: 15 (Marks: 1) - Please choose one
What functionality is performed by the instruction “lar R3, 36” of SRC?

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►It will load the register R3 with the contents of the memory location M [PC+36]
►**It will load the register R3 with the relative address itself (PC+36). (Page 48)**
►It will store the register R3 contents to the memory location M [PC+36]
►No operation

Question No: 16 (Marks: 1) - Please choose one
Which operator is used to „name" registers, or part of registers, in the Register Transfer Language?
Select correct option:
►**:= (Page 66)**
►&
►%
►©

Question No: 17 (Marks: 1) - Please choose one
In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?
►Arithmetic/logic
►**Load/store (Page 141)**
►Test/branch
►None of the given

Question No: 18 (Marks: 1) - Please choose one
What does the instruction "ldr R3, 58" of SRC do?
►**It will load the register R3 with the contents of the memory location M [PC+58] (Page 47)**
►It will load the register R3 with the relative address itself (PC+58).
►It will store the register R3 contents to the memory location M [PC+58]
►No operation

Question No: 19 (Marks: 1) - Please choose one

Type A of SRC instruction format include.

Select correct option:

3 ALU registers

4 ALU registers

1 ALU registers

2 ALU registers (Page 47)

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Note: I forgot last MCQ.

Q: 21: Which technique is used for overlapping multiple instructions simultaneously? [Marks 2]

Answer: [PAGE 202, Topic Executing machine instructions with and without pipelining]

Pipe lining is the technique in which multiple instructions execute simultaneously.

Q: 22: Differentiate between uni-bus implementation FALCON-A and SRC with respect to bus width? [Marks 2]

Answer: [PAGE 157]

FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is 32-bits wide.

Q: 23: Arrange the following steps of SRC in correct order. [Marks 3]

- **ALU operation**
- **Instruction fetch**
- **Memory access**
- **Register write**
- **Instruction decode/operand fetch**

Answer: [PAGE 206]

1. Instruction Fetch
2. Instruction decode/operand fetch
3. ALU operation
4. Memory access
5. Register write

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Q: 24: Differentiate between Memory Address Register and Memory Buffer Register. [Marks 3]

Answer: [PAGE 151]

MAR
The Memory Address Register takes input from the ALSU as the address of the memory location to be accessed and transfers the memory contents on that location onto the memory sub-system.
MBR
The Memory Buffer Register has a bi-directional connection with both the memory sub-system and the registers and ALSU. It holds the data during its transmission to and from memory.

Q: 25: Write the structural RTL for Shiftr ra, rb, c1. [Marks 5]

Answer: [PAGE 163]

Step	RTL
T0-T2	Instruction fetch
T3	n<4..0> ← IR<4..0>;
T4	C ← (Nα0) © R[rb]<15..N>;
T5	R[ra] ← C;

Q: 26: Data dependence is one the complication related to pipe lining. You need to Indentify and method use to resolving data dependence. [Marks 5]

Answer: [PAGE 203 and 204]

Resolving the Data dependency
There are two methods to remedy this situation:
1. Pipeline stalls
These are inserted into the pipeline to block instructions from entering the pipeline until some instructions in the later part of the pipeline have completed execution. Hence our modified code would become

```
…
S1: add r3, r2, r1
stall[6]
stall
stall
S2: sub r4, r5, r3
…
```

2. Data forwarding

When using data forwarding, special hardware is added to the processor, which allows the results of a particular pipeline stage to be transferred directly to another stage in the pipeline where they are required. Data may be forwarded directly from the execute stage of one instruction to the decode stage of the next instruction. Considering the above example, S1 will be in the execute stage when S2 will be decoded. Using a comparator we can determine that the destination operand of S1 and source operand of S2 are the same. So, the result of S1 may be directly forwarded to the decode stage.