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library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.numeric_std.all;

entity tb_CLA_top is
end entity tb_CLA_top;

architecture mixed of tb_CLA_top is
      component CLA_top is
            port(
                  a, b  : in std_logic_vector(31 downto 0);
                  cin   : in std_logic;
                  --
                  sum   : out std_logic_vector(31 downto 0);
                  cout  : out std_logic
            );
      end component;

      signal tb_a, tb_b : std_logic_vector(31 downto 0) := (others => '0');
      signal tb_cin           : std_logic := '0';
      signal tb_sum           : std_logic_vector(31 downto 0) := (others => '0');
      signal tb_cout          : std_logic := '0';

begin
      DUT : CLA_top
      port map(
            a => tb_a,
            b => tb_b,
            cin => tb_cin,
            --
            sum => tb_sum,
            cout => tb_cout
      );

      process begin
            -- Test 1: enkel addisjopn uten carry
            tb_a <= std_logic_vector(to_unsigned(15, 32));
            tb_b <= std_logic_vector(to_unsigned(16, 32));
            tb_cin <= '0';
            wait for 20 ns;
            assert ( tb_sum = std_logic_vector(to_unsigned(31, 32)) and tb_cout =
'0')
                  report ("FAILED: 15+16 = 31") severity failure;

            -- Test 2: små tall ingen carry
            tb_a <= std_logic_vector(to_unsigned(7, 32));
            tb_b <= std_logic_vector(to_unsigned(5, 32));
            tb_cin <= '0';
            wait for 20 ns;
            assert ( tb_sum = std_logic_vector(to_unsigned(12, 32)) and tb_cout =
'0')
                  report ("FAILED: 7+5 = 12") severity failure;

            -- Test 3: output med carry
            tb_a <= std_logic_vector(to_unsigned(15, 32));
            tb_b <= std_logic_vector(to_unsigned(1, 32));
            tb_cin <= '0';
            wait for 20 ns;
            assert ( tb_sum = std_logic_vector(to_unsigned(16, 32)) and tb_cout =
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'0')
                report ("FAILED: 15+1 = 16") severity failure;

            -- Test 4: carryin
            tb_a <= std_logic_vector(to_unsigned(8, 32));
            tb_b <= std_logic_vector(to_unsigned(8, 32));
            tb_cin <= '1';
            wait for 20 ns;
            assert ( tb_sum = std_logic_vector(to_unsigned(17, 32)) and tb_cout =
'0')
                report ("FAILED: 8+8+1 = 17") severity failure;

            -- Test 5:store tall uten carry out
            tb_a <= std_logic_vector(to_unsigned(4096, 32));
            tb_b <= std_logic_vector(to_unsigned(4096, 32));
            tb_cin <= '0';
            wait for 20 ns;
            assert ( tb_sum = std_logic_vector(to_unsigned(8192, 32)) and tb_cout =
'0')
                report ("FAILED: 4096+4096 = 8192") severity failure;

            -- Test 6: Tabsolutt maksimum
            tb_a <= x"FFFFFFFF";
            tb_b <= x"00000001";
            tb_cin <= '0';
            wait for 20 ns;
            assert ( tb_sum = x"00000000" and tb_cout = '1')
                report ("FAILED: FFFFFFFF+1 = 0 with carry out") severity
failure;

            -- Test 7: Carry-in propagerer
            tb_a <= std_logic_vector(to_unsigned(255, 32));
            tb_b <= std_logic_vector(to_unsigned(1, 32));
            tb_cin <= '1';
            wait for 20 ns;
            assert ( tb_sum = std_logic_vector(to_unsigned(257, 32)) and tb_cout =
'0')
                report ("FAILED: 255+1+carry_in = 257") severity failure;

            -- Test 8: komplex stor tall
            tb_a <= std_logic_vector(to_unsigned(100000, 32));
            tb_b <= std_logic_vector(to_unsigned(250000, 32));
            tb_cin <= '0';
            wait for 20 ns;
            assert ( tb_sum = std_logic_vector(to_unsigned(350000, 32)) and tb_cout
= '0')
                report ("FAILED: 100000+250000 = 350000") severity failure;

            -- Test 9: alternerende bits
            tb_a <= x"AAAAAAAA";
            tb_b <= x"55555555";
            tb_cin <= '0';
            wait for 20 ns;
            assert ( tb_sum = x"FFFFFFFF" and tb_cout = '0')
                report ("FAILED: AAAAAAAA + 55555555 = FFFFFFFF") severity
failure;

            -- Test 10: høy carry out
            tb_a <= x"12345678";
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            tb_b <= x"87654321";
            tb_cin <= '0';
            wait for 20 ns;
            assert ( tb_sum = x"99999999" and tb_cout = '0')
                  report ("FAILED: 12345678 + 87654321 = 99999999") severity
failure;

            report("Ferdig!") severity note;
            std.env.stop;
      end process;

end architecture mixed;
```