```
library IEEE;
  use IEEE.STD_LOGIC_1164.all;

entity fulladder is
  port (
    a  : in std_logic;
    b  : in std_logic;
    cin : in std_logic;
    s   : out std_logic;
    cout : out std_logic
    );
end fulladder;


architecture rtl of fulladder is
begin
    s  <= a xor b xor cin;
    cout <= ((a xor b) and cin) or (a and b);

end rtl;
```