AXI One Wire Controller

AXI One Wire Controller consists of three hdl module “one\_wire\_controller” as vhdl wrapper, “axi\_bus\_decoder” as axi slave decoder, “one\_wire” for the implementation of one protocol.

# Features

* Presence-Reset: Initialization handshake of one wire protocol can be sent as seperate packet.
* One wire Write: A byte or a bit can be sent in one wire timing
* One wire Read : One wire read requests can be sent for a reading a full byte or a bit.

# Slave Registers

### Base Address + 0x00:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit 31 - 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Reserved | Byte/Bit Mode | Reset | Rd\_Wr | Enable |

* Enable: With **Rising Edge** on this bit one wire packet will be started.
* Rd\_Wr: ‘0’ indicates Read Packet, ‘1’ indicates Write packet.
* Reset: When this bit is set to ‘1’ next rising edge of enable will initiate a **Reset-Presence** sequence.
* Byte/Bit Mode : When this bit is set to ‘0’ read/write operations will performed in bytes otherwise read/write operations will be performed in bits

### Base Address + 0x04:

|  |  |
| --- | --- |
| Bit 31 – 8 | Bit 7 – 0 |
| Reserved | Transmit\_Data |

* Transmit\_Data: When Rd\_Wr is set to ‘1’ and Enable is set to ‘1’ Transmit\_Data will be output from DQ\_io in **LSB** fashion.

### Base Address + 0x08:

|  |  |
| --- | --- |
| Bit 31 – 8 | Bit 7 – 0 |
| Reserved | Receive\_Data |

* Receive\_Data: When Rd\_Wr is set to ‘1’ and Enable is set to ‘1’ IP will generate Bit request(s) from the bus and replie(s) will be put into Receive\_Data in **LSB** fashion.

### Base Address + 0x0C:

|  |  |  |  |
| --- | --- | --- | --- |
| Bit 31 – 3 | Bit 2 | Bit 1 | Bit 0 |
| Reserved | Error | Busy | Receive\_Ready |

* Receive\_Ready: After Receive Packet Ends this bit will be set to one and when AXI read operation is performed in this register this bit will be cleared.
* Busy: When either Reset-Presence, Read, Write packet is processed this bit will be one.
* Error: When Reset Pulse is performed but no Presence is Received in the process this bit will be one.