3. HAFTA

BLM320

BİLGİSAYAR MİMARİSİ

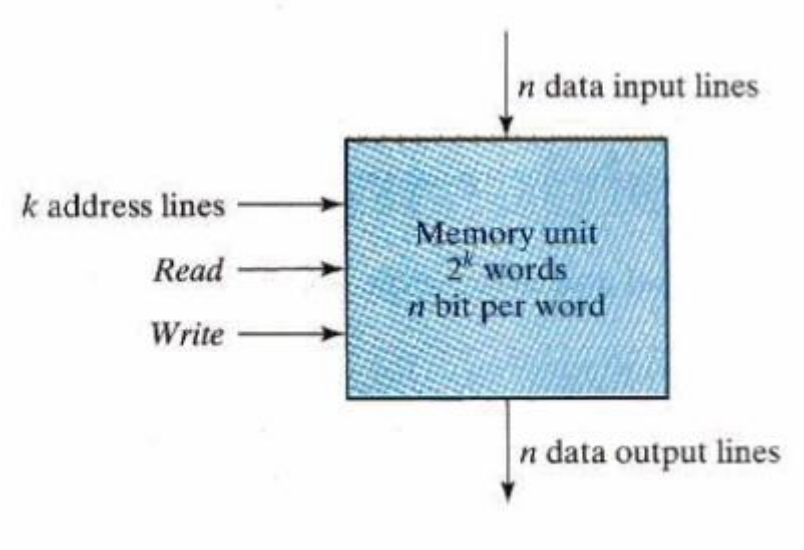
Yrd. Doç. Dr. Salih GÖRGÜNOĞLU

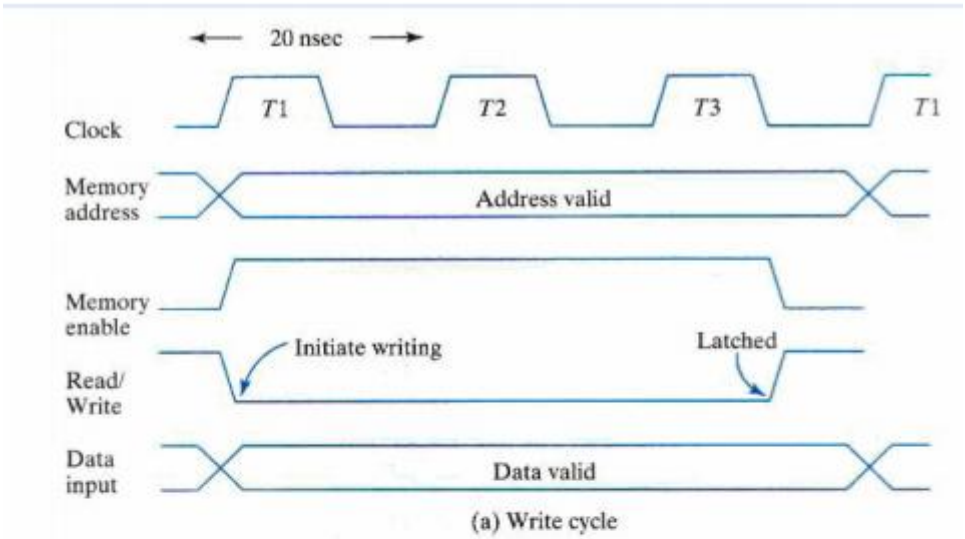
sgorgunoglu@karabuk.edu.tr

KBUZEM
Karabük Üniversitesi
Uzaktan Eğitim Uygulama ve AraştırmaMerkezi

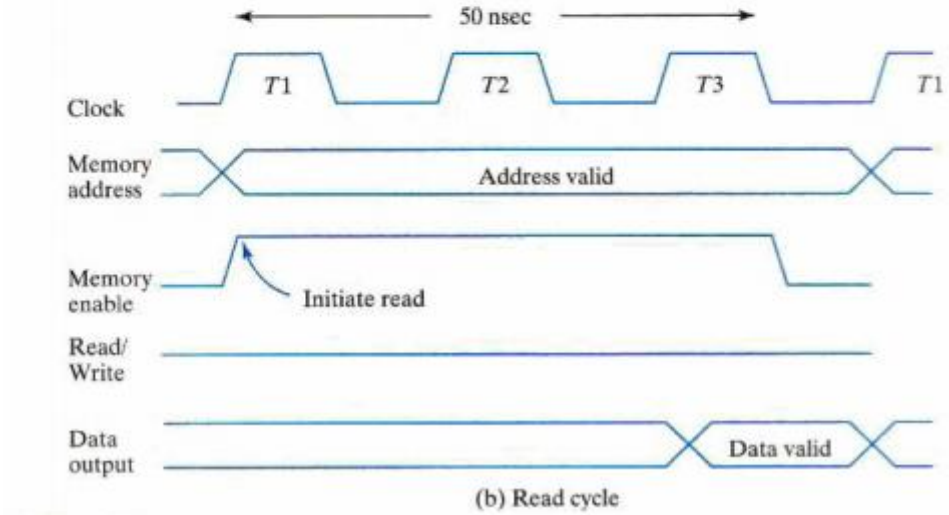
3. Hafıza yapısı

S-R Flip-Flop



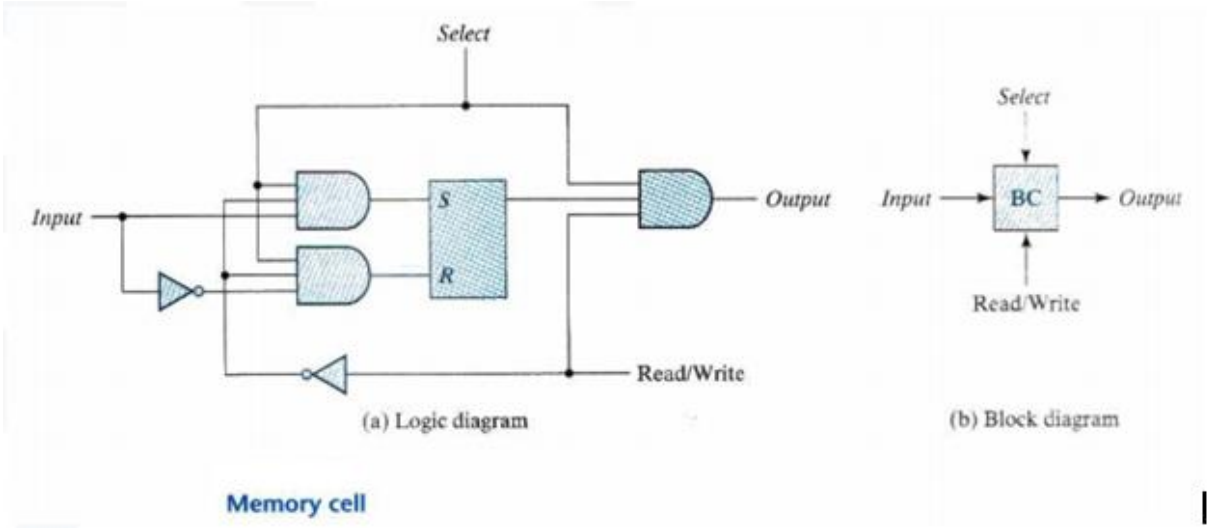


(a) Write cycle



(b) Read cycle

Memory cycle timing waveforms



(a) Logic diagram

(b) Block diagram

Memory cell

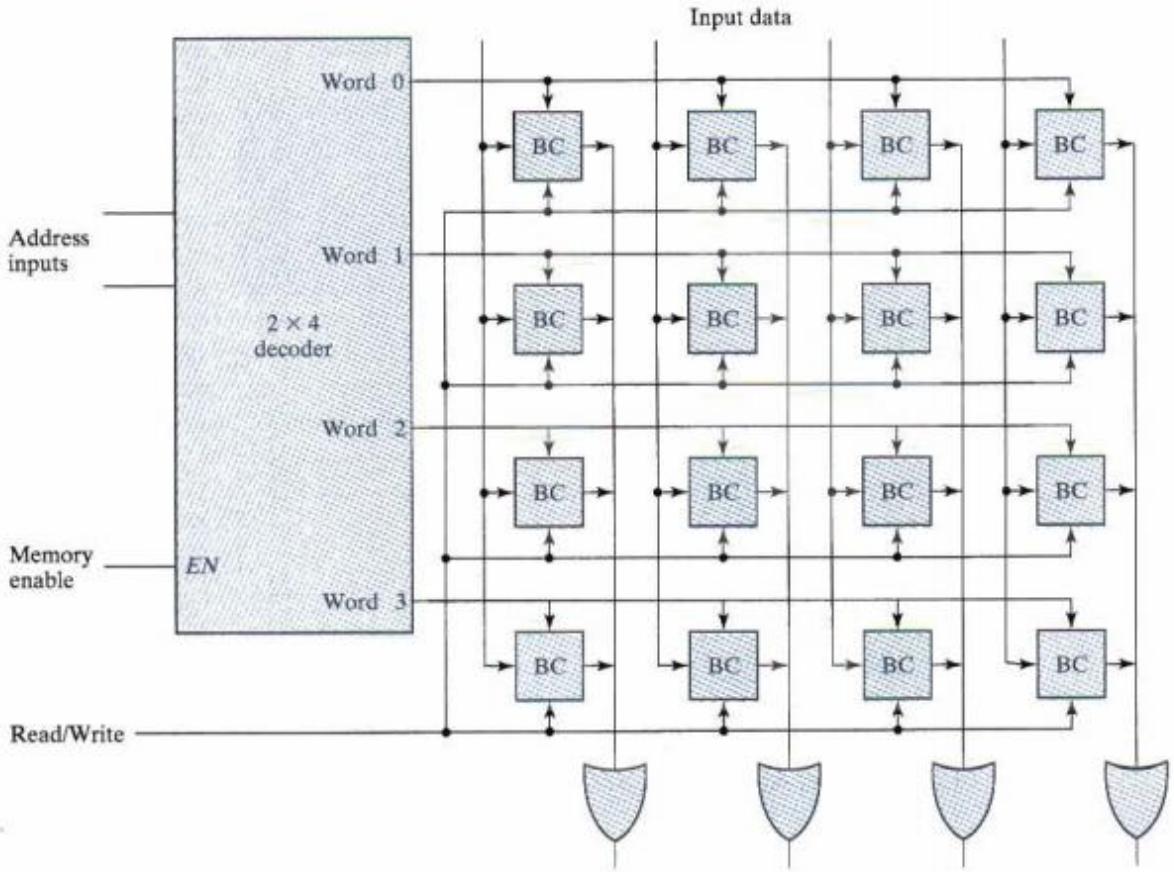
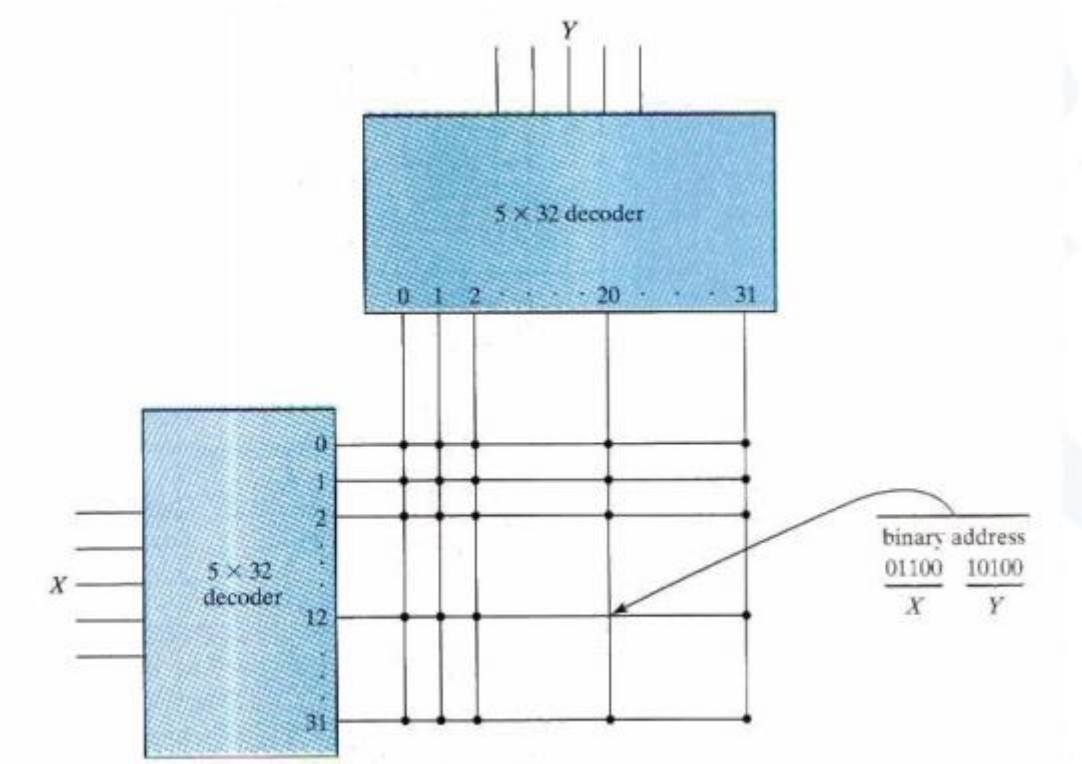
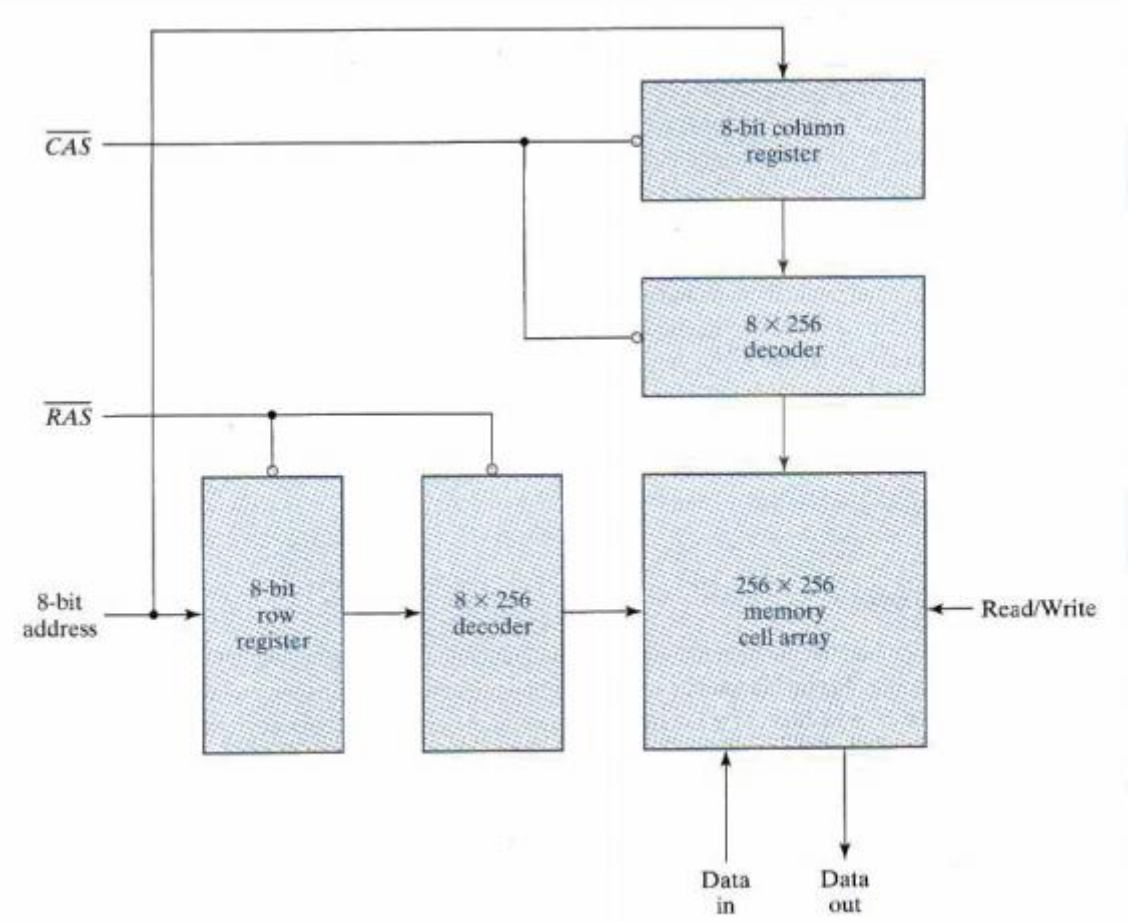


Diagram of a 4 × 4 RAM

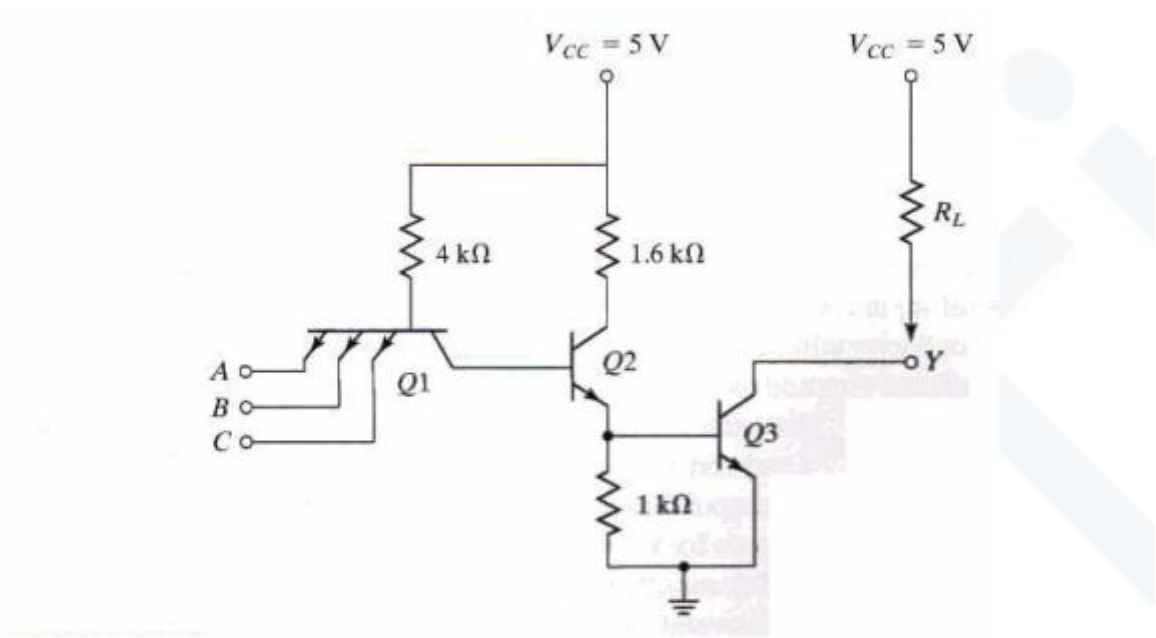


Two-dimensional decoding structure for a 1K-word memory

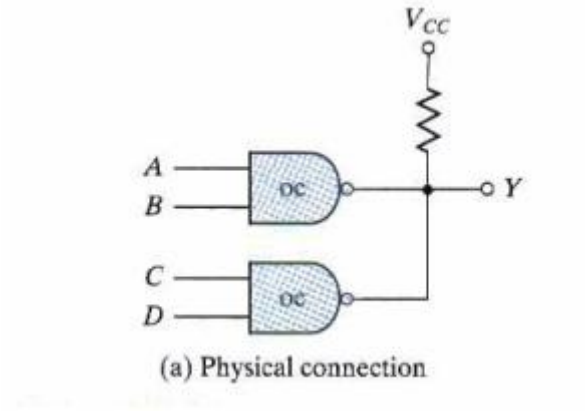


Address multiplexing for a 64K DRAM

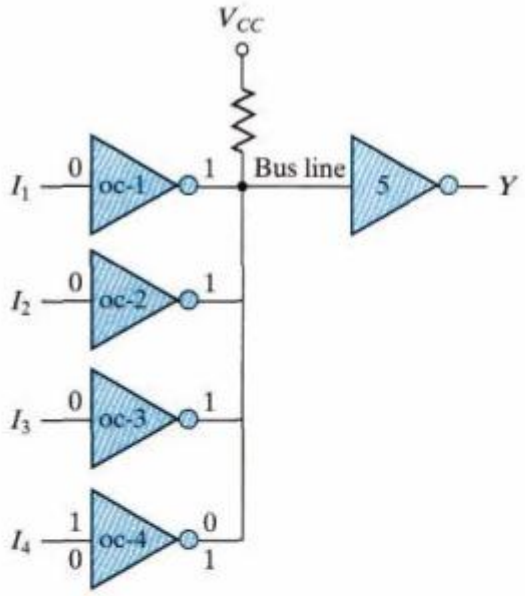
1. Open-collector output
2. Totem-pole output
3. Three-state output



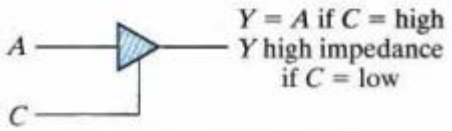
Open-collector TTL NAND gate



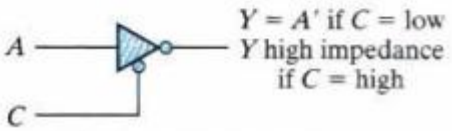
Wired AND of two open collector (oc) gates, Y=(AB+CD)'



Open-collector gates forming a common bus line



(a) Three-state buffer gate



(b) Three-state inverter gate