2. HAFTA

BLM320

BİLGİSAYAR MİMARİSİ

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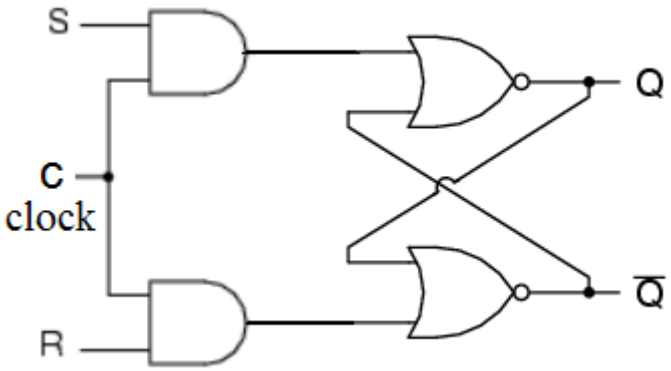
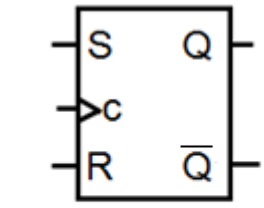
2. Kaydedici yapısı

S-R Flip-Flop

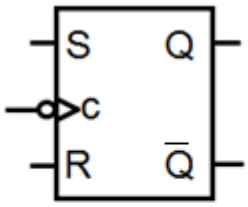
İki kararlı çok katlı flip flop isminde de belli olduğu gibi iki kararlı duruma sahiptir. Genelde bir durum set diğeri de reset olarak adlandırılır. Böylece en basit iki kararlı cihaz set-reset veya S-R flipflop olarak bilinir. Bir S-R flipflop oluşturmak için iki NOR geçidini birinin çıkışı diğerinin girişini besleyecek şekilde (ve tersi) bağlanır. Flip floplar Kaydedicilerin ve sayıcı tasarımının temelini oluşturur. Flip flop 1 birtlik veri saklar.



S	R	Q(t+1)	
0	0	Q(t)	Değişim yok
0	1	0	clear
1	0	1	set
1	1	?	Belirsiz

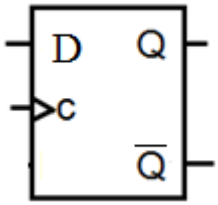


Clock yükselen Kenarda çalışır



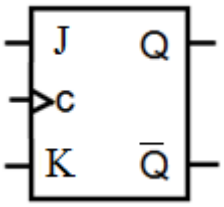
Clock düşen Kenarda çalışır

D Flip-Flop



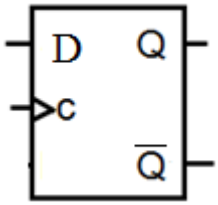
D	Q(t+1)	
0	0	clear
1	1	set

J-K Flip-Flop



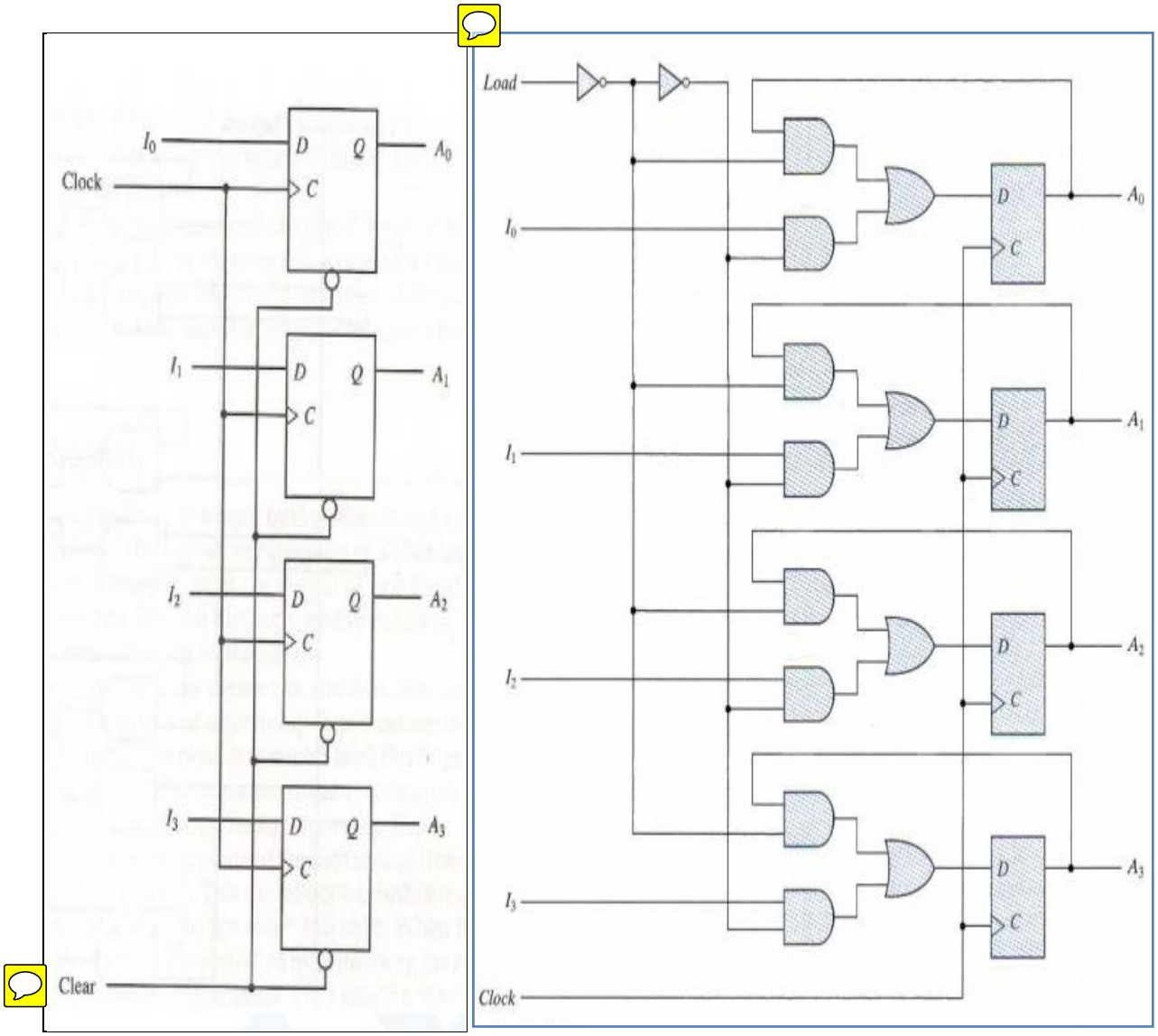
J	K	Q(t+1)	
0	0	Q(t)	Değişim yok
0	1	0	clear
1	0	1	set
1	1	Q'(t)	Complement

T Flip-Flop

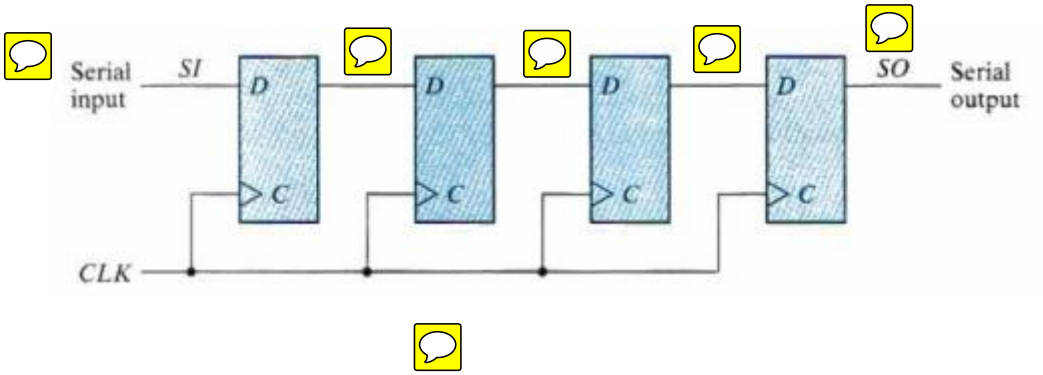


T	Q(t+1)	
0	Q(t)	Değişim yok
1	Q'(t)	Complement

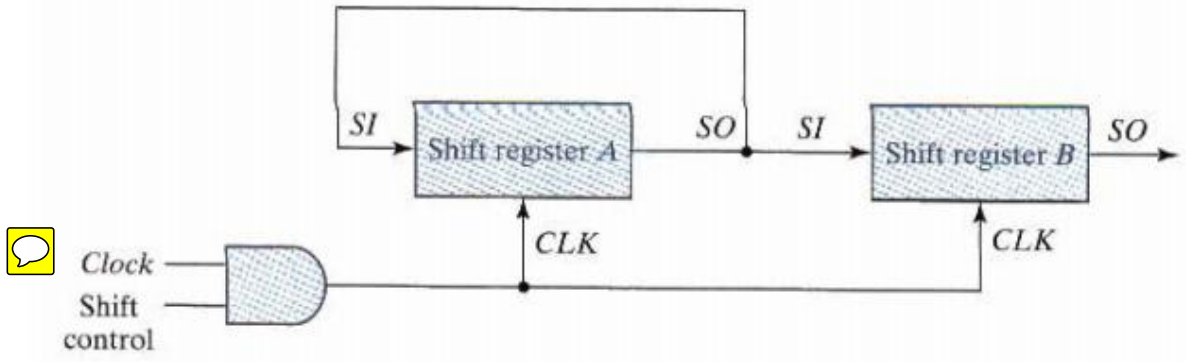
Dört bit register



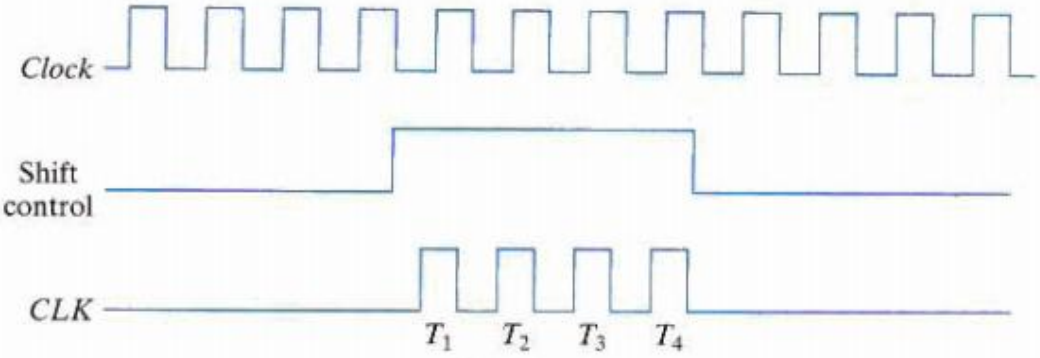
4 bit shift register



Seri veri transferi



(a) Block diagram

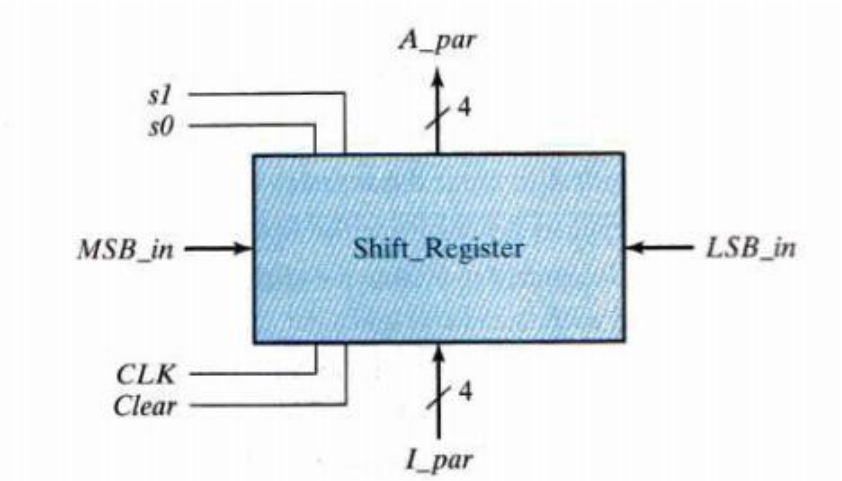


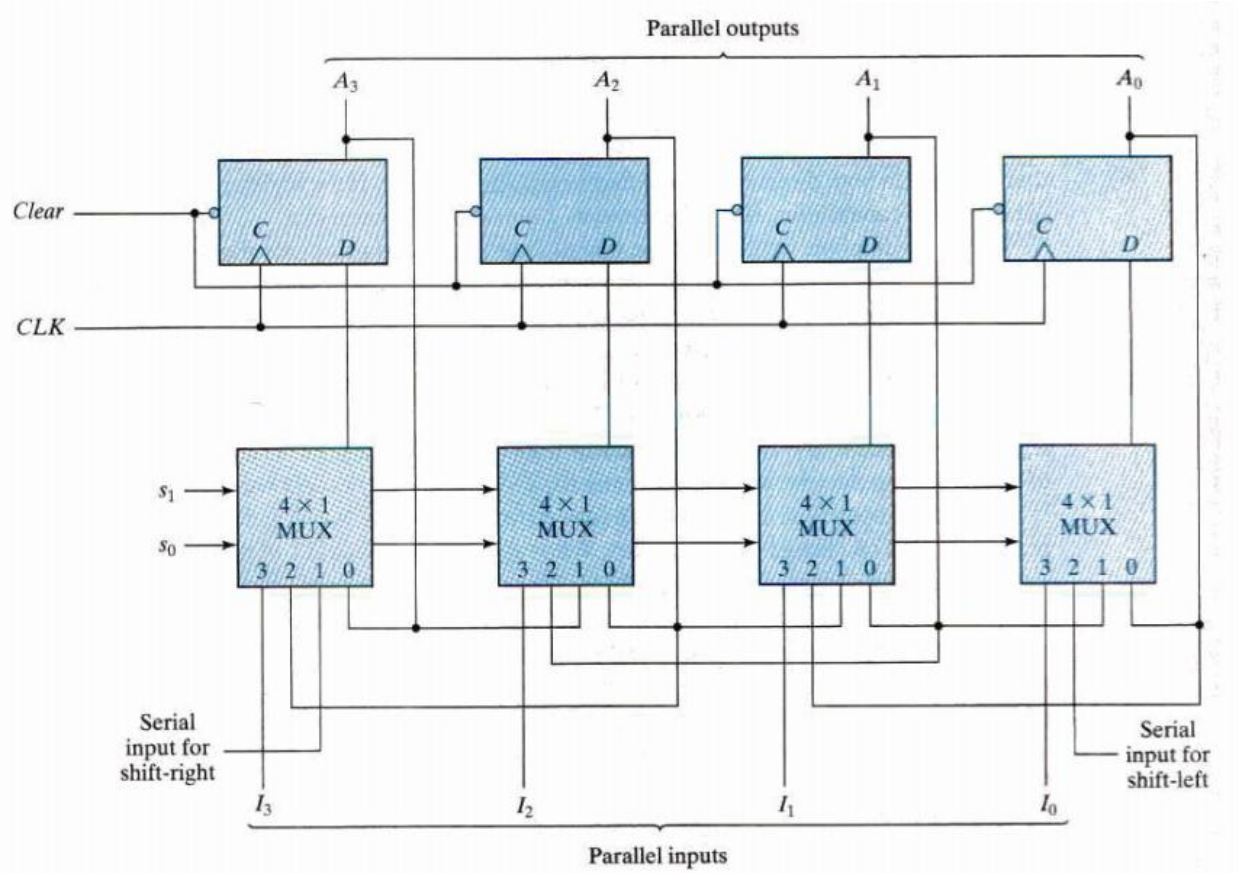
(b) Timing diagram

Serial-Transfer Example

Timing Pulse	Shift Register A				Shift Register B			
Initial value	1	0	1	1	0	0	1	0
After T_1	1	1	0	1	1	0	0	1
After T_2	1	1	1	0	1	1	0	0
After T_3	0	1	1	1	0	1	1	0
After T_4	1	0	1	1	1	0	1	1

Universal shift register

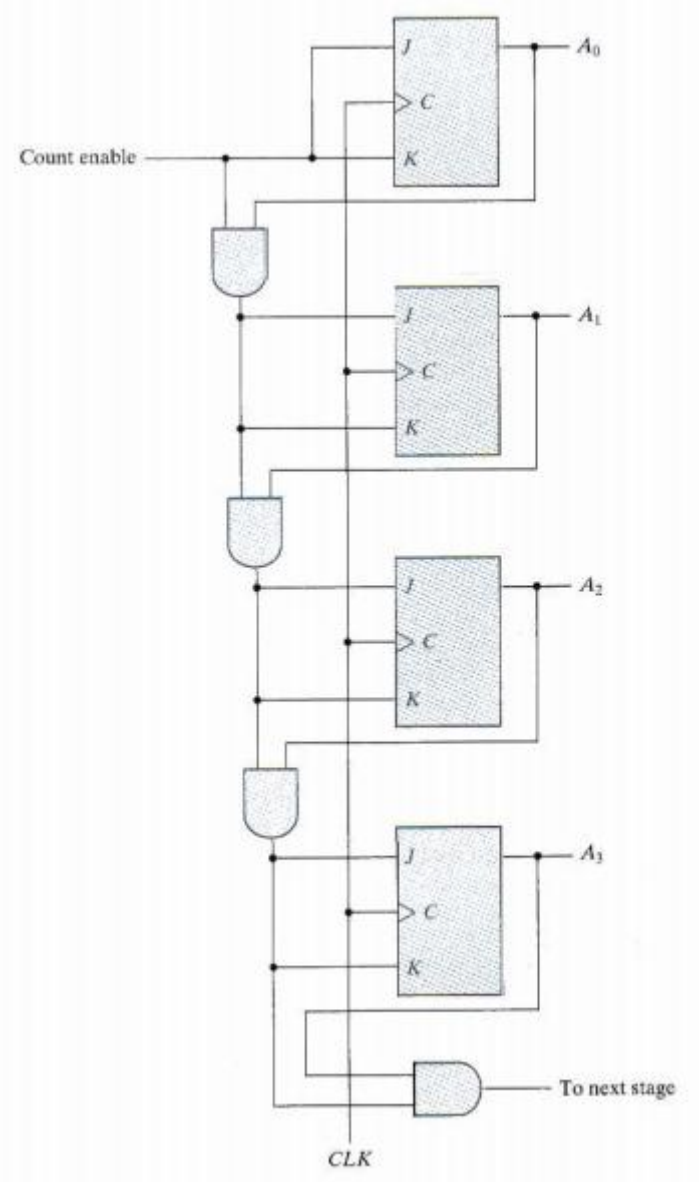




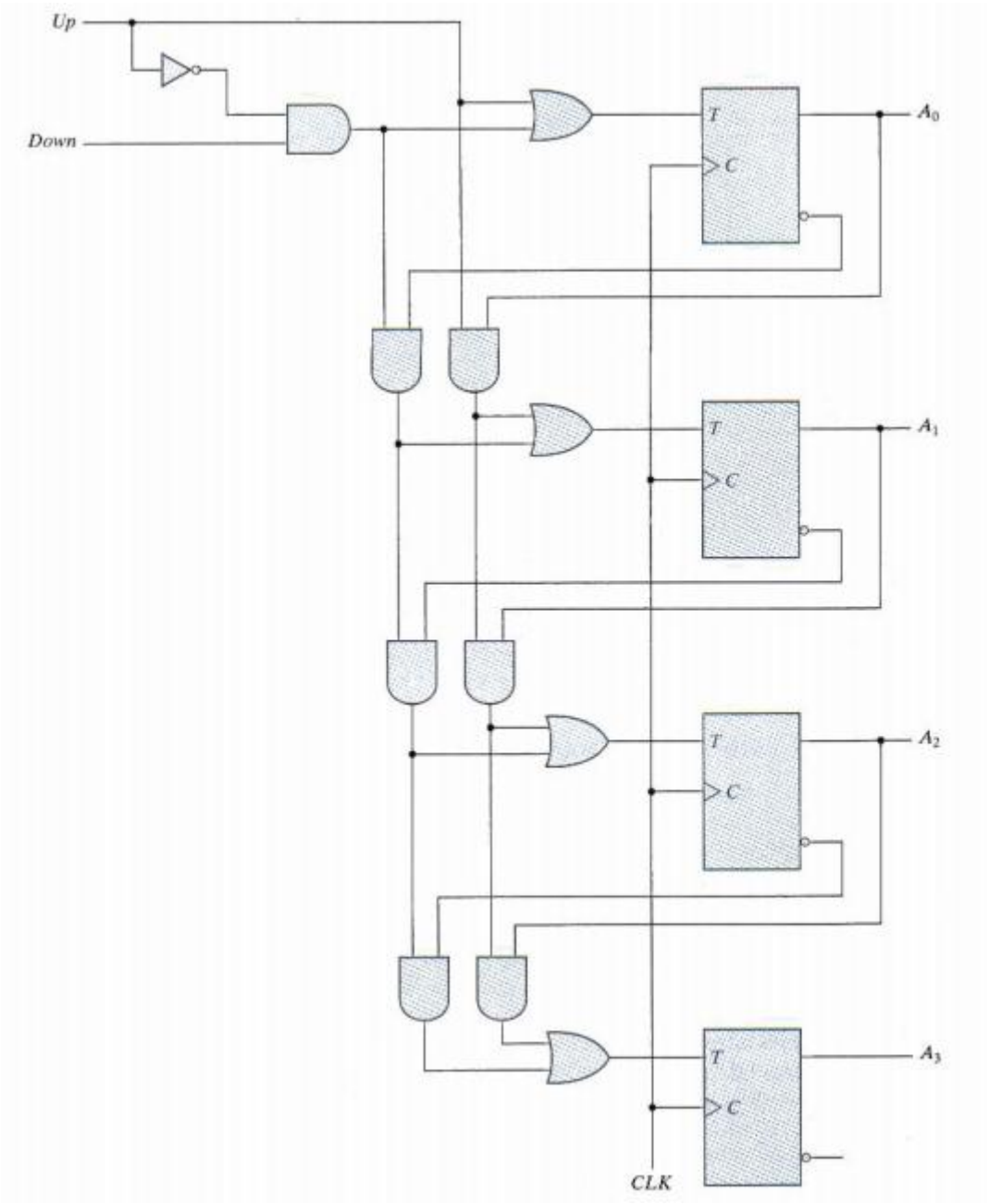
Mode Control

s_1	s_0	Register Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

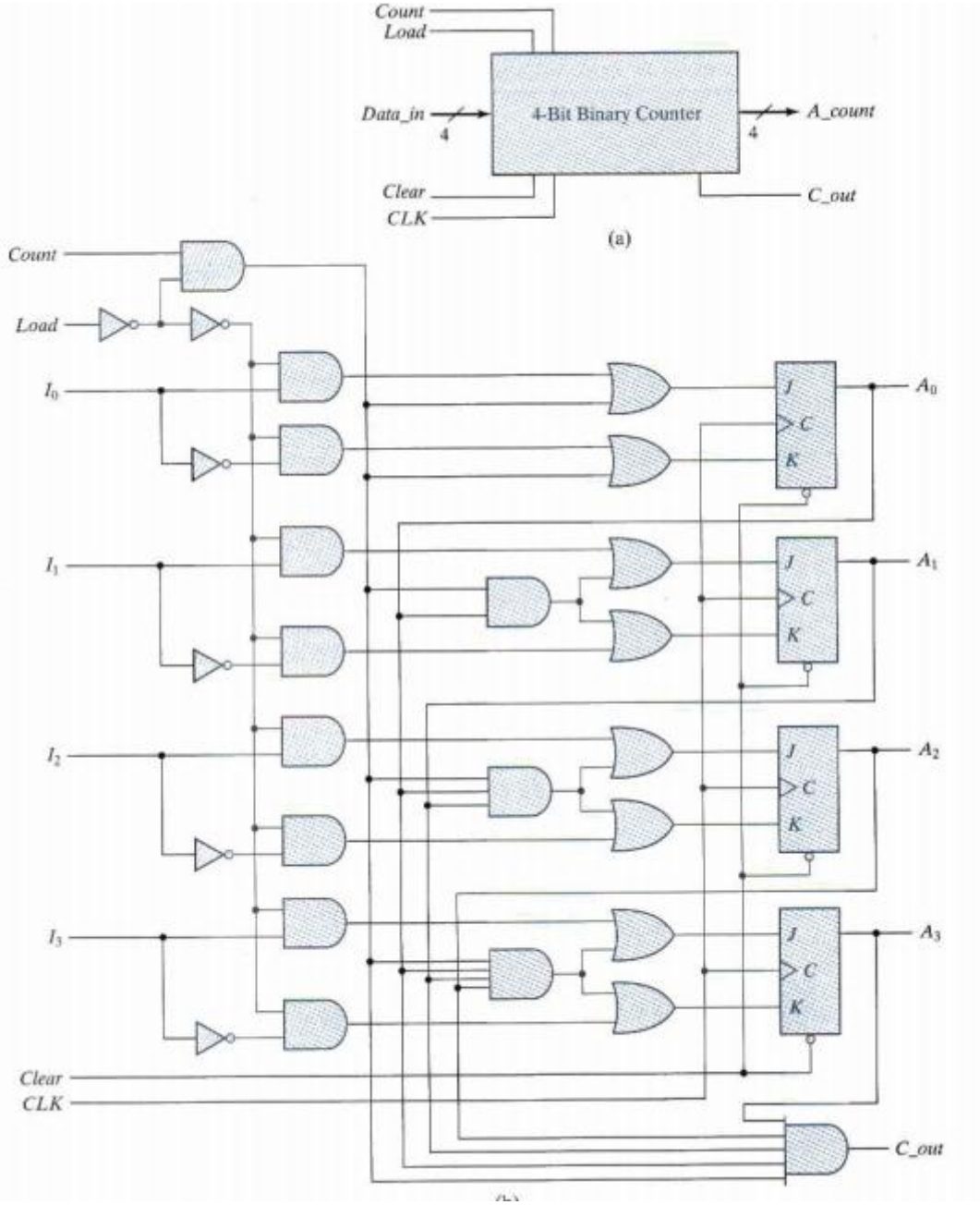
4-bit binary counter senkronize



4 bir up down binary counter



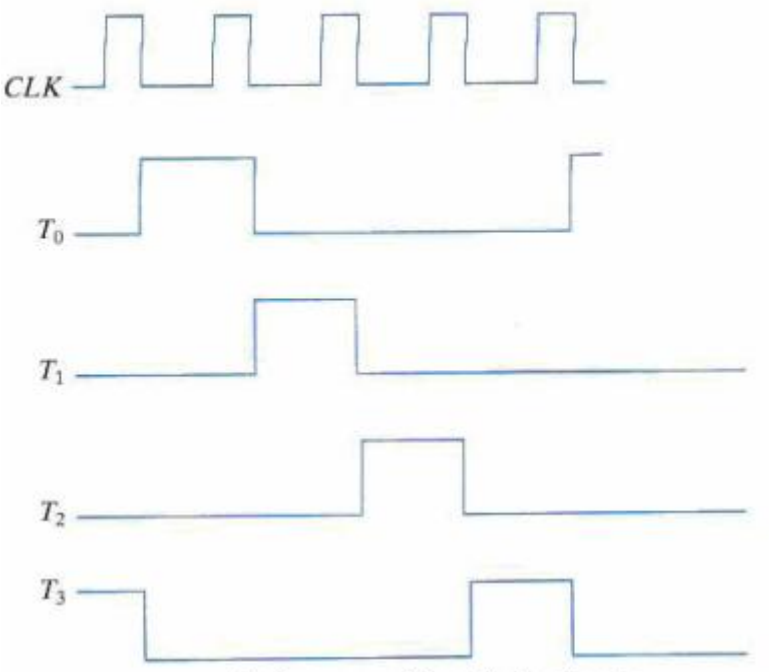
4-bit binary counter with parallel load



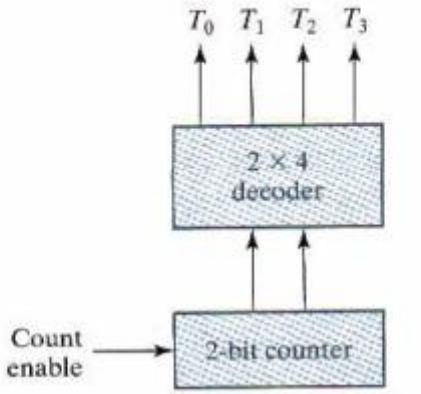
Function Table for the Counter

Clear	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change

Zamanlama Sinyallerinin üretilmesi



(b) Sequence of four timing signals



(c) Counter and decoder