Menglin Song

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EDUCATION

The Hong Kong University of Science and Technology, Hong Kong, China (Ongoing) Sep 2023-Jun 2024

Master of Science in IC Design Engineering

Southwest Jiaotong University, China (Top 50 in China) Sep 2018-Jun 2022

Bachelor of Engineering in Electronic Science and Technology

RESEARCH EXPERIENCE

High-precision mathematical Modelling and Prediction of Passive Intermodulation (PIM) via Automated Data-Driving Testing December 2021 – May 2022

Role: First Principal Instructor: Qiuyan Jin (SWJTU, Lecturer)

Step One：Preliminary Groundwork for Modelling

- ***Basic theoretical analysis of PIM***
  - Analysing RF connectors and their PIM characteristics, aiming to propose multiple methods to adapt to different passive connectors and accurately predict their PIM phenomenon.
  - Selecting SMA, BNC, and N-type connectors as the experimental subjects, determining the frequency range. Based on the equipment specifications, determining the power range of the input signals. Performing multiple experiments and taking the average to guard against the influence of jitter.
- ***Data processing and standards Formulation***
  - Evaluation of experimental outcomes. With the input voltage increasing, the slopes of i_{IM3}-V_{in} curves increased gradually, which was in accordance with the Zenner breakdown principle.
  - Establishing fitting and estimation criteria. The two-thirds of the 540,000 datasets are allocated as training set while the remaining one-third is designated as validation set for evaluating the estimation results.

Step Two: Establishment of Novel Models Based on Experimental Data

- ***Modelling and analysis of conventional polynomial models***
  - Using a seven to thirteen degree odd-order polynomial function for curve fitting and applying the Levenberg-Marquardt optimization algorithm for iterative optimization.
  - Upon conducting detailed analysis of the fitting and estimation results, observed patterns in the coefficients and the low accuracy of the polynomial model when dealing with a small amount of data and a limited number of parameters.
- ***Establishment of a model repository and automated testing***
  - Based on the physical characteristics of passive intermodulation and experimental results, a total of 184 models were pre-screened using an automated script. These models were expanded into Taylor series and identified the models that share similar characteristics in terms of coefficient patterns as the polynomial model.
  - Fitting these models with the same iterative approach. The entire testing process was fully automated by the script in Python and involved over 1,200,000 iterations.

Step Three: Analysis of Experimental Results and Optimization Test

- To compare the fitting accuracy, prediction accuracy, function graph, and design algorithm of all models, considering the number of coefficients and accuracy, a fully automated evaluation script was used, which could fit, predict, and evaluate each model, and calculate corresponding metrics.
- Resulting in the identification of two highly accurate models for predicting the PIM phenomenon---hyperbolic sine function and Gaussian algorithm, with a recognition accuracy of 95%+.
- In order to further optimize the hyperbolic sine function model, we introduced regression testing to evaluate different variations of the model by adjusting the number and characteristics of its parameters. We evaluated each variant on both training and validation datasets to determine the best-performing model, and then made comprehensive adjustments and optimizations accordingly.

Investigation on a Robust Algorithm of Placement & Routing for Multi-Die FPGAs via Deep Learning Toolkit May 2023 - Present

Role: First Principal *Instructor: Wei Zhang (HKUST, Professor), Zhixiong Di (SWJTU, Associate Professor)*

Step One: Establishing Architecture and Designing Standards

- ***Architecture analysing and hypothesis***
  - Summarized the characteristics and difference between regular structure and multiple Super Logic Region (SLR) on FPGA, which is data flow design and resource evaluation.
  - Based on Alveo U250 architecture, constructing the hypothetical architecture, featuring a 1×4 SLR topology with I/O banks and DDR controller IPs situated in the central column, and partitioned into 2×3 clock regions.
- ***Common models trial and establishment of standards***
  - Utilized the algorithm of latest Versatile Place and Routing (VPR) and Xilinx Pipelining algorithm as the reference standard and assessed the feasibility of the architecture.
  - Collected the time consuming, latency and memory usage as the criterion for judging.

Step Two: Algorithm Designing and Formal Model Training

- ***Designing the model based on PyTorch***
  - Conducted in-depth analysis of the placement and routing architecture for multi-chip FPGAs, with a primary design approach centered around Time-Driven methodology for placement, designing the function of pin arrangement and TDM allocation for data transmission.
  - Developed solutions using the PyTorch framework via machine learning, using a mix of C++ and Python in programming allows for combining the efficiency of C++ with the flexibility of Python. Provided more flexibility to route signals between different dice and achieved lower minimum channel width and critical path delay.
- ***Training by the hypothetical architecture***
  - Performing experiments to evaluate the performance of the designed algorithm and validating the effectiveness and feasibility of the routing architecture in simulated scenarios.
  - Revising the architectural design to incorporate a multi-die FPGA utilizing a 2x2 SLR (Super Logic Regions) topology, followed by conducting comprehensive model testing and evaluation.

Step Three: Real Architecture Verification and Data Analysis (In Progress)

- Verifying with more complexed commercial structure and performing a comprehensive evaluation and comparative analysis of the outcomes derived from the conducted experiments.
- Refining relevant research and preparing to publish it in relevant publications and conferences, showcasing the superiority of the designed routing architecture in multi-chip FPGA systems.

Communications & Sensor Networks for Modern Transportation International Cooperation Research Centre of China - Intelligent Router Project 02/2022 - 06/2022

Role: Principal *Instructor: Gang Liu (Assistant Dean, Associate Professor)*

- Developed the RF that was controlled by wireless transmission chip and formed local area network enabling the router to complete signal sending and receiving or be controlled by the terminal in the absence of wireless network.
- Designed a router that can be controlled by LAN, with MT7621 as the main control chip for the collection and exchange of Ethernet data and MT7615 as the wireless transmission chip.
- Created the PCB layout, and implemented the customized layout (RAM, I/O and other modules) by using Advanced Design, resulting in a 50% increase in integration.

ACADEMIC ACHIEVEMENTS

- Best Graduation Thesis (The only 1 in the major, 2% in the University)
- Entrance Scholarship in HKUST (Less than 10% in the major)
- The third prize in the Integrated Circuit EDA Elite Challenge at the national level
- Bachelor's GPA: 80.71%, Top 30%
- **Publications:**

  M. Song, W, Zhang, T, Liang. (Proceeding). GreenWave: A Robust and Time-Driven Placer for Large-Scale Multi-Die Heterogeneous FPGAs, 2024 IEEE/ACM International Conference on Computer Aided Design (ICCAD)

R. Liu, **M. Song**, Q. Jin. (Proceeding). A Novel Passive Intermodulation Model of Coaxial Cable Assemblies with Distributed and Point-source Nonlinearities, IEEE Transactions on Circuits and Systems II (SCI Journal)

M. Song, Q. Jin. (2022). High-precision Mathematical Modelling of Passive Intermodulation in Connectors, *Electronics Letters* (SCI Journal), doi: 10.1049/ell2.12539

M. Song. On the Importance of Electronic Information Engineering Practice to Students' Development, *New Education Era, 2017 (19)*

- **Patent:**
  Title: A fitting method for a passive intermodulation (PIM) mathematical model | Patent Number: 023108822605

PROFESSIONAL EXPERIENCE

TEXAS INSTRUMENTS **Chengdu, China/ Dallas, USA/KL, Malaysia**

Chip Product Engineer 07/2022 – 06/2023

- Participate in the research and development of next-generation automated technologies for semiconductors, especially the optical chip of 3D scan & machine vision products.
- Work with the global design and testing team to evaluate and deploy new validation solutions that improve (Digital Light Processing) DLP chip quality, productivity and cost.
- Collaborate with developing and production sites, support variety of new developments (AGV, Automation, Center PMI, AI/Big data, etc.)
- Be Invited to participate in the sensor product development and research in the Global research center in Dallas. USA and Tucson. USA more than 3 months.
- Participated in the in-depth research and development of the new test plan design in the Asian headquarters in Malaysia and accept training for more than 40 days.

SunMedia Chengxin Technology (Chengdu) Co., Ltd. **Chengdu, China**

Intern, Chip Design Engineer 07/2021 - 08/2021

- Participated in the research and development of SOC chips, including RTL coding and SDC development.
- Engaged in synthesis and lint/CDC inspection and formal verification.
- Participated in chip architecture design, including clock/reset/low power system design, system module division and specification definition, and system integration design.
- Learned the basic knowledge of FPGA and AXI Bus and designed AXI Slave Bus by Vivado.
- Called IP core in Vivado software, learned the knowledge about VGA timing sequence in the image processing, and implemented ROM-VGA image processing based on FPGA with Verilog HDL.

EXTRACURRICULAR ACTIVITIES

Vice President of the University Intel Campus Core Elite 05/2019 - 09/ 2020

- Organized various activities to strengthen the communication between core elites from different faculties or universities.
- Used various media to publicize the core elite organization and expand its influence.
- Developed good organization and planning ability.

Chairman of the University International Affairs Centre 09/2019 - 06/2021

- Organized various international communication activities to create an international learning and exchange atmosphere and helped students their horizons.
- Planned and organized English learning activities to improve students' cross-cultural communication skills.

SKILLS & INTERESTS

Technique Skills: C++, Python, Matlab, Verilog HDL

Interests: Football, Ping-pong, Erhu (Chinese instrument, once preformed in Golden Hall in Vienna), Deutsch