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Homework #2-2

Problem 1

4.1 Consider the following instruction:
Instruction: `and rd, rs1, rs2`
Interpretation: `Reg[rd] = Reg[rs1] AND Reg[rs2]`

4.1.1 What are the values of control signals generated by the control in Figure 4.10 for this instruction?

- RegWrite = True
- ALUOp = 0000
- ALU Operation = "and"
- MemWrite = False
- MemRead = False
- MemtoReg = 0

Problem 2

4.4 When silicon chips are fabricated, defects in materials (e.g., silicon) and manufacturing errors can result in defective circuits. A very common defect is for one signal wire to get "broken" and always register a logical 0. This is often called a "stuck-at-0" fault.

4.4.1 Which instructions fail to operate correctly if the `MemToReg` wire is stuck at 0?

Loads
: the value can never be read from memory.
Only ALU result can only be stored in register.
It can't work 'LW' because instruction fetch value from memory into registers.

4.4.2 Which instructions fail to operate correctly if the `ALUSrc` wire is stuck at 0?

I-type, Loads, Stores Instruction.
: ALU is limited by the second operand to only have value from register file as it can't fetch immediate value from instruction.
All I instruction will not work.

Problem 3

4.5 In this exercise, we examine in detail how an instruction is executed in a single-cycle datapath. Problems in this exercise refer to a clock cycle in which the processor fetches the following instruction word: 0x00c6ba23.

4.5.1 What are the values of the ALU control unit's inputs for this instruction?

100011 : the lower 6 bits of instruction will be input for ALU control process

4.5.2 What is the new PC address after this instruction is executed? Highlight the path through which this value is determined.

PC+4

4.5.3 For each mux, show the values of its inputs and outputs during the execution of this instruction. List values that are register outputs at Reg [xn].

- ALUSrc : Input : Reg[x12], 64'h14
  Outputs : 64'h14
- MemtoReg : Inputs : Reg[x13]+0x14 and <undefined>
  Outputs : <undefined>
- Branch : Inputs : PC+4, 64'h28
  Outputs : N/A

4.5.4 What are the input values for the ALU and the two add units?

- ALU Inputs : Reg[x13], 0x14
- PC Adder Inputs : PC and 4
- Branch Adder Inputs : PC and 0x28