Homework #3-2

Problem 1

5.10 In this exercise, we will look at the different ways capacity affects overall performance. In general, cache access time is proportional to capacity. Assume that main memory accesses take 70 ns and that 36% of all instructions access data memory. The following table shows data for L1 caches attached to each of two processors, P1 and P2.

	L1 Size	L1 Miss Rate	L1 Hit Time	L1 Hit Rate
P1	2 KiB	8.0%	0.66 ns	100-8.0=92
P2	4 KiB	6.0%	0.90 ns	100-6.0=94

5.10.1 Assuming that the L1 hit time determines the cycle times for P1 and P2, what are their respective clock rates?

$$\text{Clock Rate of P1} = \frac{1}{\text{L1 hit time}} = \frac{1}{0.66} = 1.5151 \text{ GHz}$$

$$\text{Clock Rate of P2} = \frac{1}{\text{L1 hit time}} = \frac{1}{0.90} = 1.11 \text{ GHz}$$

5.10.2 What is the Average Memory Access Time for P1 and P2 (in cycles)?

AMAT = Hit time + Miss rate × Miss penalty.

* in cycle *

$$\text{P1}: \frac{70\text{ns}}{0.66\text{ns}} = 106.06, \quad 1\text{cycle} + (0.08\% \times \overset{\approx 107}{106.06}\,\text{cyle}) = 9.56 \text{ cycles}$$

$$\text{P2}: \frac{70\text{ns}}{0.90\text{ns}} = 77.78, \quad 1\text{cycle} + (0.06\% \times \overset{\approx 78}{77.78}\,\text{cycle}) = 5.68 \text{ cycles}$$

Problem 2

5.12 Multilevel caching is an important technique to overcome the limited amount of space that a first-level cache can provide while still maintaining its speed. Consider a processor with the following parameters:

Base CPI, No Memory Stalls	Processor Speed	Main Memory Access Time	First-Level Cache Miss Rate per Instruction	Second-Level Cache, Direct-Mapped Speed	Miss Rate with Second-Level Cache, Direct-Mapped	Second-Level Cache, Eight-Way Set Associative Speed	Miss Rate with Second-Level Cache, Eight-Way Set Associative
1.5	2 GHz	100 ns	7%	12 cycles	3.5%	28 cycles	1.5%

First Level Cache miss rate is per instruction. Assume the total number of L1 cache misses (instruction and data combined) is equal to 7% of the number of instructions.

5.12.1 Calculate the CPI for the processor in the table using: 1) only a first-level cache, 2) a second-level direct-mapped cache, and 3) a second-level eight-way set associative cache. How do these numbers change if main memory access time doubles? (Give each change as both an absolute CPI and a percent change.) Notice the extent to which an L2 cache can hide the effects of a slow memory.

$* \text{ Miss penalty} = \frac{100\text{ns}}{(1/2\text{ GHz})} = 200 \text{ cycles}$

(1) L1-cache $= 1.5 + (0.07 \times 200) = 15.5$

(2) L2 direct-mapped cache $= 1.5 + (0.07 \times (\overset{12}{\cancel{28}} + (200 \times 0.035)))$

$= 2.83$

(3) L2 eight-way set associative cache $= 1.5 + (0.07 \times (28 + (200 \times 0.015)))$

$= 3.67$

5.12.2 It is possible to have an even greater cache hierarchy than two levels? Given the processor above with a second-level, direct-mapped cache, a designer wants to add a third-level cache that takes 50 cycles to access and will have a 13% miss rate. Would this provide better performance? In general, what are the advantages and disadvantages of adding a third-level cache?

$PI = 1.5 + 0.07 + (12 + 0.035 \times (50 + 0.13 \times 200$ cycle))

$= 2.47$ CPI

Problem 3

5.17 There are several parameters that affect the overall size of the page table. Listed below are key page table parameters.

Virtual Address Size	Page Size	Page Table Entry Size
32 bits	8 KiB	4 bytes
2^{32}	2^{13}	2^{2}

5.17.1 Given the parameters shown above, calculate the maximum possible page table size for a system running five processes.

page size = $2^3 \cdot 2^{10} = 2^{13}$ bytes, offset = 13

virtual address = page number + offset

32 = page number + 13, page number = 19

) $\frac{2^{32}}{2^{13}}$ = 19 bits = 2^{19}

$(2^{19} \times 2^2) \times 5$ (process) $= 5 \times 2 \times \underbrace{2^{20}}_{1MB} = 10MB$

5.17.2 Given the parameters shown above, calculate the total page table size for a system running five applications that each utilize half of the virtual memory available, given a two-level page table approach with up to 256 entries at the 1st level. Assume each entry of the main page table is 6 bytes. Calculate the minimum and maximum amount of memory required for this page table.

$\frac{2^{19}}{2^{8}} = 2^{11} = 2048$ entries.

2048 entries × 4 bytes each = 8KB each (1st)

16MB = 2^{24} address virtual memory

2^{31} virtual memory

$5 \times \left(\frac{2^{31}}{2^{24}}\right) \times 8KB = 5MB$ (2nd)

2048 entries,
4KB each,
covering 8MB of
the virtual address space

$5 \times 256 \times 8$ KB = 10MB

7680

Problem 4

5.21 One of the biggest impediments to widespread use of virtual machines is the performance overhead incurred by running a virtual machine. Listed below are various performance parameters and application behavior.

Base CPI	Privileged O/S accesses per 10,000 instructions	Overhead to trap to the guest O/S	Overhead to trap to VMM	I/O access per 10,000 instructions	I/O access time (includes time to trap to guest O/S)
1.5	120	15 cycles	175 cycles	30	1100 cycles

5.21.1 Calculate the CPI for the system listed above assuming that there are no accesses to I/O.

$$\text{CPI} = \text{Base CPI} + \left(\left(\frac{\text{Privileged O/S acces}}{10000}\right) \times (\text{trap to O/S} + \text{trap to VMM})\right)$$

$$= 1.5 + \left(\left(\frac{120}{10000}\right) \times (15+175)\right) = 3.78$$

5.21.2 I/O accesses often have a large effect on overall system performance.

(a) Calculate the CPI of a machine using the performance characteristics above, assuming a non-virtualized system.

$$\text{CPI (nonvirtulized)} = \text{Base CPI} + \left(\left(\frac{\text{Privileged O/S acces}}{10000}\right) \times \text{trap to O/S}\right)$$

$$+ \left(\left(\frac{\text{I/O acess}}{10000}\right) \times \text{I/O access time}\right)$$

$$= 1.5 + \left(\left(\frac{120}{10000}\right) \times 15\right) + \left(\left(\frac{30}{10000}\right) \times 1100\right)$$

$$= 4.98$$

(b) Calculate the CPI again, this time using a virtualized system.

$$\text{CPI (virtualized)} = \text{Base CPI} + \left(\left(\frac{\text{privileged O/S acess}}{10000}\right) \times (\text{trap to O/S} + \text{trap to VMM})\right)$$

$$+ \left(\left(\frac{\text{I/O acess}}{10000}\right) \times (\text{I/O acess time} + \text{trap to VMM})\right)$$

$$= 1.5 + \left(\left(\frac{120}{10000}\right) \times (15+175)\right) + \left(\left(\frac{30}{10000}\right) \times (1100+175)\right)$$

$$= 7.605$$