CS151B/EE116C – Solutions to Homework #3

Given a gate with an output signal O and k input signals I0, I1, I2, …, Ik:
DELAY(O) = MAX(DELAY(I0), DELAY(I1),…,DELAY(Ik)) + DELAY(k-input gate).

The sum of a 1-bit full adder is implemented as a 3-input XOR gate:
Sn= (An xor Bn xor Cn)

1. G0 = A0 * B0 = 2T (the delay of a 2-input AND gate) + max (0T, 0T) = 2T
2. P0 = A0 xor B0 = 2T + max(0T, 0T) = 2T
→ All Gi and Pi are 2T

3. Gα = G0*P1*P2*P3 + G1*P2*P3 + G2*P3 + G3
= 5T (the delay of 4input-OR gate) + max(5T+2T, 3T+2T, 2T+2T, 2T) = 5T + 7T = 12T
4. Pα = P0*P1*P2*P3 = 5T + max(2T, 2T, 2T, 2T) = 7T
→ All Gi and Pi of the 4-bit CLAs in the 16-bit HCLA are 12T and 7T respectively.

5. C12 = Gγ + Gβ*Pγ + Gα*Pβ*Pγ+ C0*Pα*Pβ*Pγ
= 5T (4 input-OR gate) + max (12T, 2T+max(12T, 7T), 3T+max(12T, 7T, 7T), 5T+max(0T, 7T, 7T, 7T))
= 5T + 15T = 20T

6. C15 = G14 + G13*P14 + G12*P13*P14 + C12*P12*P13*P14 since C12 is the Cin(C0) of this CLA.
= 5T (4 input-OR) + max(2T, 2T+2T, 3T+2T, 5T+20T) = 5T + 25T = 30T

7. C16 = Gδ + Gγ*Pδ + Gβ*Pδ*Pγ + Gα*Pδ*Pβ*Pγ + C0*Pδ*Pβ*Pγ*Pα
= 7T + max (12T, 2T+max(12T, 7T), 3T+max(12T, 7T, 7T), 5T+max(12T, 7T, 7T, 7T), 7T + max(0T, 7T, 7T, 7T, 7T))
= 7T + max(12T, 14T, 15T, 17T, 14T) = 7T + 17T = 24T

8. S15 = (A15 xor B15 xor C15) = 3T + max(0T, 0T, 30T) = 33T

9. C20 = G19 + G18*P19 + G17*P18*P19 + G16*P17*P18*P19 + C16*P16*P17*P18*P19, C16's delay is 0T in the CSA
= 7T + max(2T, 2T+2T, 3T+2T, 5T+2T, 7T+2T) = 7T+9T = 16T

10. To calculate the delay of S19, the delay of C19 is required.
C19 = G18 + G17*P18 + G16*P17*P18 + C16*P16*P17*P18, C16's delay is 0T in the CSA
= 5T + max(2T, 2T+2T, 3T+2T, 5T+2T) = 5T+7T = 12T

S19 = (A19 xor B19 xor C19) = 3T + max(0T, 0T, 12T) = 15T

11. C24 = G23 + G22*P23 + G21*P22*P23 + G20*P21*P22*P23 + C20*P20*P21*P22*P23
= 7T + max(2T, 2T+2T, 3T+2T, 5T+2T, 7T+16T) = 7T+23T = 30T

12. To calculate the delay of C31, the delay of C28 is required.
C28 = G27 + G26*P27 + G25*P26*P27 + G24*P25*P26*P27 + C24*P24*P25*P26*P27
= 7T + max(2T, 2T+2T, 3T+2T, 5T+2T, 7T+30T) = 7T+37T = 44T

C31 = G30 + G29*P30 + G28*P29*P30 + C28*P28*P29*P30
= 5T+max(2T, 2T+2T, 3T+2T, 5T+44T) = 5T+49T = 54T

13. C32(after MUX) = 4T (the delay of MUX) + max (C32(before MUX) inputs, selection bit(C16))

C32(before MUX) = G31 + G30*P31 + G29*P30*P31 + G28*P29*P30*P31 +
C28*P28*P29*P30*P31
= 7T + max(2T, 2T+2T, 3T+2T, 5T+2T, 7T+44T) = 7T+51T = 58T

C16 is 24T from the solution 7.

C32(after MUX) = 4T + max(58T, 58T, 24T) = 62T

14. S31(after MUX) = 4T (the delay of MUX) + max(S31(before MUX) inputs, C16)

S31(before MUX) = (A31 xor B31 xor C31) = 3T + max(0T, 0T, 54T) = 57T

S31(after MUX) = 4T+max(57T, 57T, 24T)= 61T

Maximal Delay is maximum latency of the various output signals:

- S0-S15 from the 16-bit HCLA, with the maximum latency provided by S15 at 33T
- S16-S31 from the output MUX of the 16-bit CSA, with the maximum latency provided by S31 at 61T
- C31 from the output MUX of the 16-bit CSA at 62T

Maximal Delay: 62T