**SEQUENCE DEETECTOR**

Sequence detectors are crucial elements in digital systems, tasked with identifying specific patterns within a data stream. Using finite state machines (FSMs), these detectors can accurately recognize and indicate the presence of the target sequences. This project involves designing and implementing a sequence detector that identifies the sequence "01111110" in the preceding clock cycles. The detector will have a single input 'w' and an output 'z', transitioning through states based on the input and producing the output accordingly.

**Project Components**

To design and implement a sequence detector for the sequence "01111110," the following components are typically needed:

Flip-Flops: These are fundamental elements in FSMs, used to store the current state of the sequence detector. Depending on the detector's complexity, multiple flip-flops may be required to represent different states.

Combinational Logic Gates: Gates such as AND, OR, and XOR are used to implement the transition and output logic of the sequence detector. They combine and manipulate input signals to determine the next state and generate the desired output based on the current state.

Clock Source: A clock source provides the necessary timing for the sequence detector, generating clock pulses that synchronize state transitions and output updates. Typically, the positive edge of the clock signal triggers changes in the circuit.

Input Register: This stores and synchronizes the input signal 'w' with the clock pulses, ensuring that the input is stable during the positive edge of the clock to prevent timing issues.

Output Register: This stores and synchronizes the output signal 'z' with the clock pulses, ensuring the output is stable and can be reliably used in subsequent circuitry.

State Transition Table: A reference table that defines the next state based on the current state and input signal. It determines state transitions and updates the flip-flops accordingly.

Output Table: Specifies the desired output value based on the current state, determining if the detected sequence is present and generating the appropriate output signal.

Wiring and Interconnections: Refers to the physical connections between different components of the sequence detector, enabling signal flow and facilitating the desired circuit functionality.

**Working**

The sequence detector operates sequentially, involving state transitions, sequence detection, and output generation. It starts in an initial state, usually S0, upon system initialization. On each positive edge of the clock signal, the detector's current state is evaluated based on the input signal 'w' and the current state. This combination determines the next state of the detector.

As state transitions occur, the sequence detector continuously checks if the received input sequence matches the desired sequence "01111110." It tracks the input bits from previous clock cycles to determine if the complete sequence has been detected. This comparison enables the detector to identify the desired sequence in the immediately preceding clock cycles.

When the detector successfully identifies the complete sequence "01111110," the output signal 'z' is set to '1,' indicating sequence detection. If the sequence is not detected, the output signal 'z' remains '0.' The output generation is synchronized with the clock signal, ensuring accurate detection based on the input and current state.

By following this sequential process, the sequence detector continuously monitors the input signal and updates its state accordingly. It compares the received sequence with the desired one and generates the corresponding output signal upon detecting the specified sequence within the input data stream.

**Assumptions**

The design and implementation of the sequence detector are based on the following assumptions:

Synchronous Operation: The detector assumes all state transitions and output updates occur precisely at the positive edge of the clock signal, with properly synchronized input 'w' and clock signals.

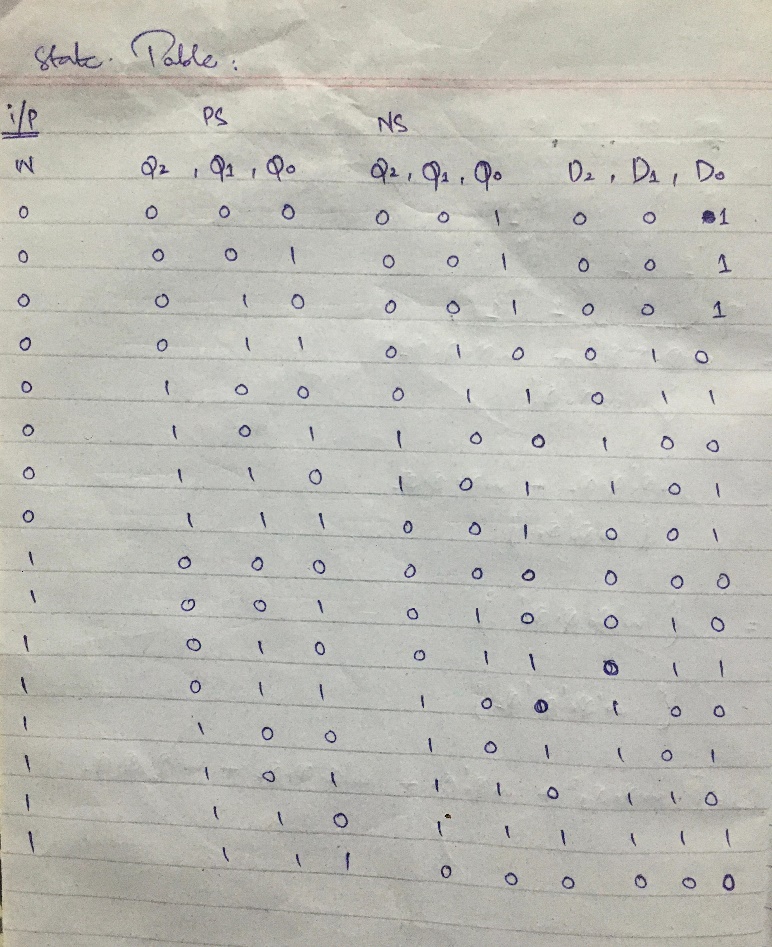
Single-Bit Input: The detector is designed for a single-bit input 'w', representing the binary data stream analysed for the sequence "01111110."

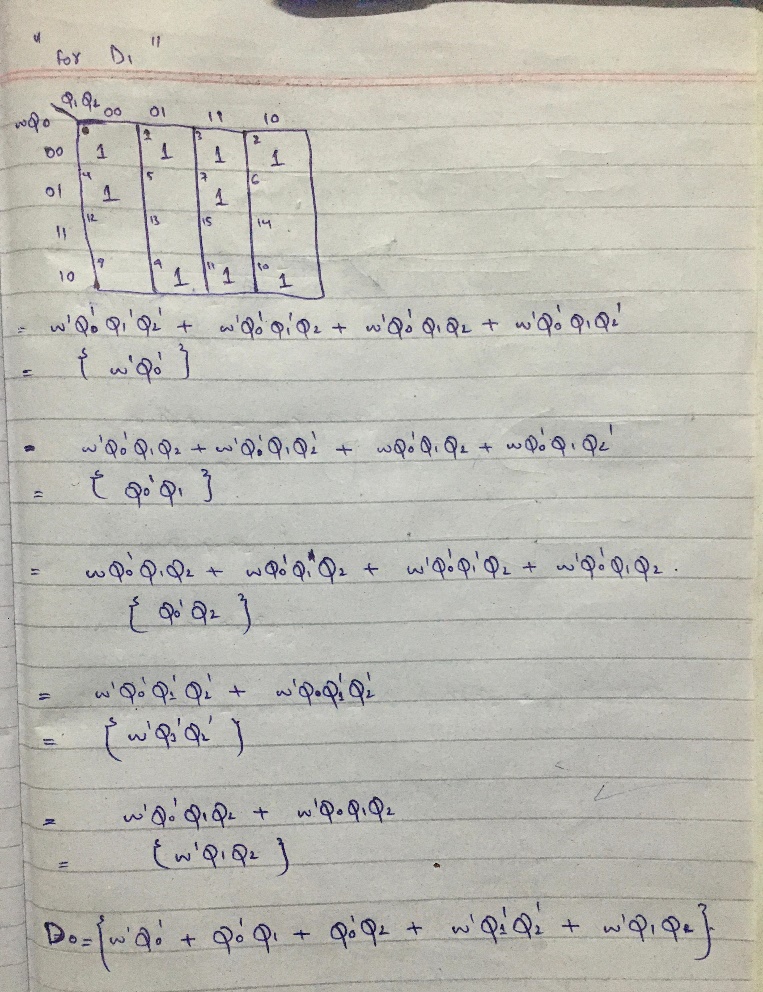
Ideal Logic Gates: The design assumes logic gates are ideal, without propagation delay or glitches, and operate perfectly to produce the expected output.

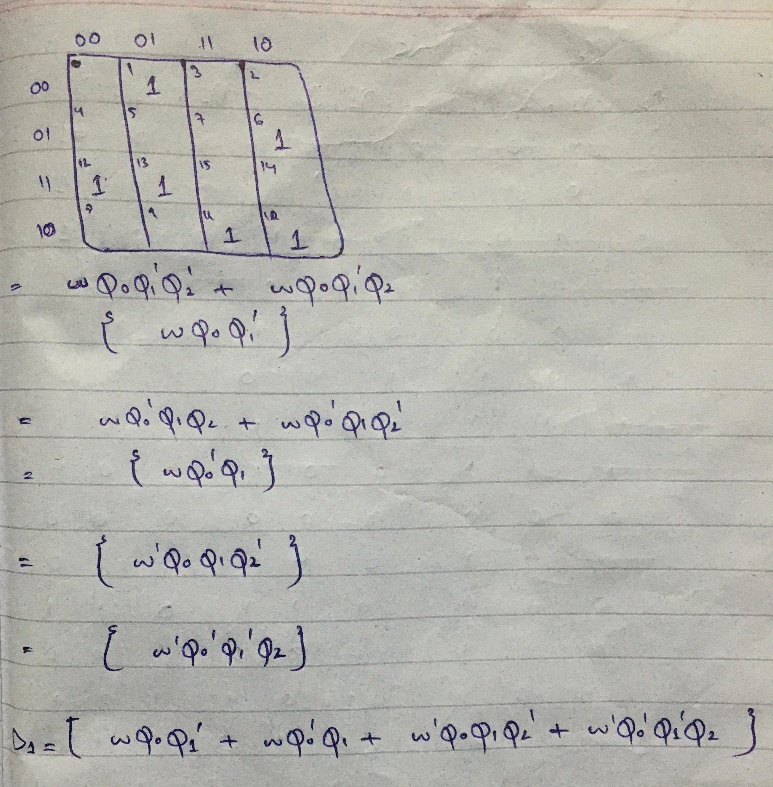
Single-Output Signal: The detector assumes a single output 'z' indicating whether the desired sequence has been detected. A logic high ('1') output is generated when the complete sequence is detected, and a logic low ('0') otherwise.

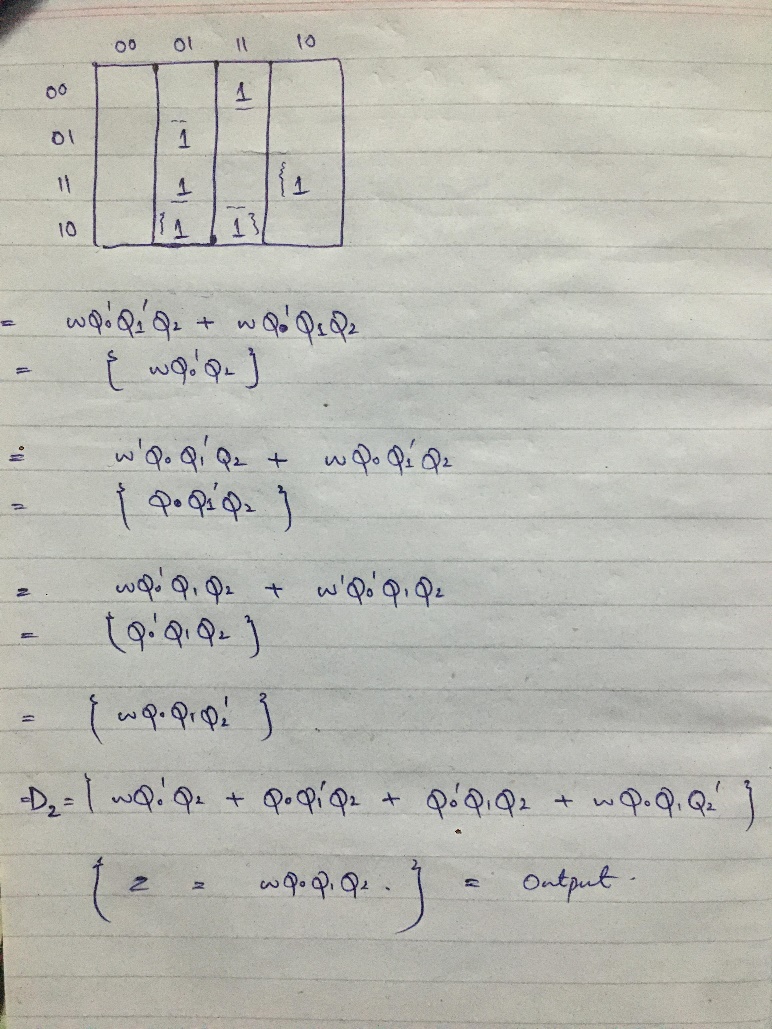
Immediate Preceding Clock Cycles: The detector checks for the desired sequence "01111110" in the immediate preceding clock cycles, not considering data beyond that timeframe.

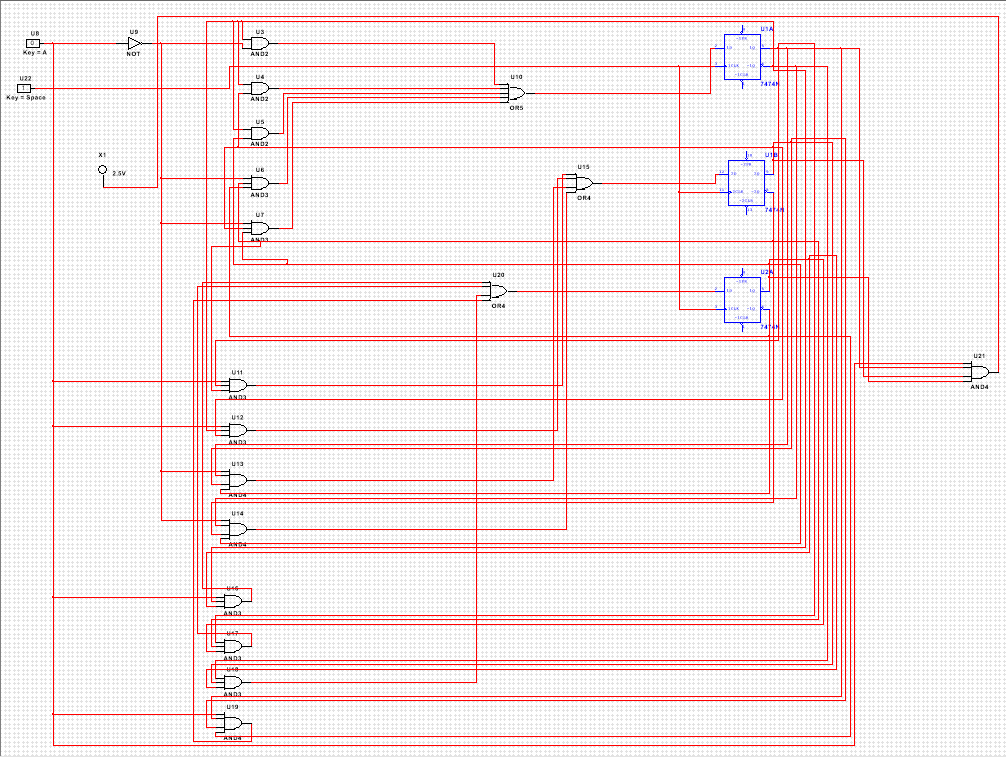
Deterministic Behaviour: The detector assumes the input signal 'w' is deterministically generated, free from noise, random variations, or unexpected patterns, and reliably follows the specified sequence.











**Conclusion**

The sequence detector has been successfully designed and implemented to identify the sequence "01111110" in the immediately preceding clock cycles. Utilizing finite state machine principles, the detector transitions between states based on the input signal 'w' and accurately identifies the target sequence. By generating the output signal 'z' when the sequence is detected, the detector reliably indicates the presence of the sequence.

This designed circuit highlights the importance of sequence detection in various digital applications, enabling enhanced data processing, synchronization, and control capabilities. It acts as a fundamental building block for advanced data processing, synchronization, and decision-making, promoting seamless integration of digital components and ensuring the smooth operation of complex digital systems. Overall, the sequence detector proves to be a critical element in digital circuit design, empowering numerous applications with its robust sequence detection capabilities.