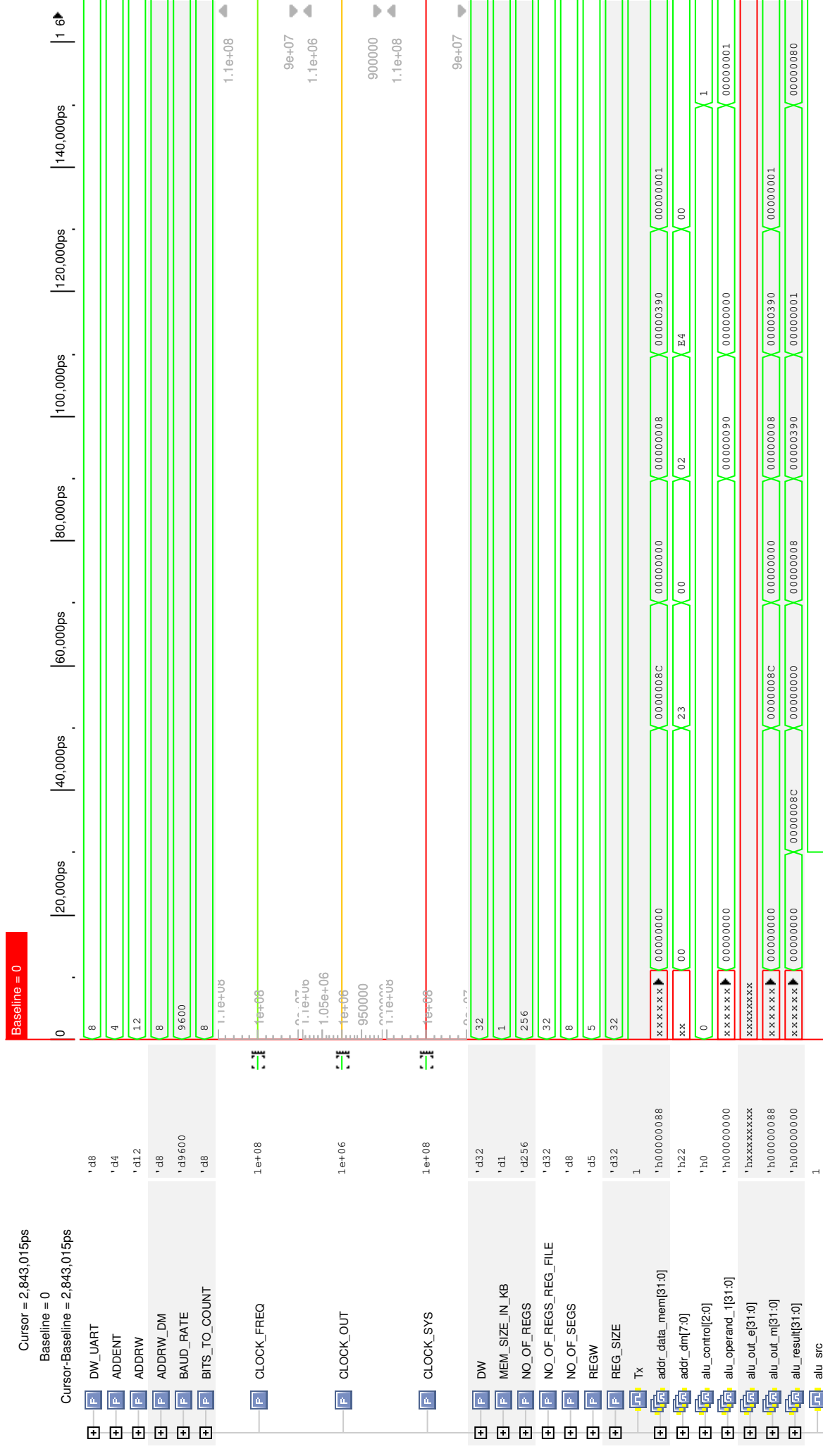


Computer Architecture

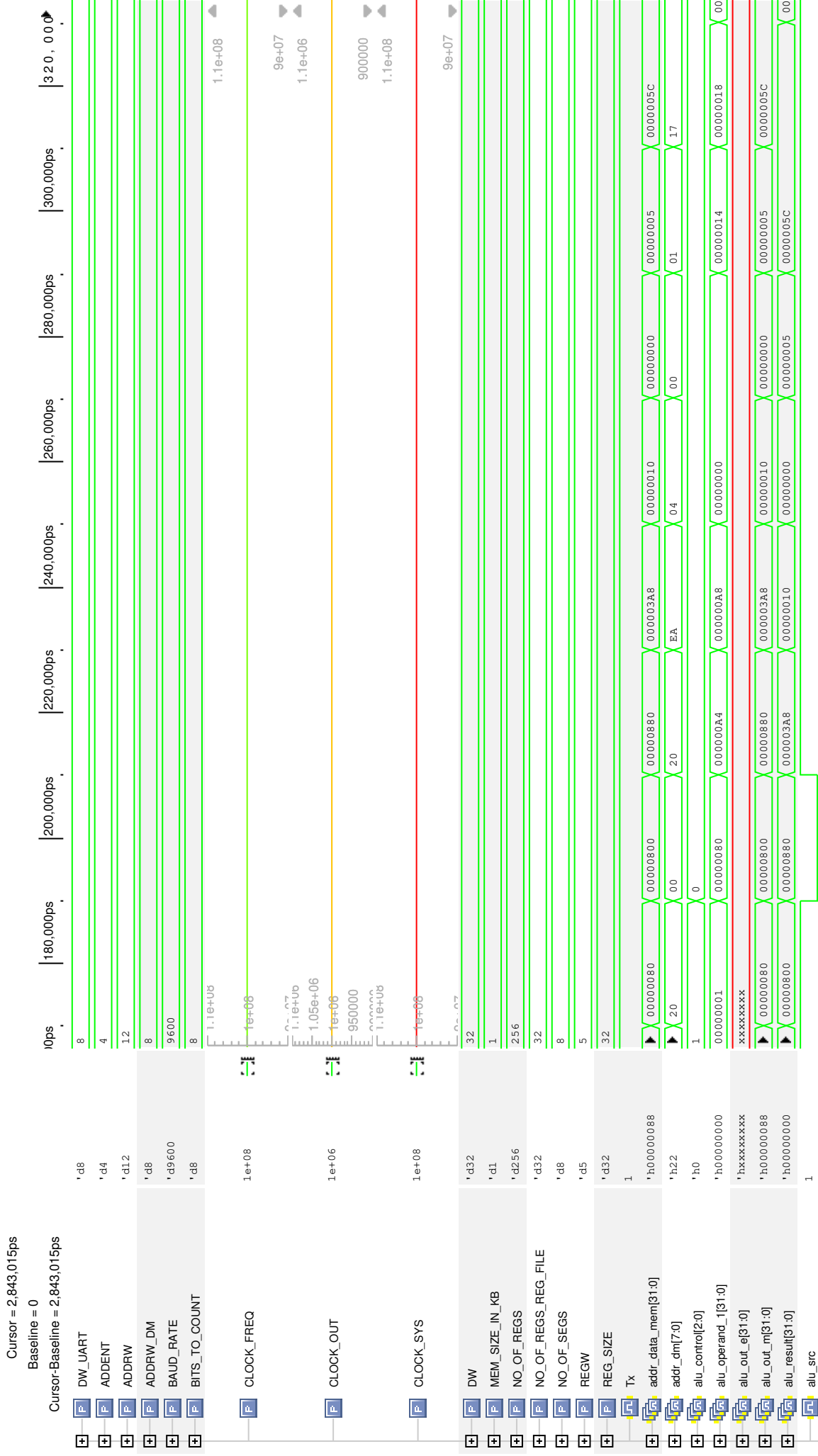
Ahsan Ali (2019-EE-115)

3 stage pipelined RISC-V Core



Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core



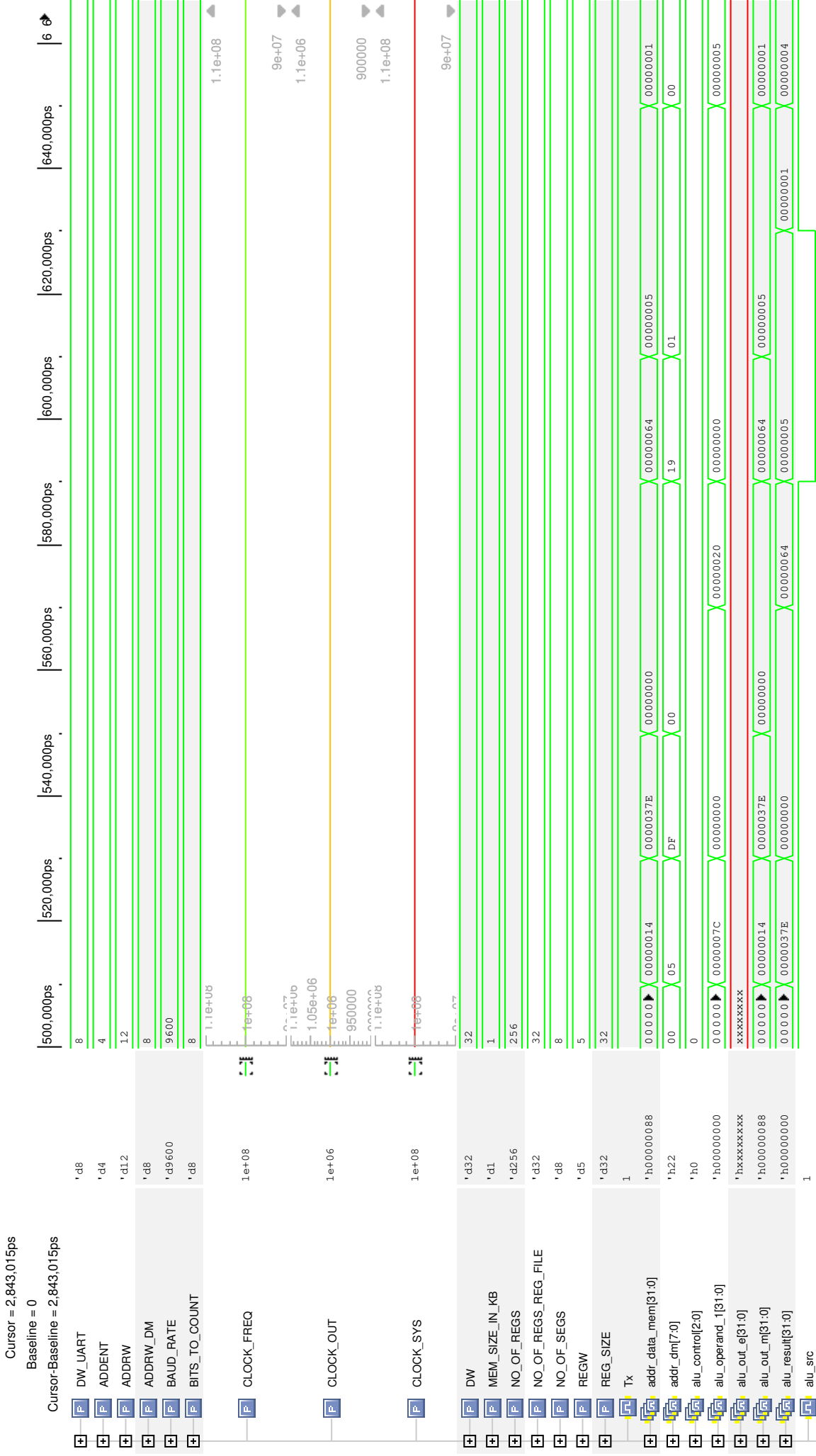
Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core



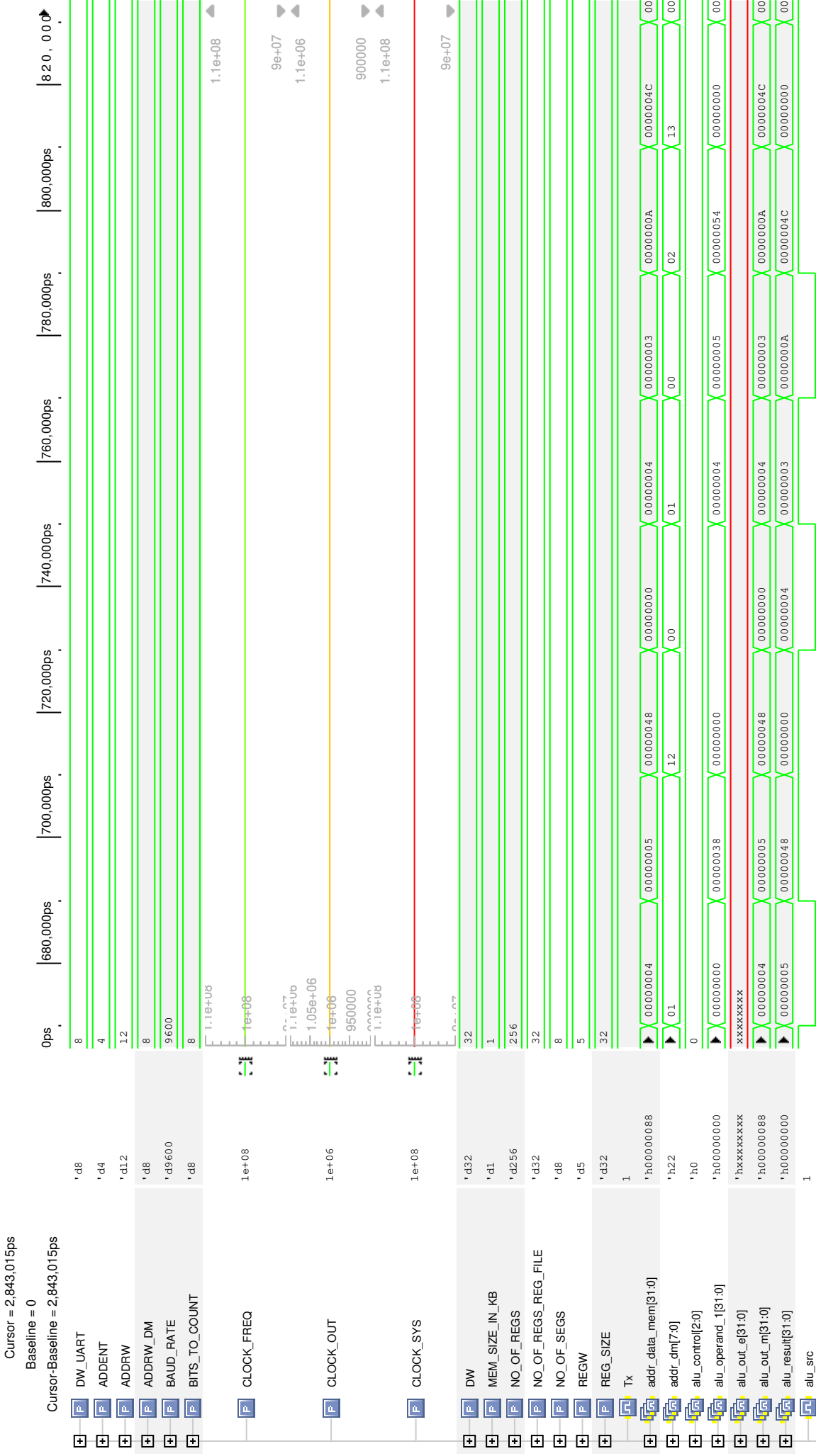
Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core



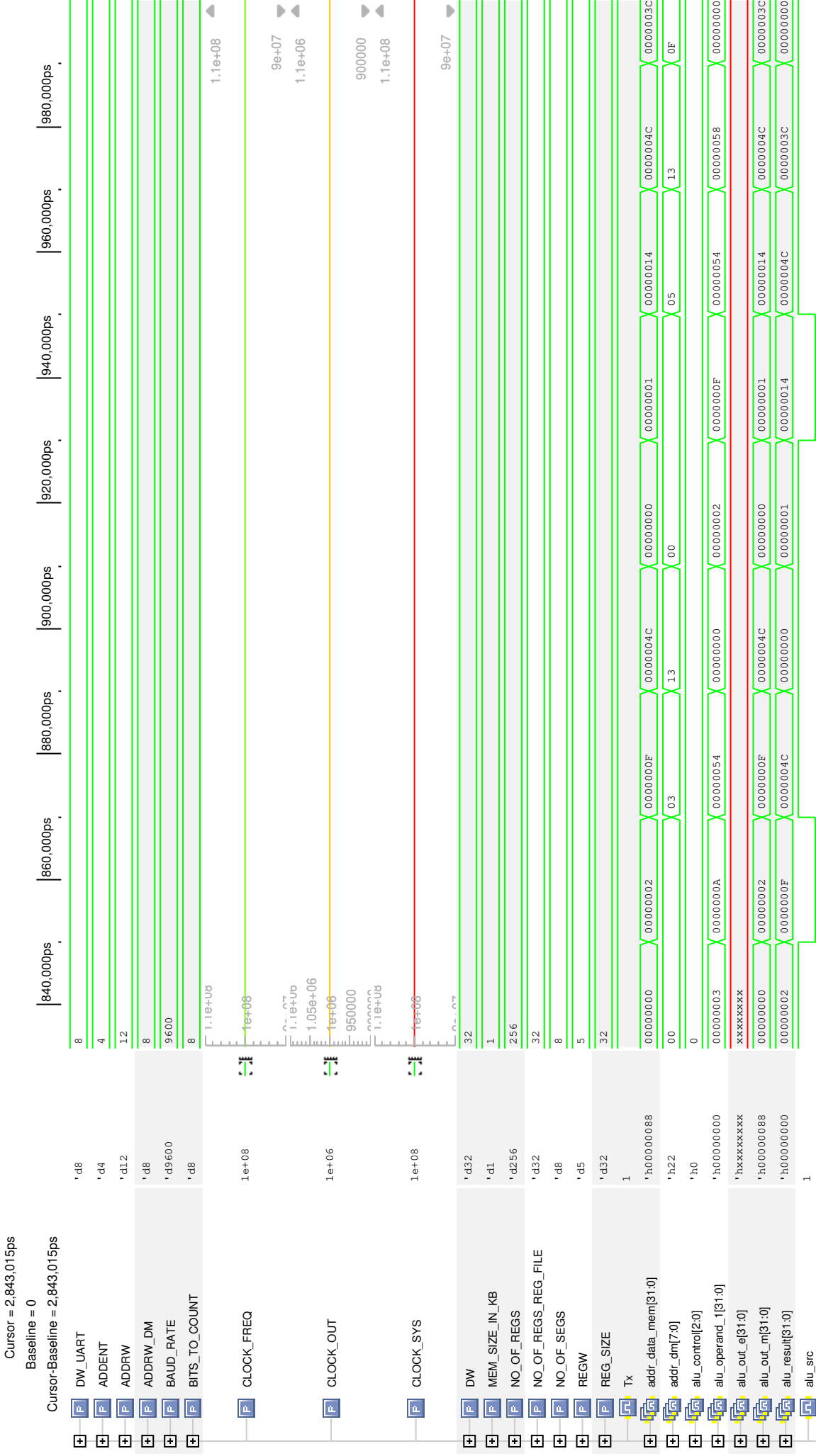
Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core



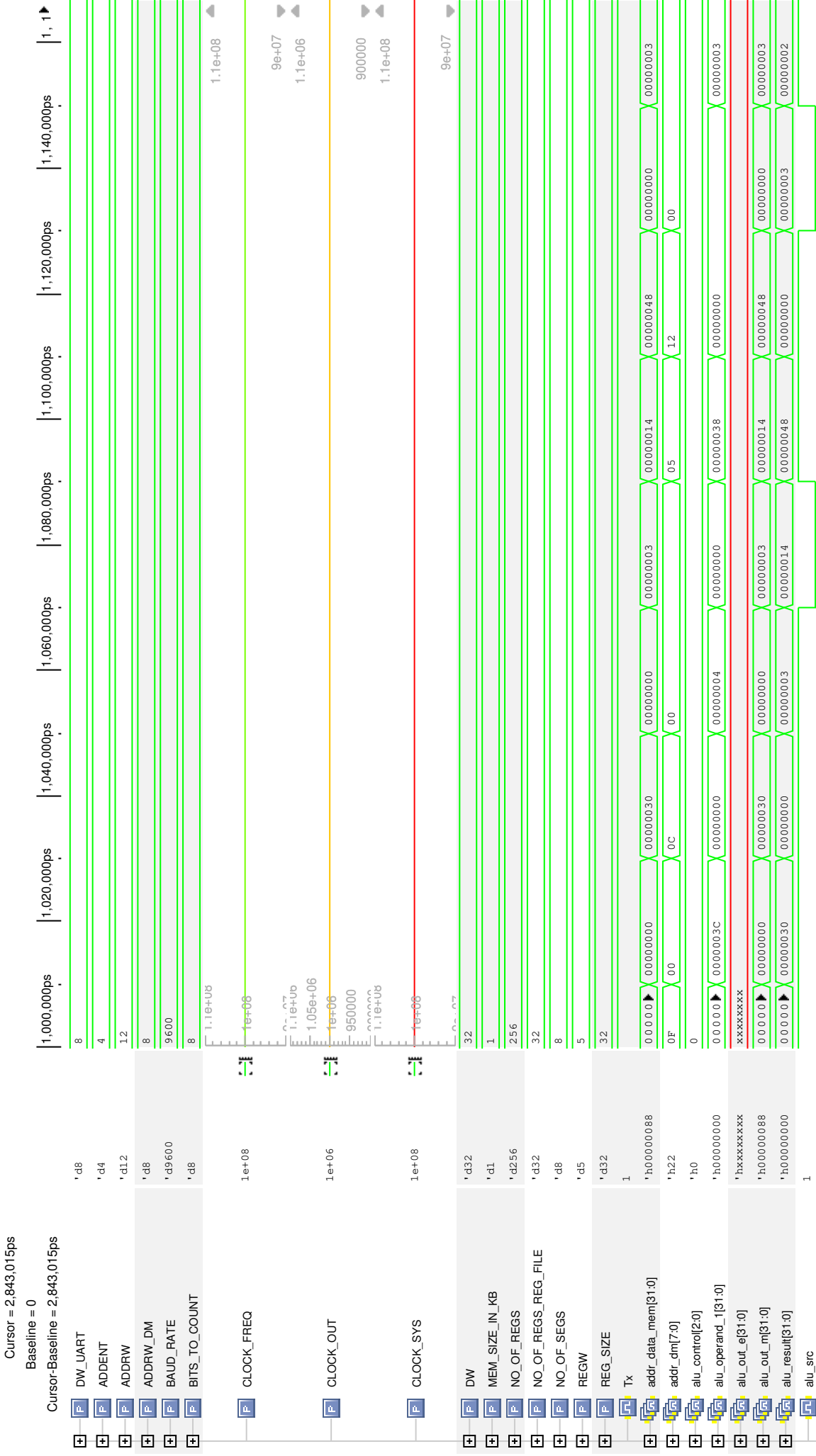
Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core



Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core



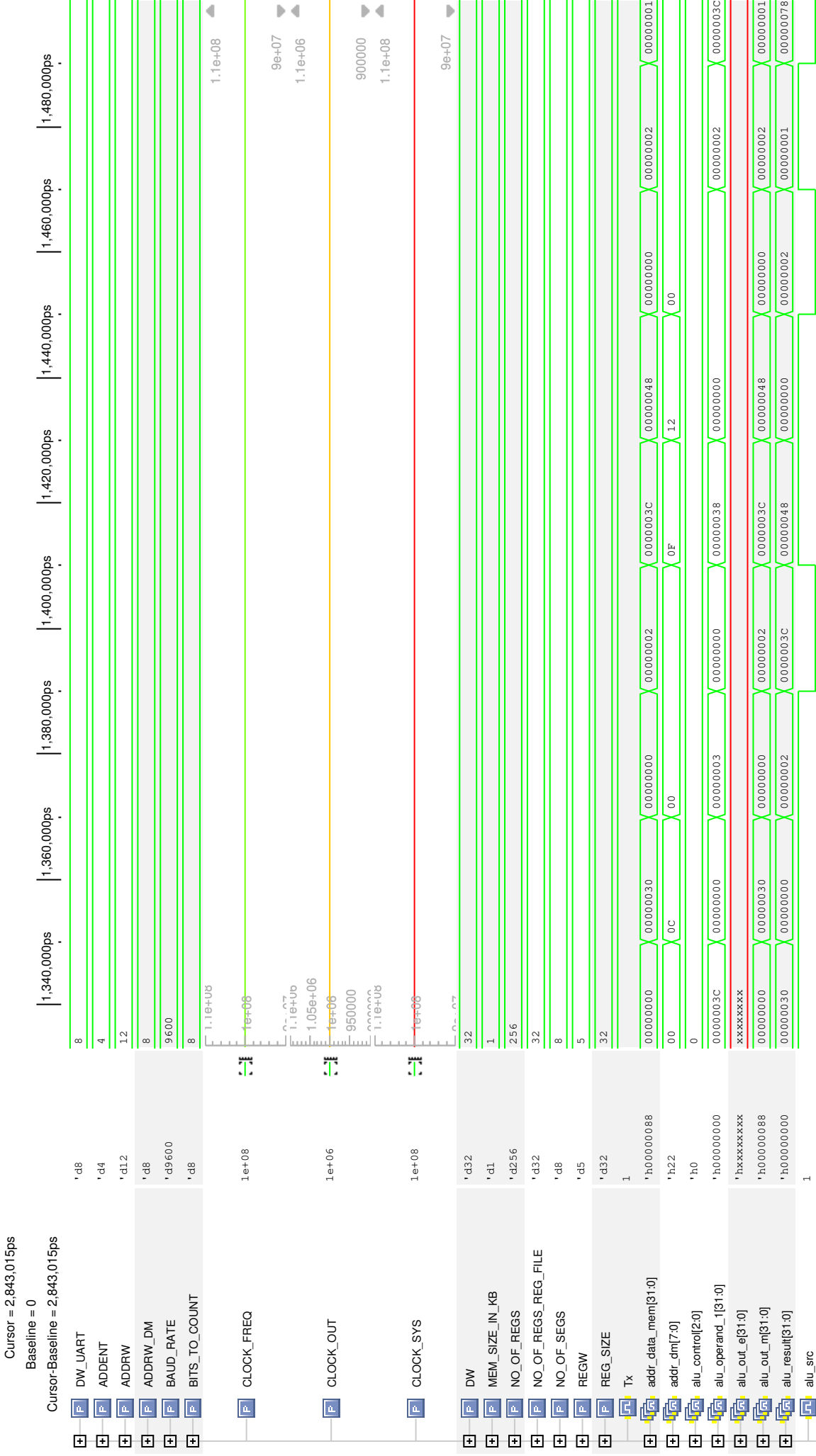
Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core



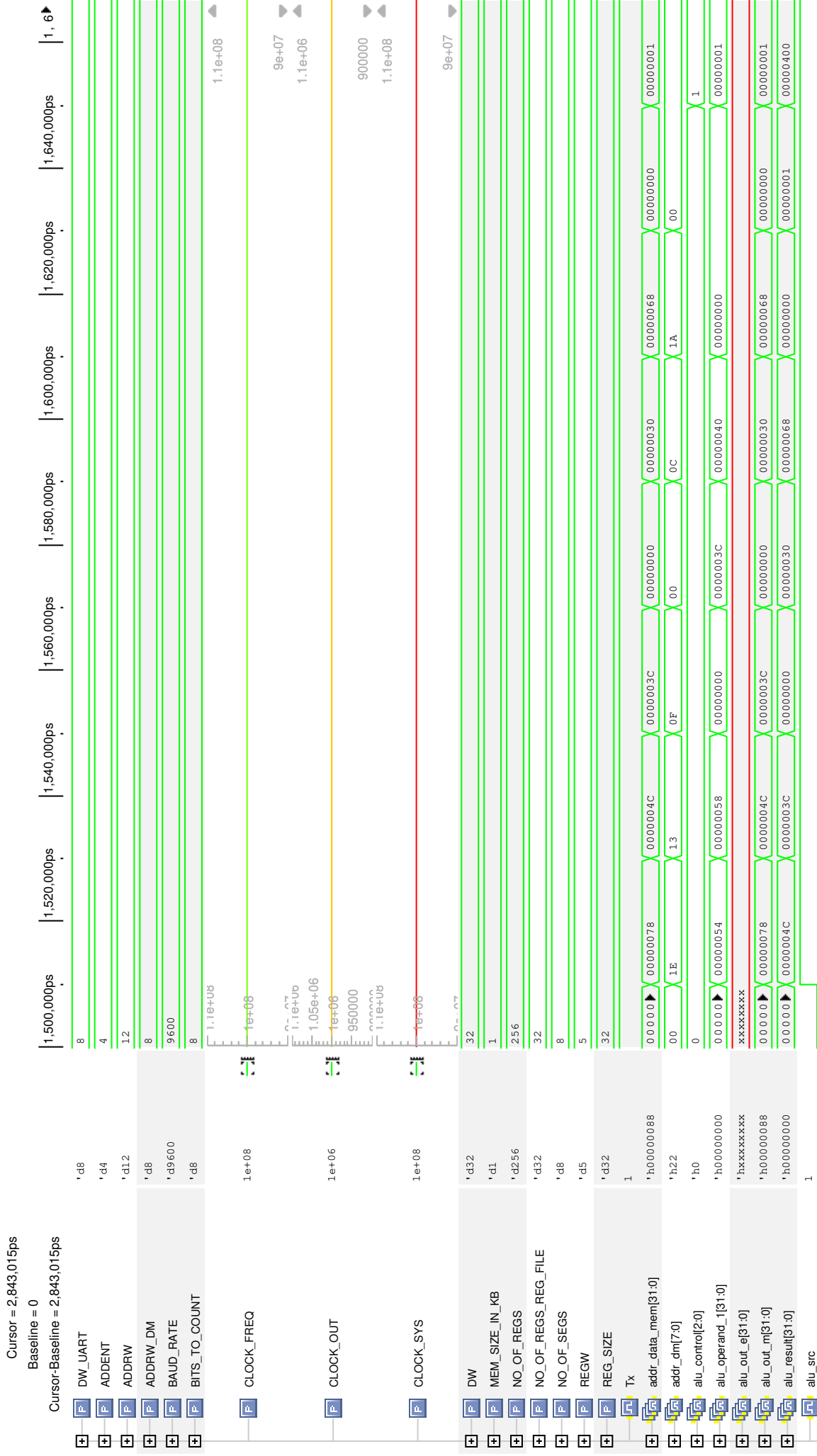
Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core



Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core



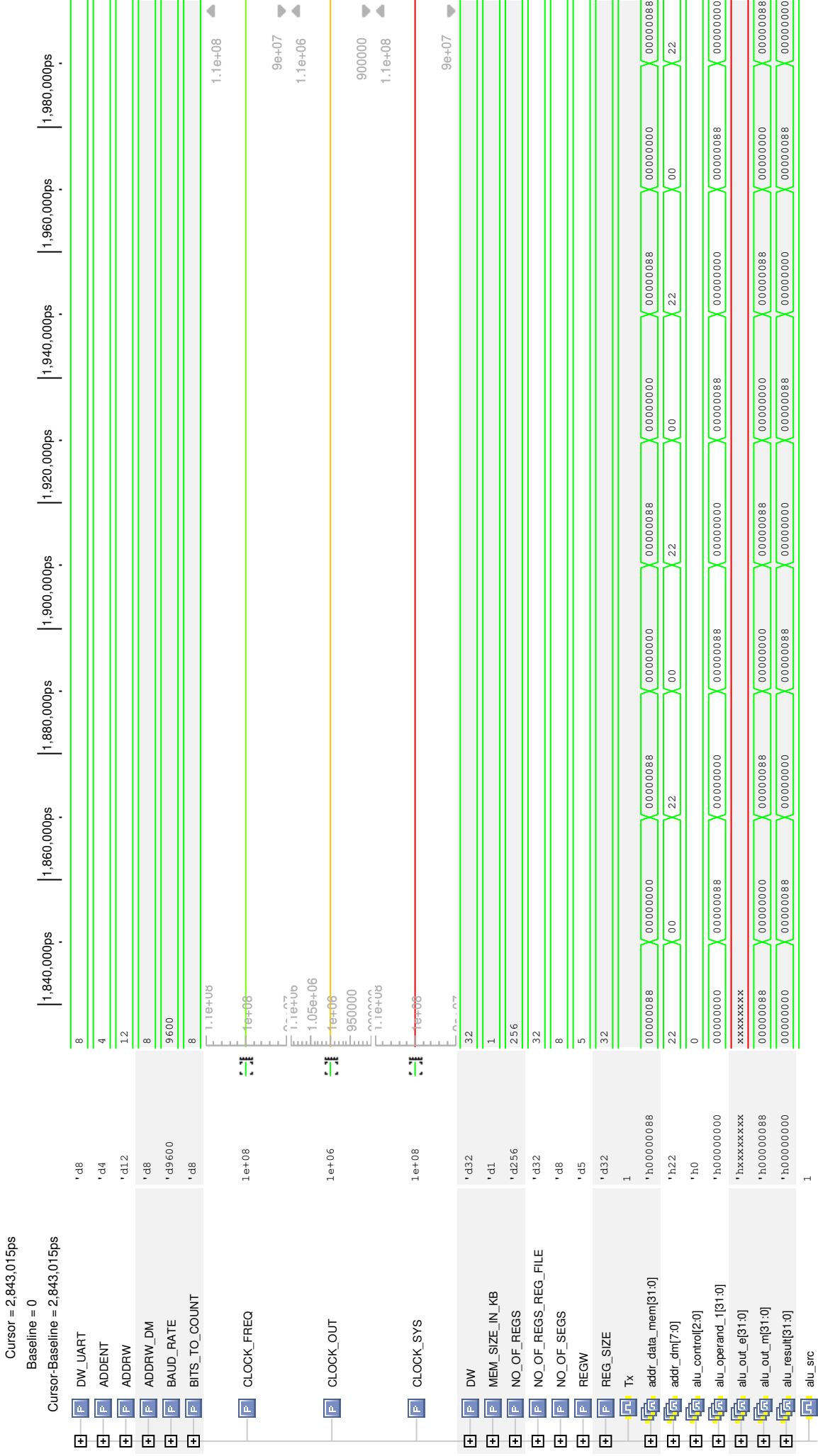
Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core



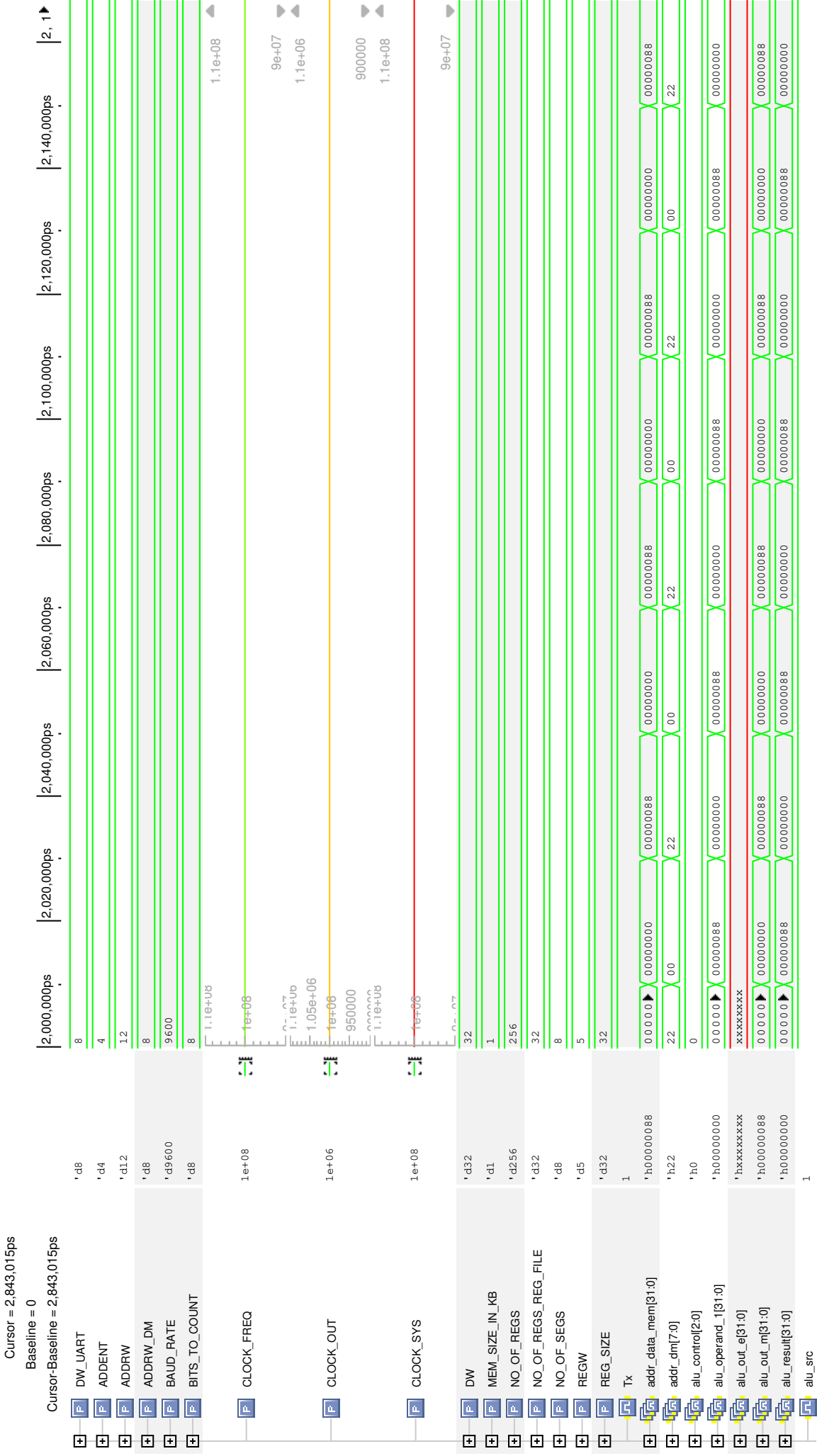
Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core



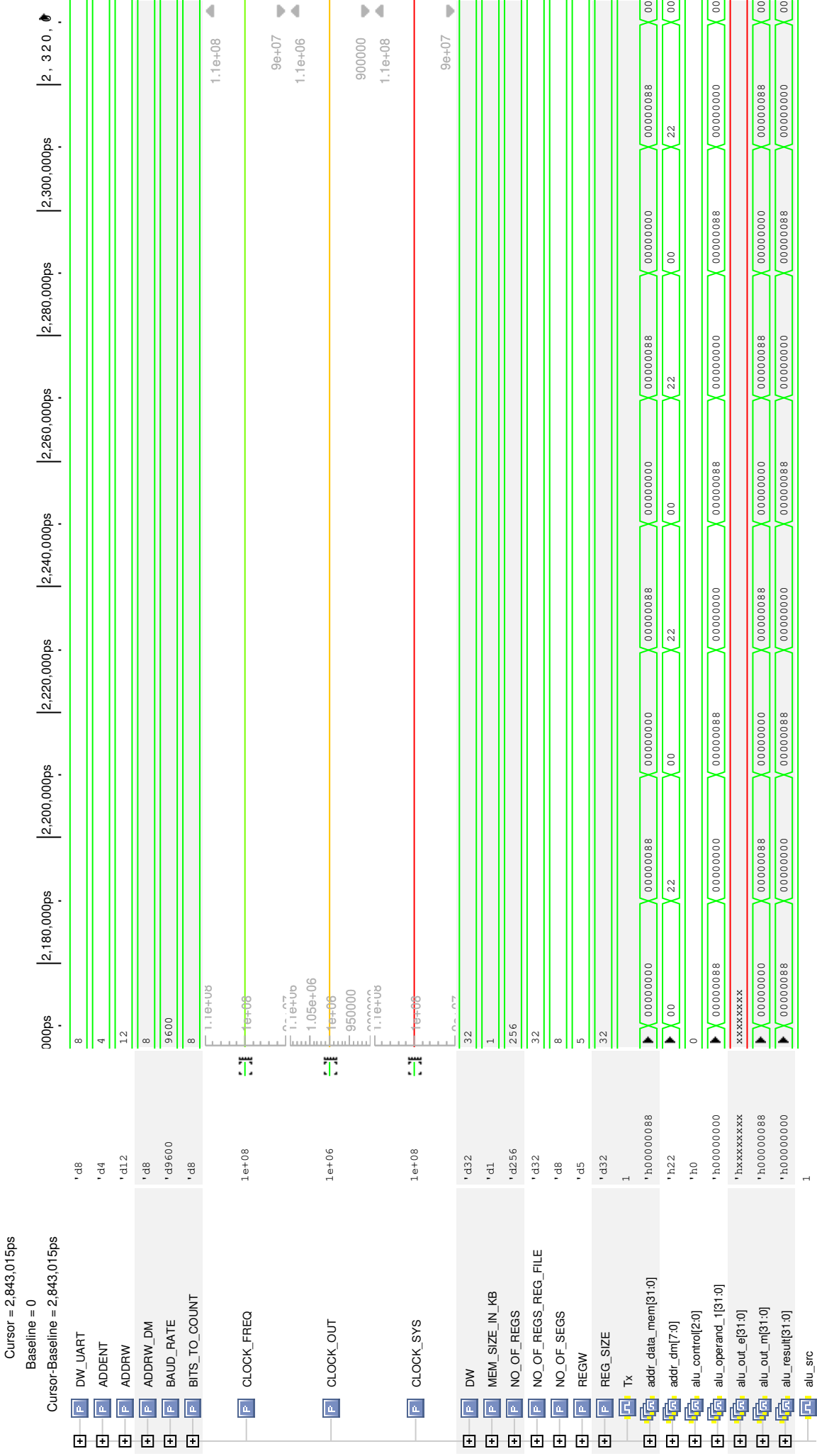
Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core



Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core

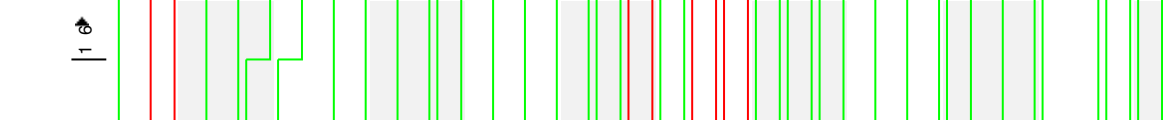


Computer Architecture

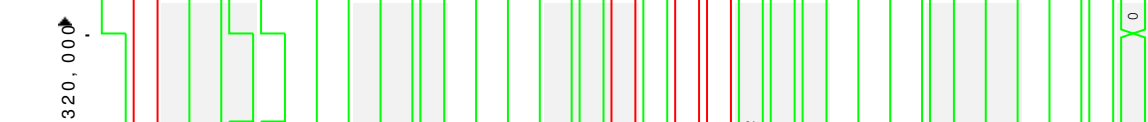
Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core



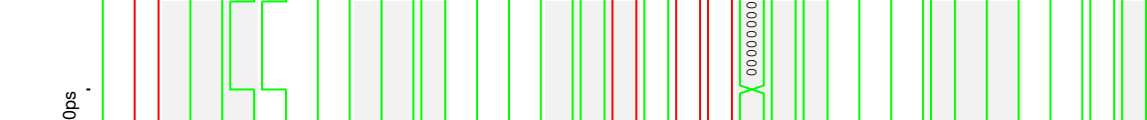
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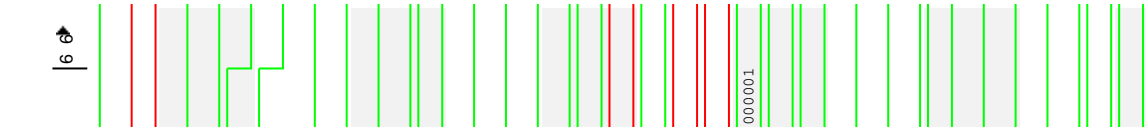
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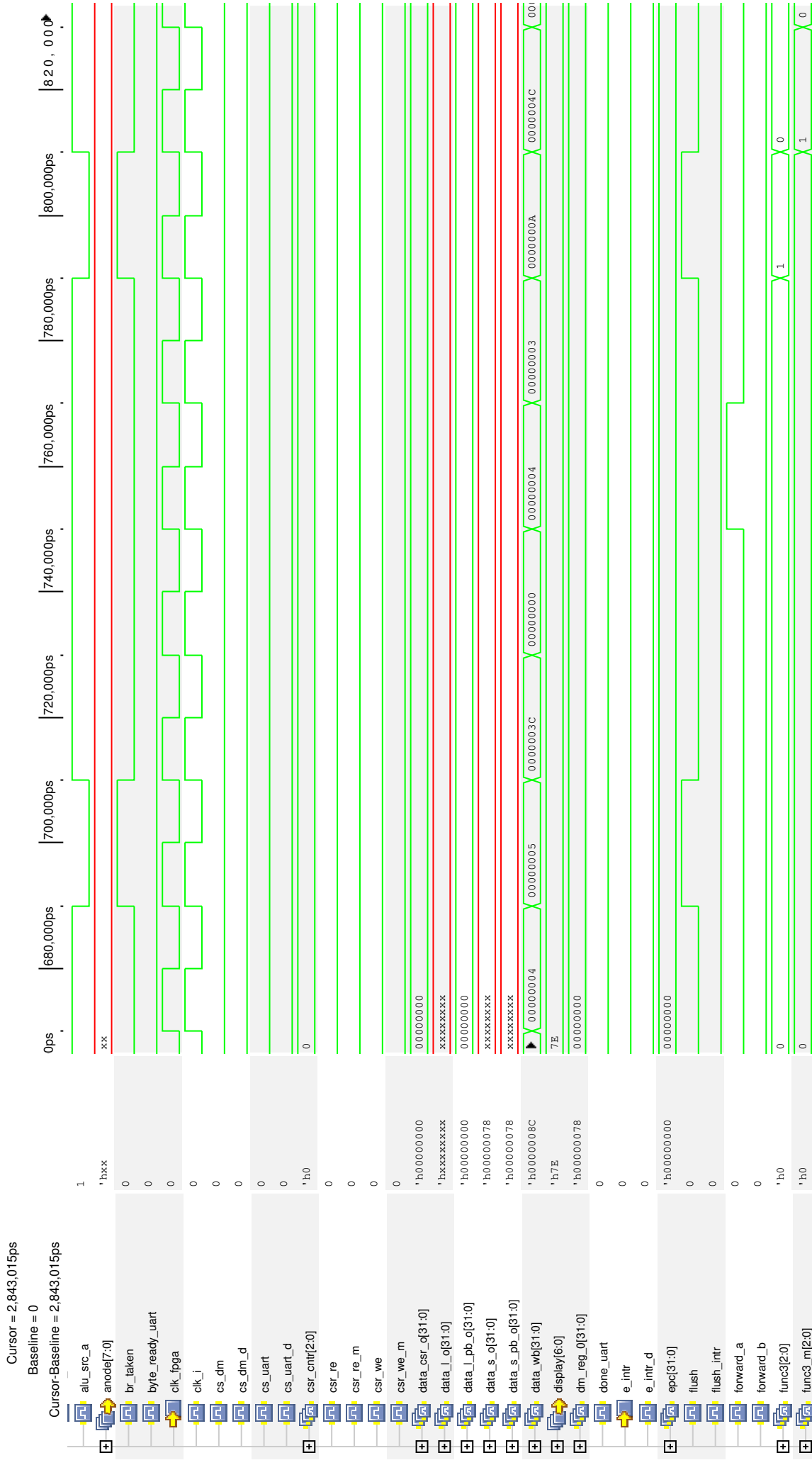


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Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core



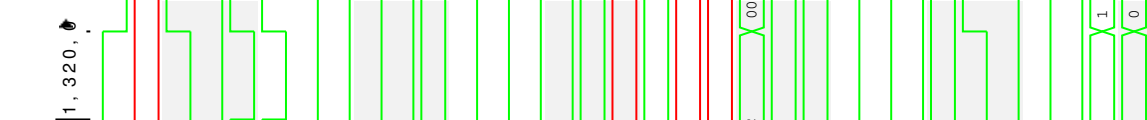
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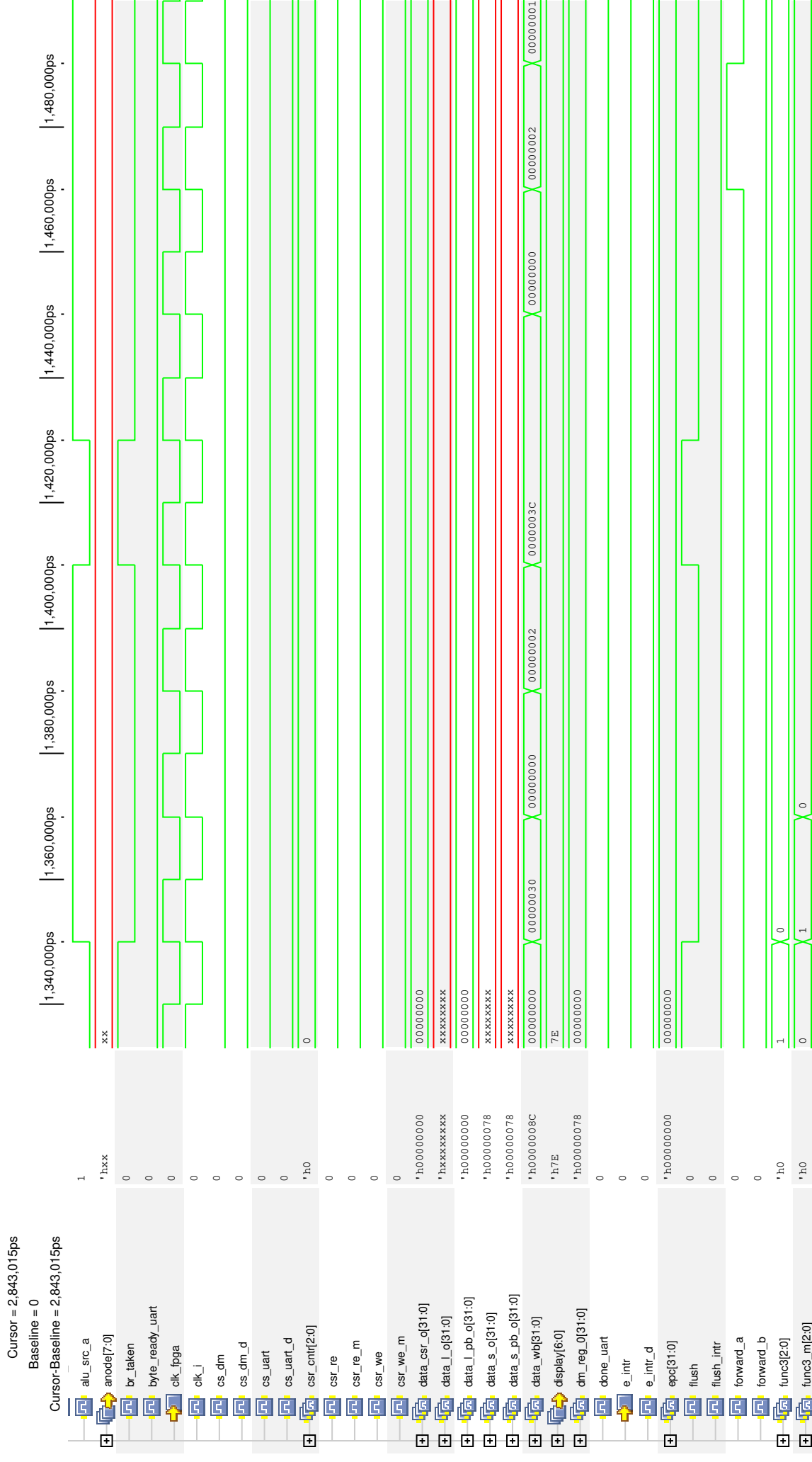
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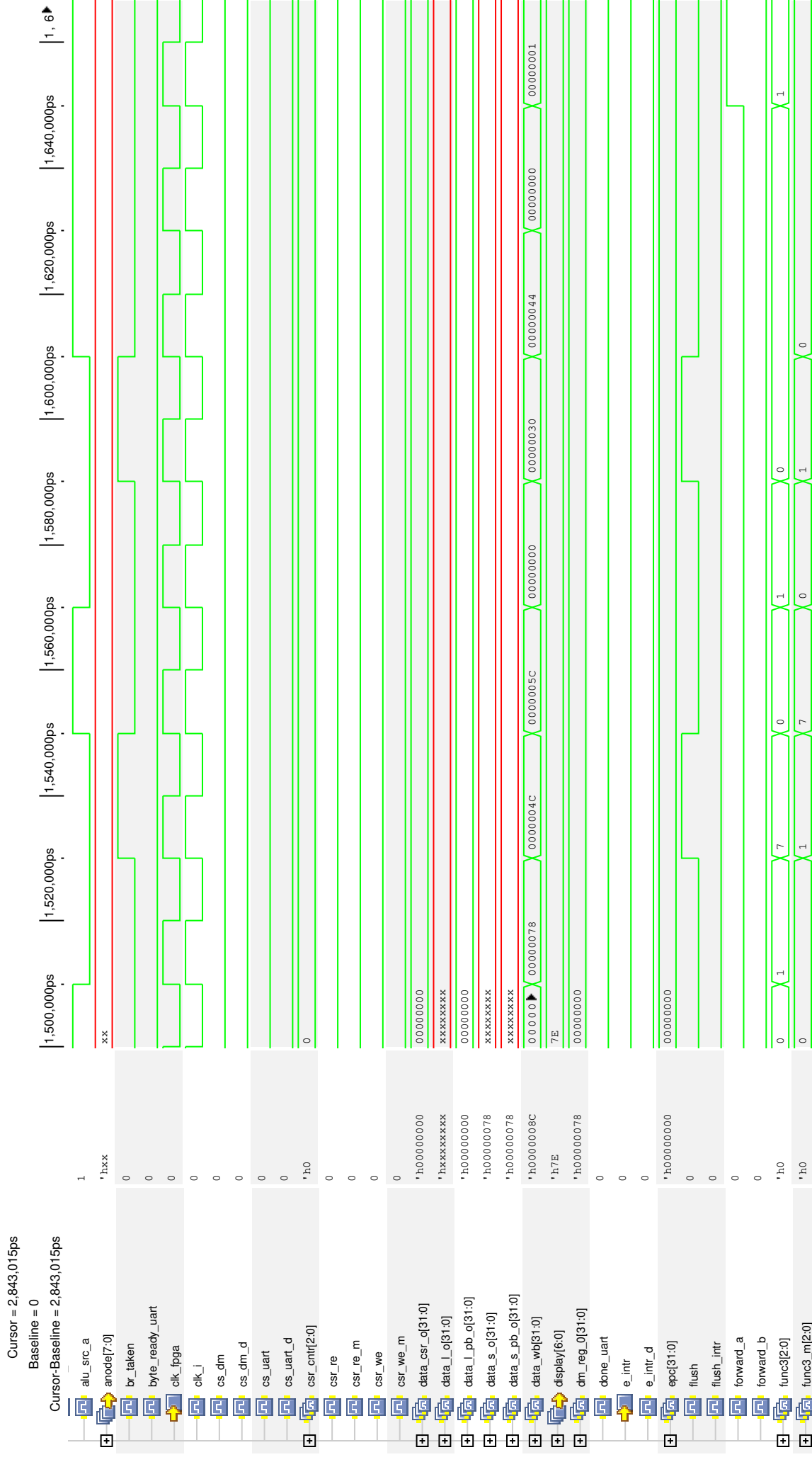
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Computer Architecture

Ahsan Ali (2019-EE-115)

3 stage pipelined RISC-V Core

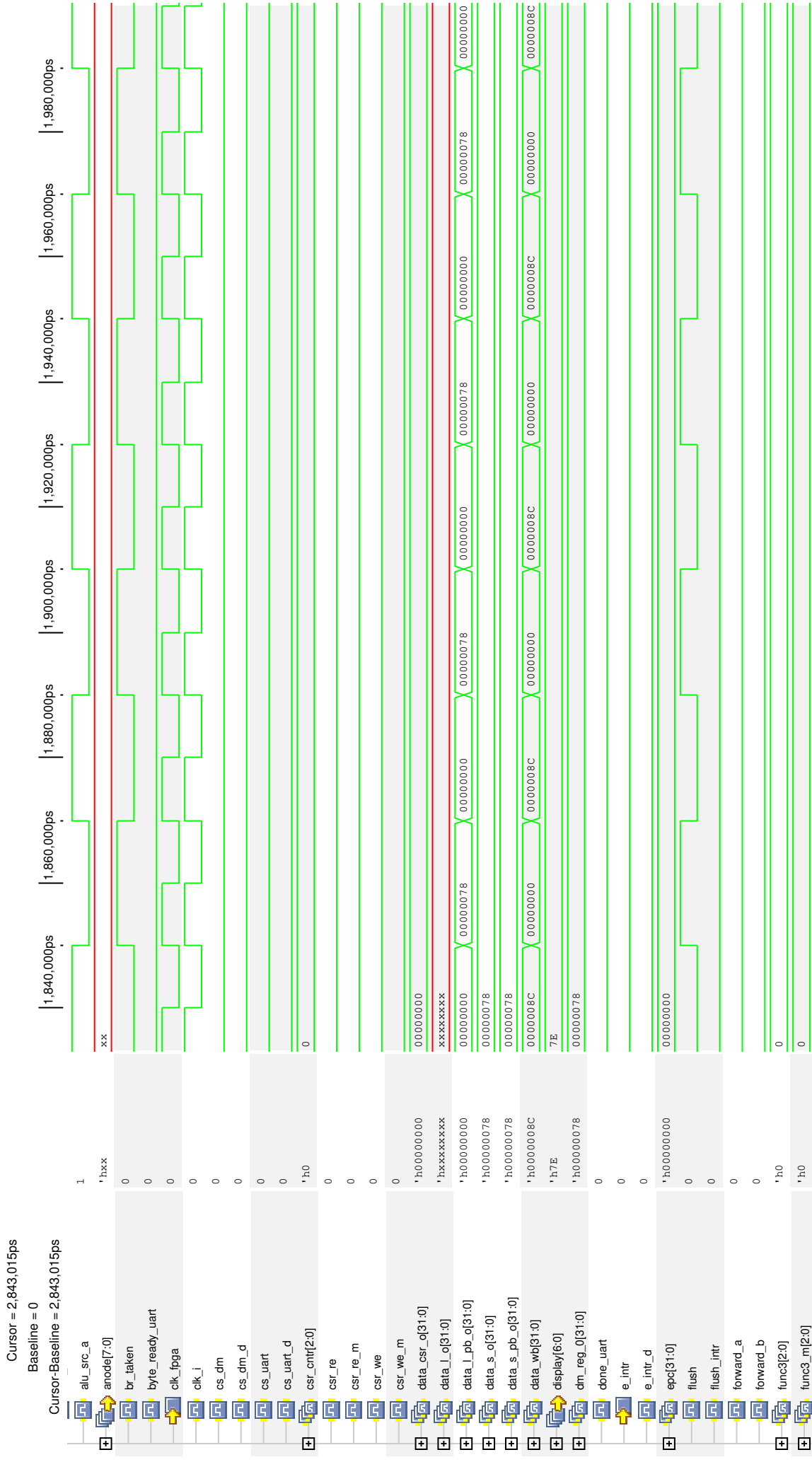


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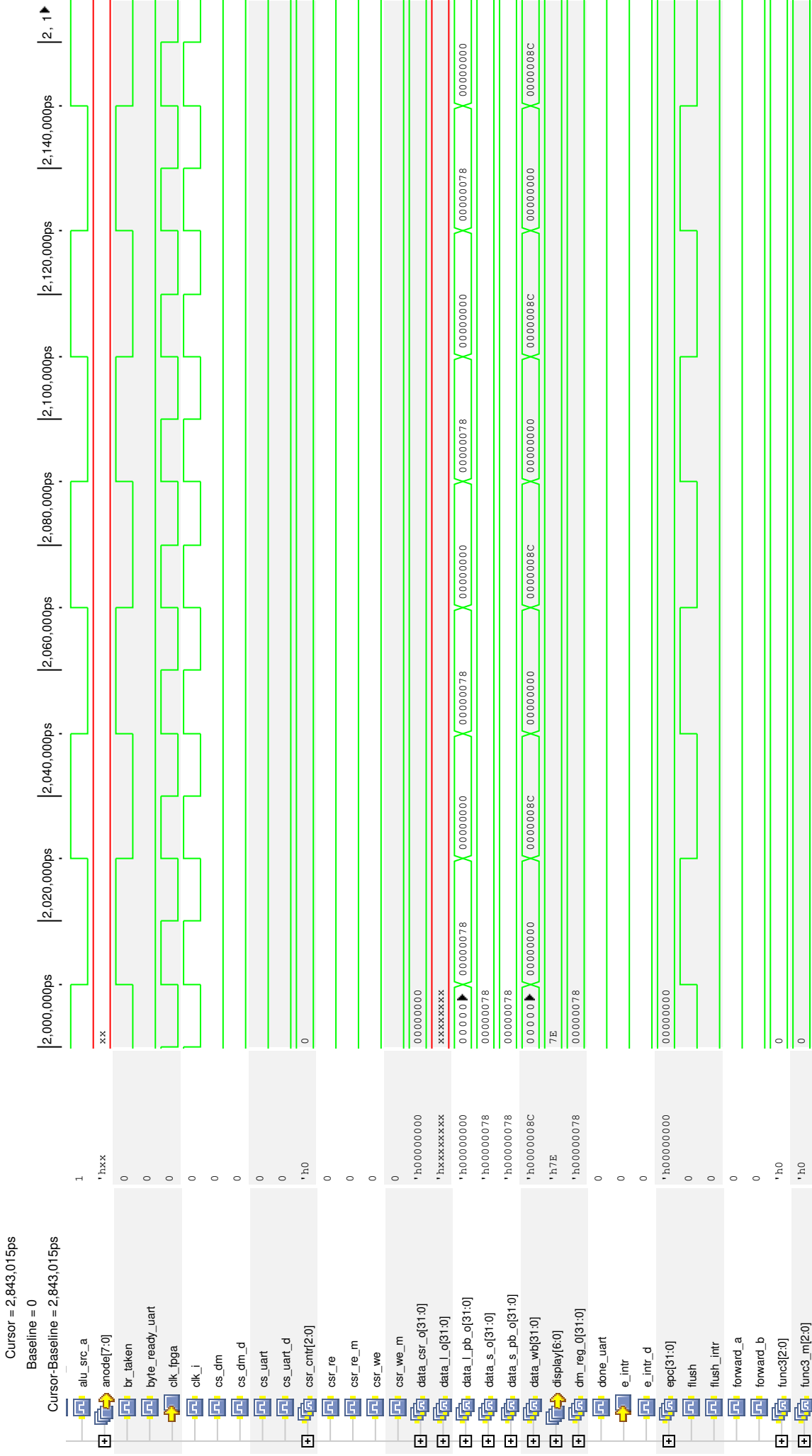
Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core



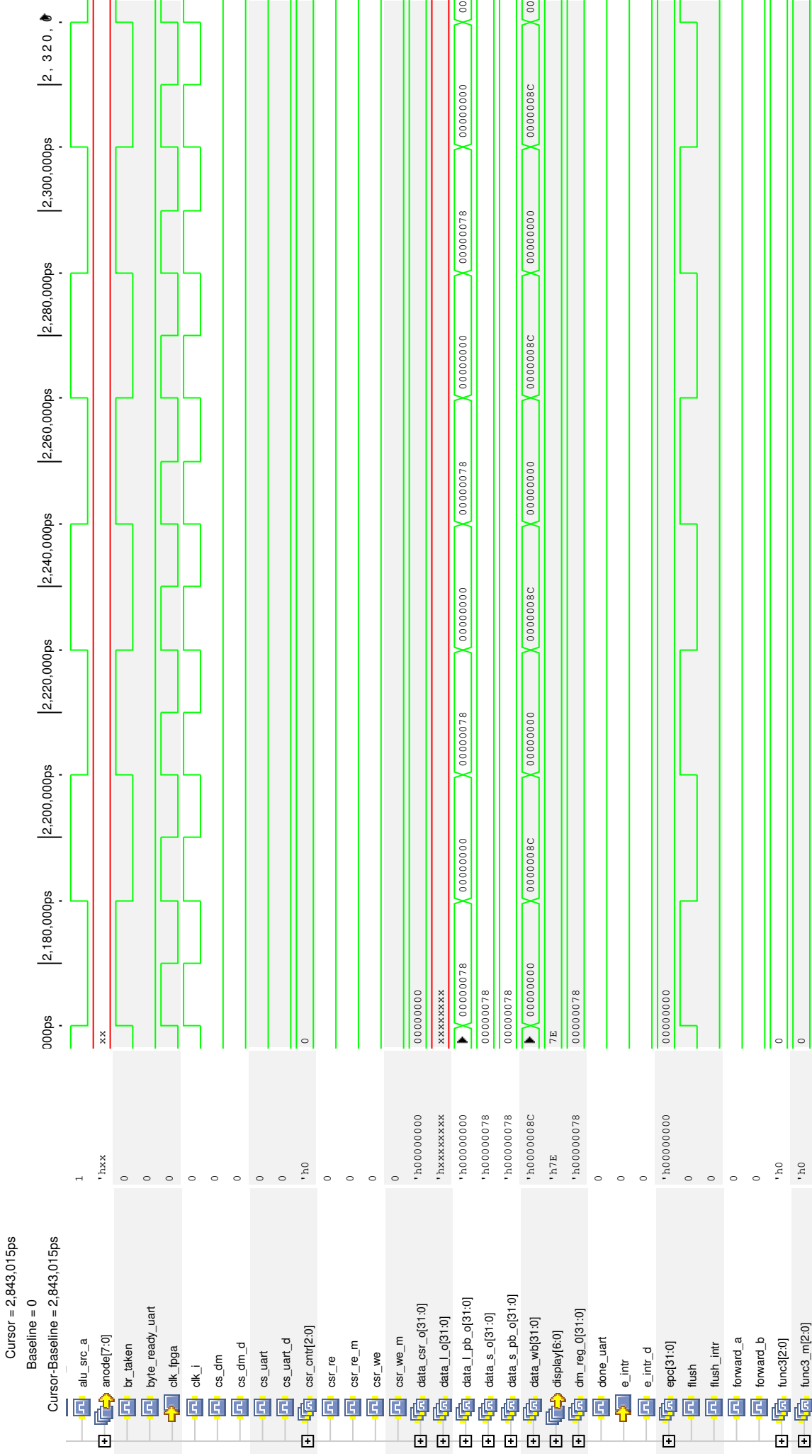
Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core

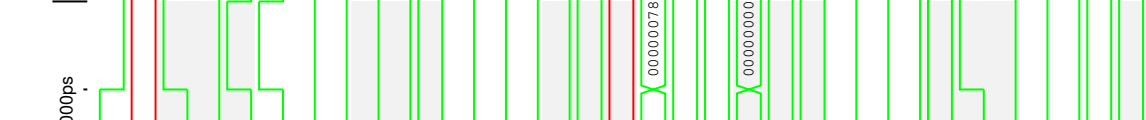


Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core



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Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core



Computer Architecture

Ahsan Ali (2019-EE-115)

UET

3 stage pipelined RISC-V Core


































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Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core
































Cursor = 2,843,015ps
Baseline = 0
Cursor-Baseline = 2,843,015ps

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	going_in_alu_a[31:0]	'h00000000	00000000	00000005	00000000			
	going_in_alu_b[31:0]	'h00000000	00000000	00000002	00000000			
	imm_csr_d[31:0]	'hxxxxxxxx	xxxxxxxx					
	imm_csr_m[31:0]	'h00000000	00000002	00000044	00000003	00000000	00000070	00000000
	imm_ext[31:0]	'h00000000	00000002	00000044	00000003	00000000	00000070	00000014
	imm_ext_d[31:0]	'h00000000	00000044	00000002	00000044	00000003	00000000	
	imm_src[2:0]	'h0	2	0	0	3	0	
	inst_o[31:0]	'h0000006F	04118263	00300233	00128293	0700006F	01400A13	30200073
	instr_d[31:0]	'h00000013	00200093	04118263	00300233	00000013	00000013	01400A13
	instr_m[31:0]	'h0000006F	04018263	00200093	04118263	00300233	00000013	00000013
	intr	0						
	is_mret	0						
	mask[3:0]	'hF	x					
	mask_dm[3:0]	'hF	x					
	mem_write	0						
	mem_write_m	0						
	opcode_d[6:0]	'h13	13	63	33	13	6F	13
	opcode_ff[6:0]	'h6F	63	33		13	6F	73
	opcode_m[6:0]	'h6F	63	13	63	33	13	13
	pc[31:0]	'h00000088	00000020	00000024	00000028	00000008	0000000C	0000007C
	pc_d[31:0]	'h00000088	0000001C	00000020	00000024	00000028	00000008	00000078
	pc_final[31:0]	'h0000008C	00000024	00000028	0000002C	00000008	00000078	00000080
	pc_m[31:0]	'h00000088	00000018	0000001C	00000020	00000024	00000028	00000008
	pc_next[31:0]	'h0000008C	00000024	00000028	0000002C	00000030	0000000C	0000007C
	pc_plus_4[31:0]	'h0000008C	00000024	00000028	0000002C	00000030	0000000C	00000080
	pc_plus_4_d[31:0]	'h0000008C	00000020	00000024	00000028	0000002C	0000000C	0000007C
	pc_plus_4_m[31:0]	'h0000008C	0000001C	00000020	00000024	00000028	0000002C	
	pc_target[31:0]	'h0000008C	00000024	00000028	0000002C	00000030	0000000C	00000080
	rd_m[4:0]	'h0	04	01	04	02	00	
	rdata1[31:0]	'h00000000	00000000	00000005	00000000			
	rdata2[31:0]	'h00000000	00000000	00000000	00000000	00000000		
	rdata_data_mem[31:0]	'h00000000	00000000	00000000	00000000	00000000		

Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core

Cursor = 2,843,015ps
Baseline = 0
Cursor-Baseline = 2,843,015ps

	func7[6:0]	'h00	18	00	02	00	580,000ps	600,000ps	620,000ps	640,000ps	6
	going_in_alu_a[31:0]	'h00000000				00000005	00000000			00000005	
	going_in_alu_b[31:0]	'h00000000				00000002	00000005			00000002	
	imm_csr_d[31:0]	'hxxxxxxxx									
	imm_csr_m[31:0]	'h00000000				00000000	00000044			00000003	00000001
	imm_ext[31:0]	'h00000000				00000000	00000044			00000001	FFFFFFF
	imm_ext_d[31:0]	'h00000000				00000014	00000000			00000003	00000001
	imm_src[2:0]	'h0	5	0	2	0					
	inst_o[31:0]	'h0000006F				04118263	00300233			00128293	004001B3
	instr_d[31:0]	'h00000013				00000013	00300233			00300133	FFF10113
	instr_m[31:0]	'h0000006F				00000013	00300233			00300133	00128293
	intr	0									
	is_mret	0									
	mask[3:0]	'hF									
	mask_dm[3:0]	'hF									
	mem_write	0									
	mem_write_m	0									
	opcode_d[6:0]	'h13	73	13	63	33				13	
	opcode_ff[6:0]	'h6F	13	63	33					13	33
	opcode_m[6:0]	'h6F	13	73		13	63	33			13
	pc[31:0]	'h00000088				00000020	00000024	00000028	0000002C	00000030	00000034
	pc_d[31:0]	'h00000088					00000020	00000024	00000028	0000002C	00000030
	pc_final[31:0]	'h0000008C				00000020	00000028	0000002C	00000030	00000034	00000038
	pc_m[31:0]	'h00000088				00000078	00000020	00000028	00000024	00000028	0000002C
	pc_next[31:0]	'h0000008C				00000084	00000024	00000028	00000030	00000034	00000038
	pc_plus_4[31:0]	'h0000008C				00000084	00000024	00000028	00000030	00000034	00000038
	pc_plus_4_d[31:0]	'h0000008C					00000024	00000028	0000002C	00000030	00000034
	pc_plus_4_m[31:0]	'h0000008C				0000007C	00000080	00000024	00000028	0000002C	00000030
	pc_target[31:0]	'h0000008C				00000084	00000024	00000028	00000030	00000034	00000038
	rd_m[4:0]	'h00	14	00		04			02		05
	rdata1[31:0]	'h00000000					00000005	00000000			00000005
	rdata2[31:0]	'h00000000				00000000				00000002	00000000
	rdata_data_mem[31:0]	'h00000000									

Computer Architecture

Ahsan Ali (2019-EE-115)

UET

3 stage pipelined RISC-V Core

Cursor = 2,843,015ps

Baseline = 0
































Cursor-Baseline = 2,843,015ps

	func7[6:0]	'h00	00	7F	00	7F	00	7F
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	going_in_alu_b[31:0]	'h00000000	00000005	00000000	00000005	00000001	00000000	00
	imm_csr_d[31:0]	'hxxxxxxxxxx						
	imm_csr_m[31:0]	'h00000000	FFFFFFF	00000004	00000010	00000002	FFFFFFF	001
	imm_ex[31:0]	'h00000000	00000004	00000010	00000000	FFFFFFF	00000003	FFFFF8
	imm_ext_d[31:0]	'h00000000	FFFFFFF	00000004	00000000	FFFFFFF	00000003	001
	imm_src[2:0]	'h0	0	3	0	2	0	
	inst_o[31:0]	'h0000006F	FE111AE3	002003B3	FFF38393	00320233	FE539CE3	FFF38393
	instr_d[31:0]	'h00000013	004001B3	0100006F	00000013	FFF38393	00320233	FE539CE3
	instr_m[31:0]	'h0000006F	FFf10113	004001B3	0100006F	00000013	FFF38393	00320233
	intr	0						
	is_mret	0						
	'hf	'hf						
	mask[3:0]	'hf						
	mask_dm[3:0]	'hf						
	mem_write	0						
	mem_write_m	0						
	opcode_d[6:0]	'hi13	33	6F	13	13	63	13
	opcode_ff[6:0]	'h6F	6F	63	33	63	6F	13
	opcode_m[6:0]	'h6F	13	33	6F	33	33	63
	pc[31:0]	'h00000088	00000038	0000003C	00000048	00000050	00000058	0000004C
	pc_d[31:0]	'h00000088	00000034	00000038	00000048	00000050	00000054	0000004C
	pc_final[31:0]	'h0000008C	0000003C	00000048	0000004C	00000050	00000058	00000050
	pc_m[31:0]	'h00000088	00000030	00000034	00000038	00000048	00000050	00000054
	pc_next[31:0]	'h0000008C	0000003C	00000040	0000004C	00000050	00000058	00000050
	pc_plus_4[31:0]	'h0000008C	0000003C	00000040	0000004C	00000050	00000058	00000050
	pc_plus_4_d[31:0]	'h0000008C	00000038	0000003C	0000004C	00000050	00000058	00000050
	pc_plus_4_m[31:0]	'h0000008C	00000034	00000038	0000004C	00000050	00000054	00000058
	pc_target[31:0]	'h0000008C	0000003C	00000048	0000004C	00000050	00000058	00000050
	rd_m[4:0]	'h00	02	03	00	07	04	19
	rdata[31:0]	'h00000000	00000000					
	rdata2[31:0]	'h00000000	00000005	00000000	00000004	00000005	00000001	00000000
	rdata_data_mem[31:0]	'h00000000	00000000					

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
































Cursor = 2,843.015ps
Baseline = 0
Cursor-Baseline = 2,843.015ps

	func7[6:0]	'h0	00	7F	00	7F	00	7F	00	7F	00
	going_in_alu_a[31:0]	'h00000000	0000000A	00000002	00000000	00000002	0000000F	00000001	00000000	00000000	00
	going_in_alu_b[31:0]	'h00000000	00000005	00000001	00000000	00000005	00000005	00000001	00000000	00000000	00000000
	imm_csr_d[31:0]	'hxxxxxxxx									
	imm_csr_m[31:0]	'h00000000	FFFFFFFF	00000003	FFFFFFFF8	00000000	FFFFFFF	00000003	FFFFFFF8	00000003	FFFFFFF4
	imm_ext[31:0]	'h00000000	00000003	FFFFFFFF8	00000000	FFFFFFFF	00000003	FFFFFFFF8	00000000	FFFFFFFF4	00000000
	imm_ext_d[31:0]	'h00000000	FFFFFFFF	00000003	00000000	00000000	FFFFFFF	00000003	FFFFFFF8	00000003	FFFFFFF8
	imm_src[2:0]	'h0		2	0			2	3	0	
	inst_o[31:0]	'h0000006F	FE539CE3	FE5F06F	FFF38393	00320233	FE539CE3	FE5F06F	00100213	FE111AE3	
	instr_d[31:0]	'h00000013	00320233	FE539CE3	00000013	FFF38393	00320233	FE539CE3	FE5F06F	00000013	
	instr_m[31:0]	'h0000006F	FFF38393	00320233	FE539CE3	00000013	FFF38393	00320233	FE539CE3	FE5F06F	
	intr	0									
	is_mret	0									
	mask[3:0]	'hF									
	mask_dm[3:0]	'hF									
	mem_write	0									
	mem_write_m	0									
	opcode_d[6:0]	'h13	33	63	13		33	63	6F	13	
	opcode_ff[6:0]	'h6F	63	6F	13	33	63	6F	13	63	
	opcode_m[6:0]	'h6F		33	63	13		33	63	6F	
	pc[31:0]	'h00000088	00000050	00000058	0000004C	00000050	00000054	00000058	0000005C	0000003C	
	pc_d[31:0]	'h00000088	00000050	00000054	00000050	0000004C	00000050	00000054	00000058	00000058	
	pc_final[31:0]	'h0000008C	00000054	00000058	0000004C	00000050	00000054	00000058	0000005C	00000040	
	pc_m[31:0]	'h00000088	00000054	0000004C	00000050	00000054	0000004C	00000050	00000054	00000040	
	pc_next[31:0]	'h0000008C	00000058	0000005C	00000050	00000054	00000058	0000005C	00000054	00000058	
	pc_plus_4[31:0]	'h0000008C	00000054	00000058	0000005C	00000050	00000054	00000058	0000005C	00000040	
	pc_plus_4_d[31:0]	'h0000008C	00000050	00000054	00000058	00000050	00000054	00000058	0000005C	0000005C	
	pc_plus_4_m[31:0]	'h0000008C	00000058	00000054	00000050	00000054	00000058	0000005C	00000054	00000058	
	pc_target[31:0]	'h0000008C	00000054	00000058	0000004C	00000050	00000054	00000058	0000005C	00000040	
	rd_m[4:0]	'h00	07	04	19	00	07	04	19	00	
	rdata1[31:0]	'h00000000	00000003	0000000A	00000002	00000000	0000000F	00000001	00000000	00000000	
	rdata2[31:0]	'h00000000	00000000	00000005	00000001	00000000	00000005	00000001	00000000	00000000	
	rdata_data_mem[31:0]	'h00000000									

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

Cursor = 2,843,015ps
Baseline = 0
Cursor-Baseline = 2,843,015ps

	func7[6:0]	'h00	7F	00	7F	00	1,000,000ps	1,020,000ps	1,040,000ps	1,060,000ps	1,100,000ps	1,120,000ps	1,140,000ps	1,160,000ps
	going_in_alu_a[31:0]	'h00000000	00000004	00000000	00000000	00000000								7F
	going_in_alu_b[31:0]	'h00000000	00000002	00000000	00000000	00000014						00000003		00000000
	imm_csr_d[31:0]	'hxxxxxxxx												
	imm_csr_m[31:0]	'h00000000	FFFFFFF4	FFFFFFF4	00000000	FFFFFFFF					00000004	00000010	00000000	00000002
	imm_ext[31:0]	'h00000000	FFFFFFF4	00000000	FFFFFFFF	00000004					00000010	00000000	00000002	FFFFFFFF
	imm_ext_d[31:0]	'h00000000	FFFFFFF4	00000000	FFFFFFFF	00000004					00000004	00000000	00000002	00000000
	imm_src[2:0]	'h0	2	0	0	3					0			
	inst_o[31:0]	'h0000006F	FE111B	0280006F	FEF10113	004001B3					0100006F	FE111AE3	002003B3	00320233
	instr_d[31:0]	'h00000013	000000	FE111AE3	00000013	FEF10113					004001B3	00000013	002003B3	FFF38393
	instr_m[31:0]	'h0000006F	FE5FFB	00000013	FE111AE3	00000013					FEF10113	0000006F	00000013	002003B3
	intr	0												
	is_mret	0												
	mask[3:0]	'hF												
	mask_dm[3:0]	'hF												
	mem_write	0												
	mem_write_m	0												
	opcode_d[6:0]	'h13	63	13	13	33					6F	13	33	13
	opcode_f[6:0]	'h6F	6F	13	13	6F					63	33	13	33
	opcode_m[6:0]	'h6F	13	63	63	13					33	6F	13	33
	pc[31:0]	'h00000088	000000	00000040	00000030	00000034					0000003C	00000048	0000004C	00000050
	pc_d[31:0]	'h00000088	000000	0000003C	00000030	00000034					00000038	00000048	0000004C	00000054
	pc_final[31:0]	'h0000008C	000000	00000030	00000034	00000038					0000003C	0000004C	00000050	00000054
	pc_m[31:0]	'h00000088	00000058	0000003C	00000030	00000034					00000038	00000048	00000054	00000058
	pc_next[31:0]	'h0000008C	000000	00000044	00000034	00000038					0000003C	0000004C	00000050	00000054
	pc_plus_4[31:0]	'h0000008C	000000	00000044	00000034	00000038					0000003C	0000004C	00000050	00000054
	pc_plus_4_d[31:0]	'h0000008C	000000	00000040	00000034	00000038					0000003C	0000004C	00000050	00000054
	pc_plus_4_m[31:0]	'h0000008C	0000005C	00000040	00000034	00000038					0000003C	0000004C	00000050	00000054
	pc_target[31:0]	'h0000008C	000000	00000030	00000034	00000038					0000003C	0000004C	00000050	00000054
	rd_m[4:0]	'h00	00	15	00	02					03	00	07	07
	rdata1[31:0]	'h00000000	000000	00000004	00000000	00000004					00000000	00000004	00000008	0000000C
	rdata2[31:0]	'h00000000	000000	00000002	00000000	00000004					00000000	00000004	00000008	0000000C
	rdata_data_mem[31:0]	'h00000000	00000000											

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




























Cursor = 2,843,015ps
Baseline = 0
Cursor-Baseline = 2,843,015ps

	fnc7[6:0]	'h0	7F	00	7F	00	7F	00	7F
	going_in_alu_a[31:0]	'h00000000	00000002	00000000	00000002	00000028	00000001	00000000	00
	going_in_alu_b[31:0]	'h00000000	00000001	00000000	00000014	00000001	00000000	00000000	00
	imm_csr_d[31:0]	'xxxxxxxx	xxxxxxxx						
	imm_csr_m[31:0]	'h00000000	00000003	FFFFFFF8	00000000	FFFFFFF8	00000003	FFFFFFF8	00
	imm_ext[31:0]	'h00000000	FFFFFFF8	00000000	FFFFFFF8	00000003	FFFFFFF8	00000000	FF
	imm_ext_d[31:0]	'h00000000	00000003	00000000	FFFFFFF8	00000003	FFFFFFF8	00000000	00
	imm_src[2:0]	'h0	2	0	2	3	0	2	2
	inst_o[31:0]	'h0000006F	FE5FF06F	FFF38393	00320233	FE59CE3	FE5FF06F	00100213	FE111AE3
	instr_d[31:0]	'h00000013	FE59CE3	00000013	FFF38393	00320233	FE59CE3	FE5FF06F	00000013
	instr_m[31:0]	'h0000006F	00320233	FE59CE3	00000013	FFF38393	00320233	FE59CE3	FE5FF06F
	intr	0							
	is_mret	0							
	mask[3:0]	'hF							
	mask_dm[3:0]	'hF							
	mem_write	0							
	mem_write_m	0							
	opcode_d[6:0]	'h13	63	13	33	63	6F	13	63
	opcode_ff[6:0]	'h6F	6F	13	33	6F	13	63	6F
	opcode_m[6:0]	'h6F	33	63	13	33	63	6F	13
	pc[31:0]	'h00000088	00000054	00000058	0000004C	00000050	00000054	00000058	0000003C
	pc_d[31:0]	'h00000088	00000050	00000054	0000004C	00000050	00000054	00000058	00000000
	pc_final[31:0]	'h0000008C	00000058	0000004C	00000050	00000054	00000058	0000003C	00000040
	pc_m[31:0]	'h00000088	0000004C	00000050	00000054	0000004C	00000050	00000054	00000058
	pc_next[31:0]	'h0000008C	00000058	0000005C	00000050	00000054	00000058	00000060	00000040
	pc_plus_4[31:0]	'h0000008C	00000058	0000005C	00000050	00000054	00000058	00000060	00000040
	pc_plus_4_d[31:0]	'h0000008C	00000054	00000058	00000050	00000054	00000058	0000005C	00000000
	pc_plus_4_m[31:0]	'h0000008C	00000050	00000054	00000050	00000054	00000058	0000005C	0000005C
	pc_target[31:0]	'h0000008C	00000058	0000004C	00000050	00000054	00000058	0000003C	00000040
	rd_m[4:0]	'h0	04	19	00	07	04	19	00
	rdata1[31:0]	'h00000000	00000014	00000002	00000000	00000028	00000001	00000000	00000000
	rdata2[31:0]	'h00000000	00000014	00000001	00000000	00000014	00000001	00000000	00000000
	rdata_data_mem[31:0]	'h00000000	00000000						

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Cursor = 2,843,015ps
Baseline = 0
Cursor-Baseline = 2,843,015ps

































	func7[6:0]	'h0	00	7F	00	00	7F	00	00	7F	00
	going_in_alu_a[31:0]	'h00000000	00000003	00000000	00000003	00000000	00000000	00000002	00000002	00000002	0000003C
	going_in_alu_b[31:0]	'h00000000	00000002	00000000	00000000	00000000	00000000	00000000	00000000	00000000	0000003C
	imm_csr_d[31:0]	'hxxxxxxxx	xxxxxxx								
	imm_csr_m[31:0]	'h00000000	00000000	00000000	00000000	00000000	00000004	00000010	00000000	00000002	FFFFFFF
	imm_ext[31:0]	'h00000000	FFFFFFF4	00000000	FFFFFFF	00000004	00000010	00000000	00000002	FFFFFFF	00000003
	imm_ext_d[31:0]	'h00000000	00000000		FFFFFFF	00000004	00000004	00000000	00000002	FFFFFFF	
	imm_src[2:0]	'h0	0				3	0			
	inst_o[31:0]	'h0000006F	0280006F	FF10113	004001B3	0100006F	FE111AE3	002003B3	FFF38393	00320233	FE539CE3
	instr_d[31:0]	'h00000013	FE111AE3	00000013	004001B3	0100006F	00000013	00000013	002003B3	FFF38393	00320233
	instr_m[31:0]	'h0000006F	00000013	FE111AE3	00000013	FF10113	004001B3	0100006F	00000013	002003B3	FFF38393
	intr	0									
	is_mret	0									
	mask[3:0]	'hF	x								
	mask_dm[3:0]	'hF	x								
	mem_write	0									
	mem_write_m	0									
	opcode_d[6:0]	'h13	63	13	33	6F	13	33	13	33	33
	opcode_ff[6:0]	'h6F	6F	13	6F	63	33	13	33	63	63
	opcode_m[6:0]	'h6F	13	63	13	33	6F	13	33	13	13
	pc[31:0]	'h00000088	00000040	00000030	00000034	00000038	0000003C	00000048	0000004C	00000050	00000054
	pc_d[31:0]	'h00000088	0000003C	00000030	00000034	00000038	00000038	00000048	0000004C	00000050	00000050
	pc_final[31:0]	'h0000008C	00000030	00000034	00000038	0000003C	00000048	00000050	00000054	00000058	00000058
	pc_m[31:0]	'h00000088	00000058	0000003C	00000030	00000034	00000038	00000048	0000004C	00000050	00000054
	pc_next[31:0]	'h0000008C	00000044	00000034	00000038	0000003C	00000040	0000004C	00000050	00000054	00000058
	pc_plus_4[31:0]	'h0000008C	00000044	00000034	00000038	0000003C	00000040	0000004C	00000050	00000054	00000058
	pc_plus_4_d[31:0]	'h0000008C	00000040	00000034	00000038	0000003C	0000003C	0000004C	00000050	00000054	00000054
	pc_plus_4_m[31:0]	'h0000008C	0000005C	00000040	00000034	00000038	00000038	0000003C	0000004C	00000050	00000050
	pc_target[31:0]	'h0000008C	00000030	00000034	00000038	0000003C	00000048	0000004C	00000050	00000054	00000058
	rd_m[4:0]	'h0	00	15	00	02	03	00	07		
	rdata1[31:0]	'h00000000	00000003	00000000	00000003	00000000		0 0 0	0 0 0	0 0 0	0000003C
	rdata2[31:0]	'h00000000	00000002	00000000	0000003C	00000000	00000002	00000000	00000000	00000000	0000003C
	rdata_data_mem[31:0]	'h00000000	00000000								

Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core

Cursor = 2,843,015ps
Baseline = 0

Cursor-Baseline = 2,843,015ps

	func7[6:0]	*h0	00	1,840,000ps	1,860,000ps	1,880,000ps	1,900,000ps	1,920,000ps	1,940,000ps	1,960,000ps	1,980,000ps
	going_in_alu_a[31:0]	*h00000000	00000000								
	going_in_alu_b[31:0]	*h00000000	00000000								
	imm_csr_d[31:0]	*hxxxxxxxx	xxxxxxxx								
	imm_csr_m[31:0]	*h00000000	00000000								
	imm_ext[31:0]	*h00000000	00000000								
	imm_ext_d[31:0]	*h0	0	3	0	3	0	3	0	3	0
	inst_o[31:0]	*h0000006F	0000006F	00800B13	0000006F	00800B13	0000006F	00800B13	0000006F	00800B13	0000006F
	instr_d[31:0]	*h00000013	00000013	0000006F	00000013	0000006F	00000013	0000006F	00000013	0000006F	00000013
	instr_m[31:0]	*h0000006F	0000006F	00000013	0000006F	00000013	0000006F	00000013	0000006F	00000013	0000006F
	intr	0									
	is_mret	0									
	mask[3:0]	*hF	F								
	mask_dm[3:0]	*hF	F								
	mem_write	0									
	mem_write_m	0									
	opcode_d[6:0]	*h13	13	6F	13	6F	13	6F	13	6F	13
	opcode_ff[6:0]	*h6F	6F	13	6F	13	6F	13	6F	13	6F
	opcode_m[6:0]	*h6F	6F	13	6F	13	6F	13	6F	13	6F
	pc[31:0]	*h00000088	00000088	0000008C	00000088	00000088	0000008C	00000088	0000008C	00000088	00000088
	pc_d[31:0]	*h00000088	00000088								
	pc_final[31:0]	*h0000008C	0000008C	00000088	0000008C	00000088	0000008C	00000088	0000008C	00000088	0000008C
	pc_m[31:0]	*h00000088	00000088								
	pc_next[31:0]	*h0000008C	0000008C	00000090	0000008C	00000090	0000008C	00000090	0000008C	00000090	0000008C
	pc_plus_4[31:0]	*h0000008C	0000008C	00000090	0000008C	00000090	0000008C	00000090	0000008C	00000090	0000008C
	pc_plus_4_d[31:0]	*h0000008C	0000008C								
	pc_plus_4_m[31:0]	*h0000008C	0000008C								
	pc_target[31:0]	*h0000008C	0000008C	00000088	0000008C	00000088	0000008C	00000088	0000008C	00000088	0000008C
	rd_m[4:0]	*h0	00								
	rdata1[31:0]	*h00000000	00000000								
	rdata2[31:0]	*h00000000	00000000								
	rdata_data_mem[31:0]	*h00000000	00000000	00000078	00000000	00000078	00000000	00000078	00000000	00000078	00000000

Computer Architecture

Ahsan Ali (2019-EE-115)

UET

3 stage pipelined RISC-V Core

Cursor = 2,843,015ps

Baseline = 0

Cursor-Baseline = 2,843,015ps

[illegible]

Computer Architecture

Ahsan Ali (2019-EE-115)

UET

3 stage pipelined RISC-V Core

Cursor = 2,843,015ps

Baseline = 0

Cursor-Baseline = 2,843,015ps

[illegible]

Computer Architecture

Ahsan Ali (2019-EE-115)

UET

3 stage pipelined RISC-V Core

Cursor = 2,843,015ps

Baseline = 0

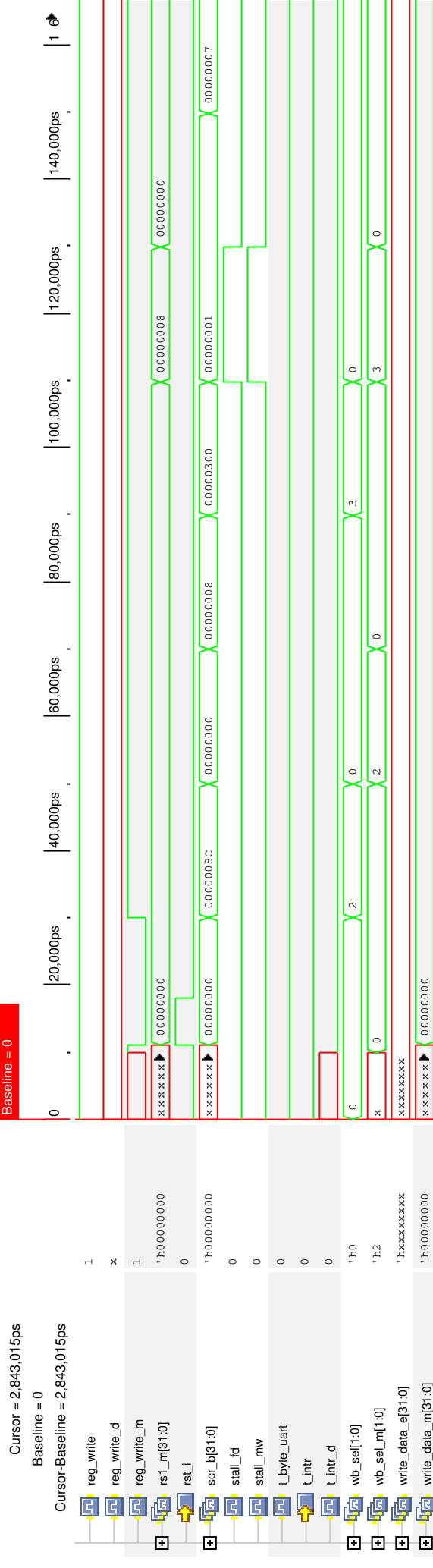
Cursor-Baseline = 2,843,015ps

[illegible]

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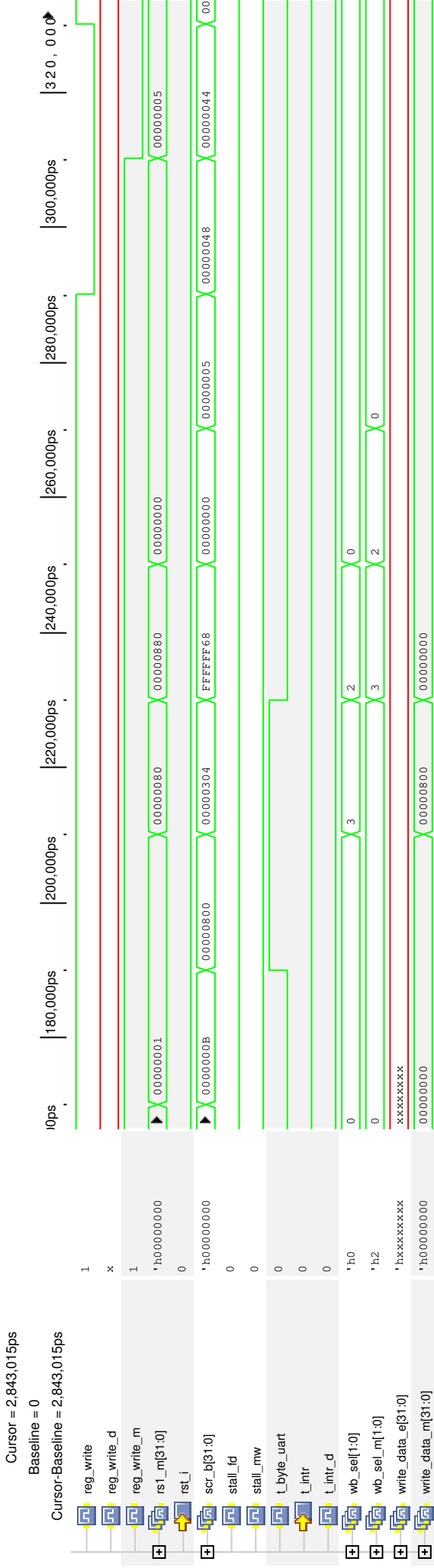
UET

3 stage pipelined RISC-V Core



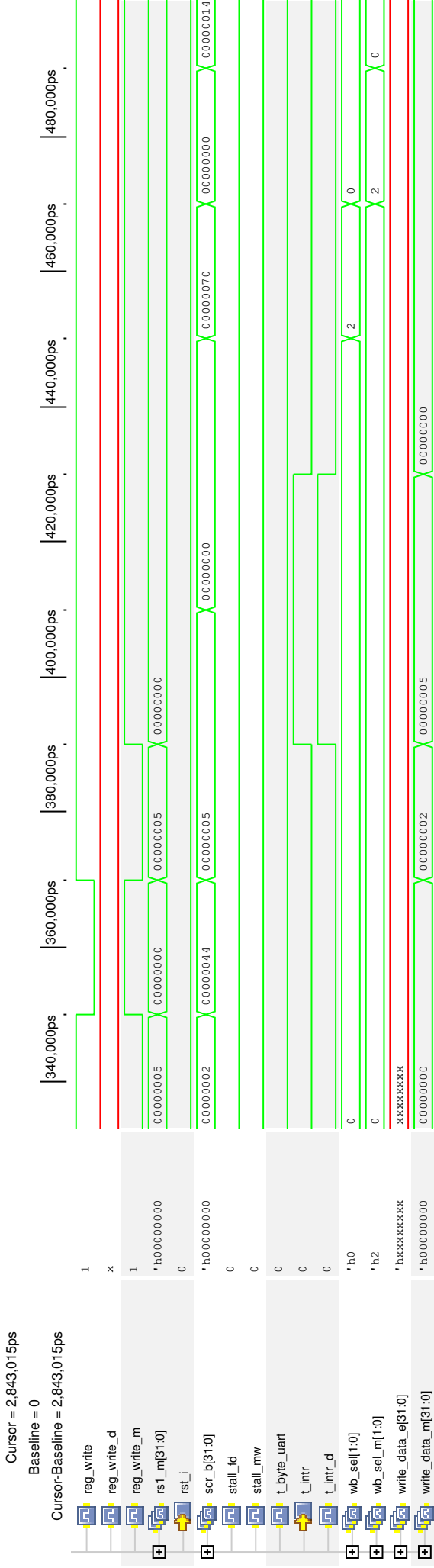
Computer Architecture

Ahsan Ali (2019-EE-115)
UET
3 stage pipelined RISC-V Core



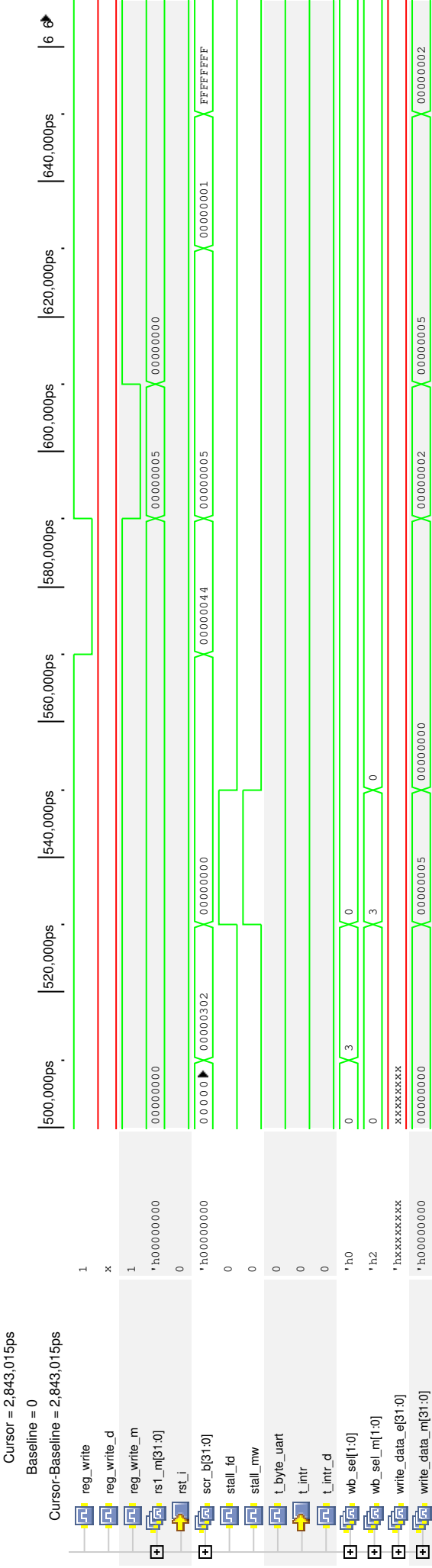
Computer Architecture

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3 stage pipelined RISC-V Core



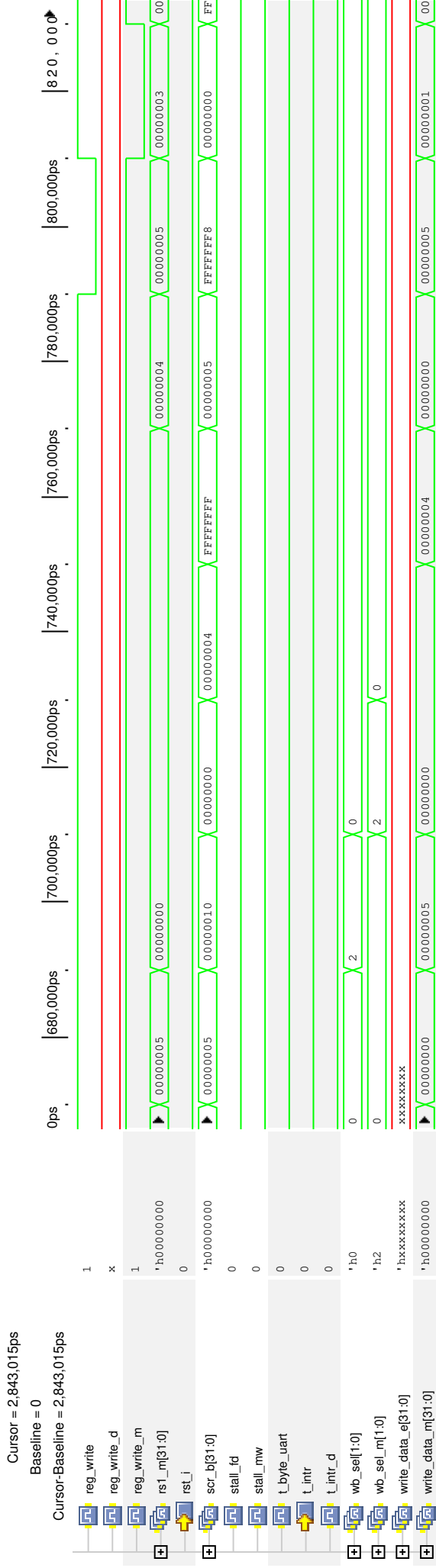
Computer Architecture

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3 stage pipelined RISC-V Core



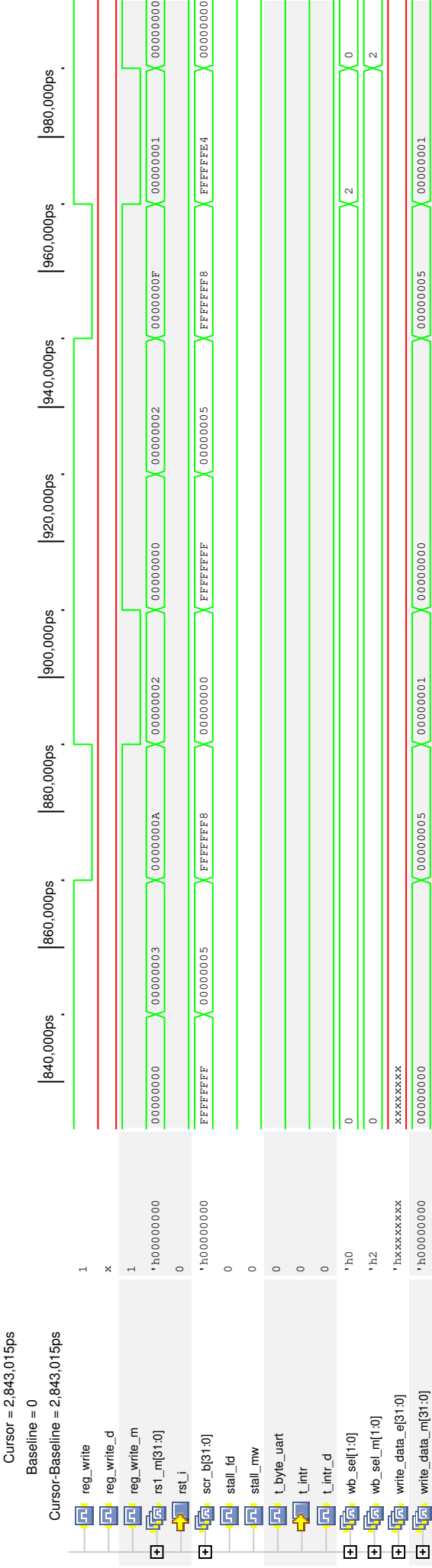
Computer Architecture

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3 stage pipelined RISC-V Core



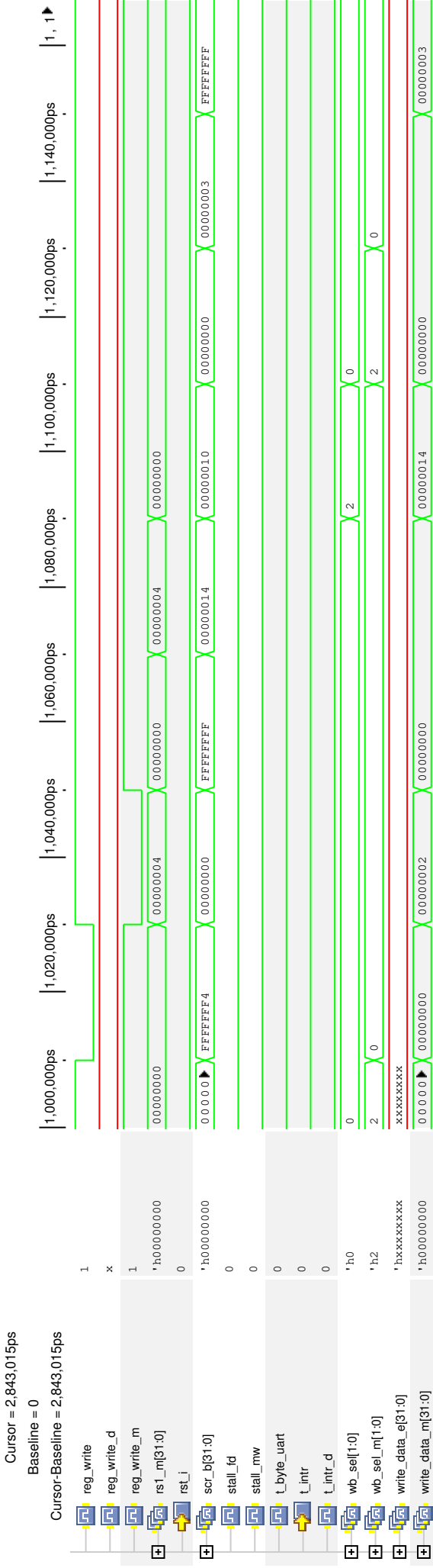
Computer Architecture

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3 stage pipelined RISC-V Core



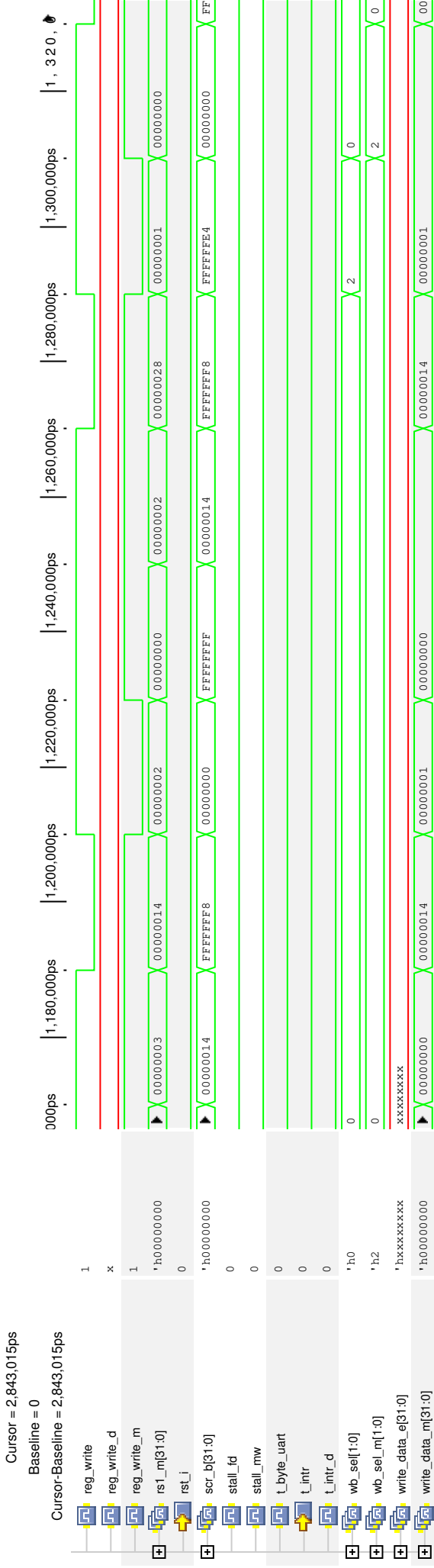
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Computer Architecture

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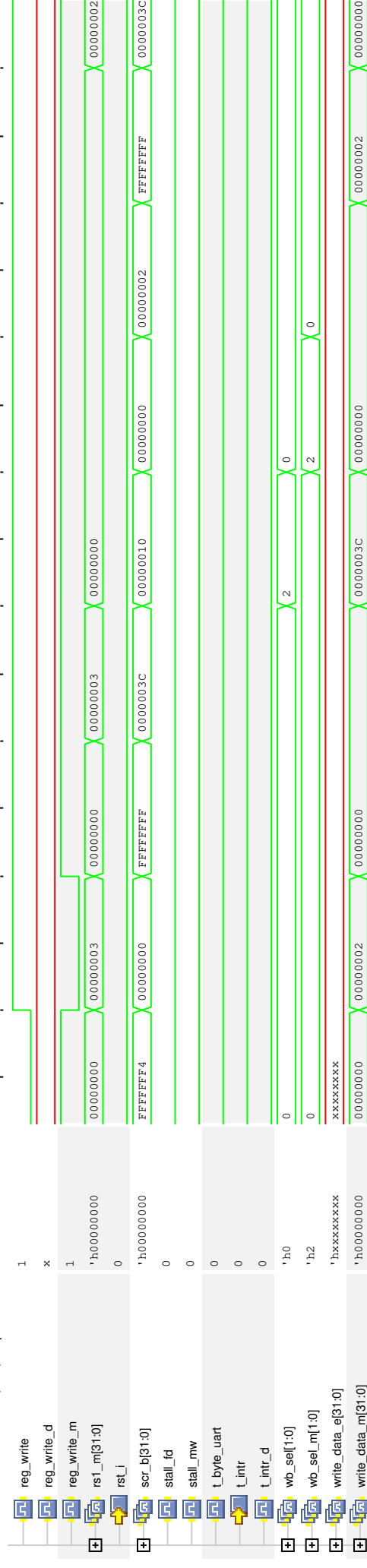
UET

3 stage pipelined RISC-V Core

Cursor = 2,843,015ps

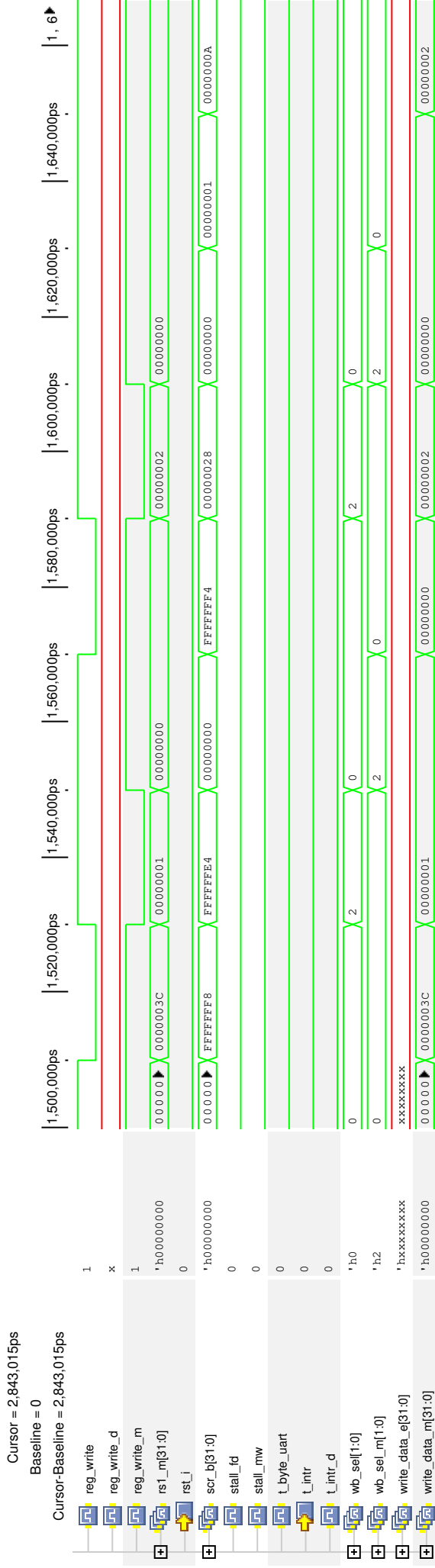
Baseline = 0

Cursor-Baseline = 2,843,015ps



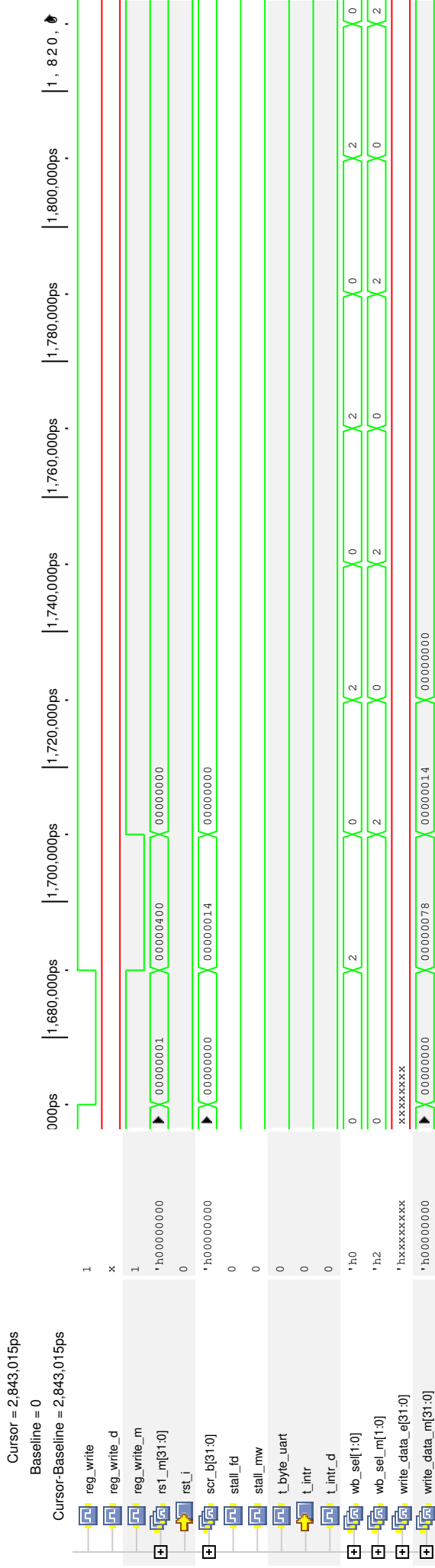
Computer Architecture

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UET
3 stage pipelined RISC-V Core



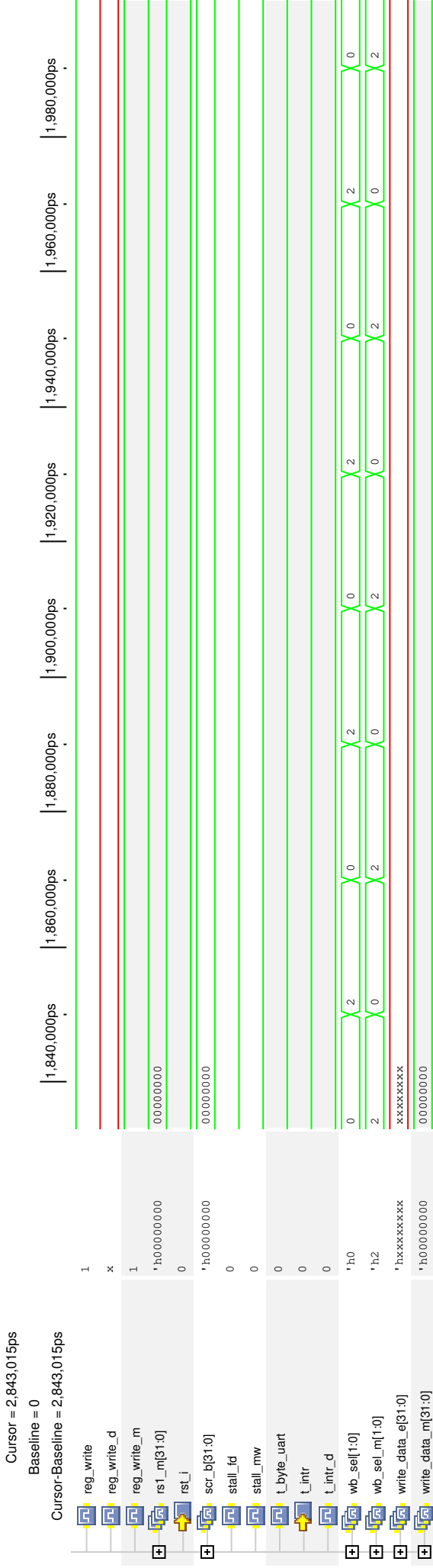
Computer Architecture

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3 stage pipelined RISC-V Core

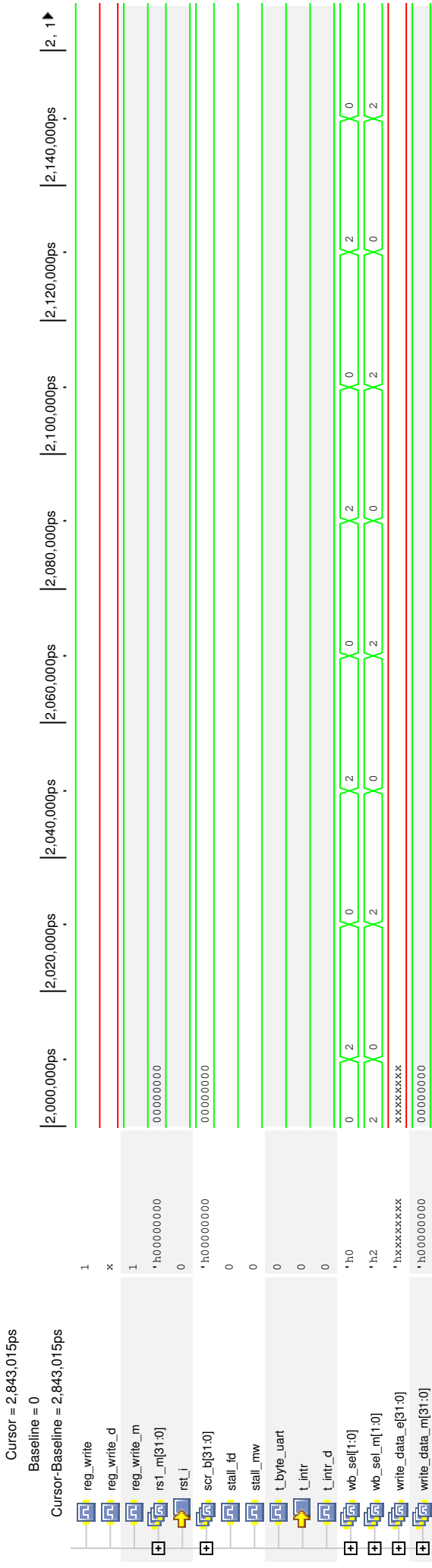


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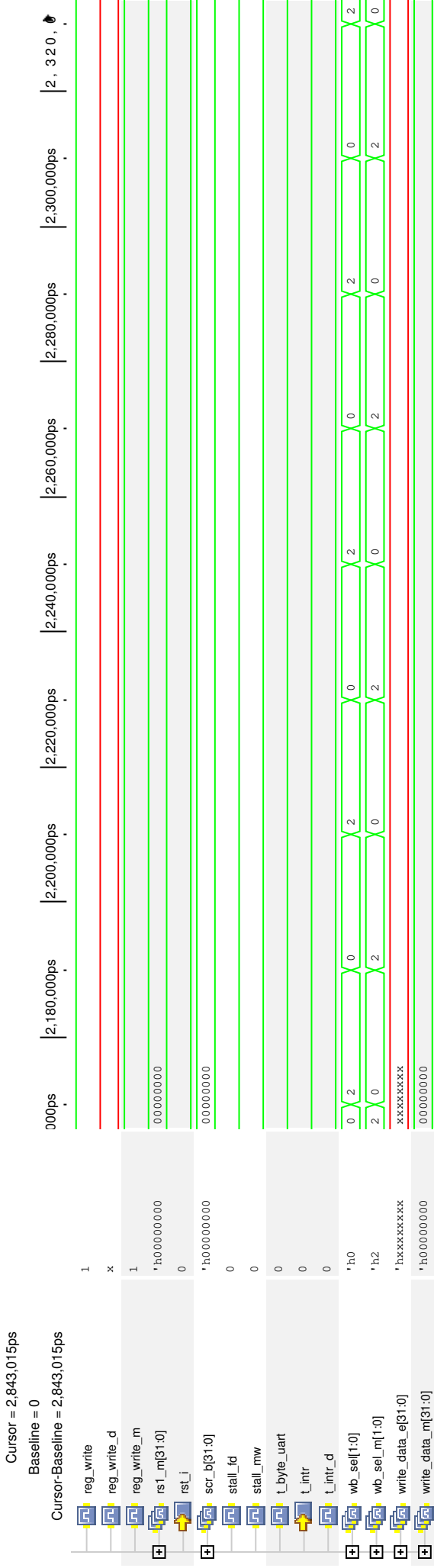
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3 stage pipelined RISC-V Core



Computer Architecture

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Computer Architecture

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