1. Always use forward slashes (**/**) while giving address of some file in **QuestaSim.** Just like in the example below:



1. This error occurs when you do not add a Verilog file in QuestaSim. Also make sure that the file is properly referenced (Instantiated) in the main file.

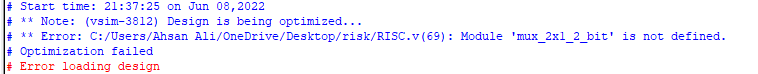


Figure 1: Some error.

1. Make your reset signal high until first edge (either positive or negative) of the clock then make it zero just like the diagram below:



Figure 2: Clock and reset settings.

And not like the following one:



Figure 3: Not recommended.

The reason to avoid it is that the program counter (PC) is changed/incremented as the edge of the clock, it should face at least one cycle before it is reset (This does not make sense because reset is asynchronous). This is just a matter of experience. Results may come true in 2nd case at your side. But 1st practice is recommended.

1. Avoid using x (don’t care) in your Verilog code. Use OR operation instead (either 1 or 0).