Bahria University
Discovering Knowledge

BAHRIA UNIVERSITY,
(Karachi Campus)
Department of Software Engineering
ASSIGNMENT #. 01 – Spring 2023

Course Title: **Operating Systems**		Course Code:	**CSC-320**
Class: **BSE - 4(A & B)**		Shift:	**Morning**
Course Instructor: **Engr. Rizwan Fazal**		Date:	**27-March-2023**
Due Date: **16-APRIL-2023 (11:55 PM)**		Max. Marks:	**20 Points**

ASSIGNMENT #. 1

Submitted by:

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Registration #: 79309

Section: 4B

Date

NAME :- Ahsan Sajjad
SECTION :- BSE-4B
COURSE: Operating System
ASSIGNMENT: NO 01
ENROLLMENT NO :- 02-131212-049

1.3

Question....

(a) What is the maximum directly addressable memory Capacity.

Here the given microprocessor is 64 bit thats why it can addres a maximum memory location of 2^{64}. The max directly addressable memory capacity is depend only on the size of operand. If it has 8 byte then the maximum Directly addressable memory Capacity is approximatly 256 terabyte.

(b) What ideal size of microprocenor addres buses should be used? How will System Speed be affected for data buses of 64 bits, 32 bits and 16 bits.

The transfer of full instructions with different data buses bits are given

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bits	cycles
64	Single Cycle without any additional clock cycle
32	two(2) cycle. for 64 bit instruction
16	Four (4) Cycle for 64 bit instruction.

(c) How many bits should the instruction Register Contain if th instruction register is to Contain only The opcode, and how many if the instruction register is to. Contain the whole instruction?

It can Contain at least four byter If the Instruction Register is to Contain only. opcode.
but Instruction Register can Contain 64 bits if the IR Can Contain whole instruction.

Question.... 1.4

(a) What is the maximum meory addren. Space that the procenor can accen. directly if it is connected to a. 16 bit memory.

It Can address upto two power. 16 ~~bit~~ a memory address space. which is

2^{16}.

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b) What is the maximum Address Space that the processor can access directly if it is Connected to an 8 bit memory?

The processor can only Read or Write 8 bits of data among from each of the memory location. It means that if he required to access a 16 bit word it will need to perform two different memor accesses, two iterations. Because it is 8 bit wide meony.
Thats why it can address 2^{16} memory locations.

(c) What Architectural features will allow this microprosser to access a separate I/O Space?

The architectural features will allow this microprocessor to accen a Separte I/O Space is achieved through memory mapped I/O, I/O mapped I/O and dedicated I/O Instruction.

(d) If an I/O instruction can Specify an 8 bit I/O port, number how many 8 bit I/O Space can the microprocessor Support? How many 16 bit I/O ports?
Explain?

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If processor can specify an 8 bit I/O port number then it can support upto 2^8 ports of I/O. which represent values from 0-255.

where if the processor can specify an 16 bit register I/O process then here require 2^{16} by supporting of. "65,536" I/O ports.

1.5

Maximum 4 bytes bus cycle per second. can executed by the processor which can transferred upto 16 bytes per second across its 32 bit external data bus. For Improving its performance the external data bus. should be 64 bit to transfer upto. 32 byte per second.

Double the external clock frequency alone. would not increase the data transfer. rate per bus cycle, which remain at 4 byte.

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1.6.

+ Describe how the CPU, using the first four registers listed in this problem can achive I/O with the Teletype.

answer:-

(a) To input and output characters with the teletype, the CPU check if a character is received using the input flag, reads it if it has, proces it, sets the output register for printing the character, wrote it to the printer, and sets the output flag. An I/O module interfaces with the teletype to the input flag and output flag and the interrupt enable bit allow to the CPU which reply immediately to new characters received or to output character.

(b) Describe how the function can be more performed efficiently by also employing IEN.

The IEN allow the CPU to be interrupted by the I/O module when the ~~Cp~~ input or output operation is completed. This mean that CPU can do other tasks while waiting for I/O operations to complete and the I/O module can signal the CPU when it is done. using IEN improves efficiency and allows multitasking.