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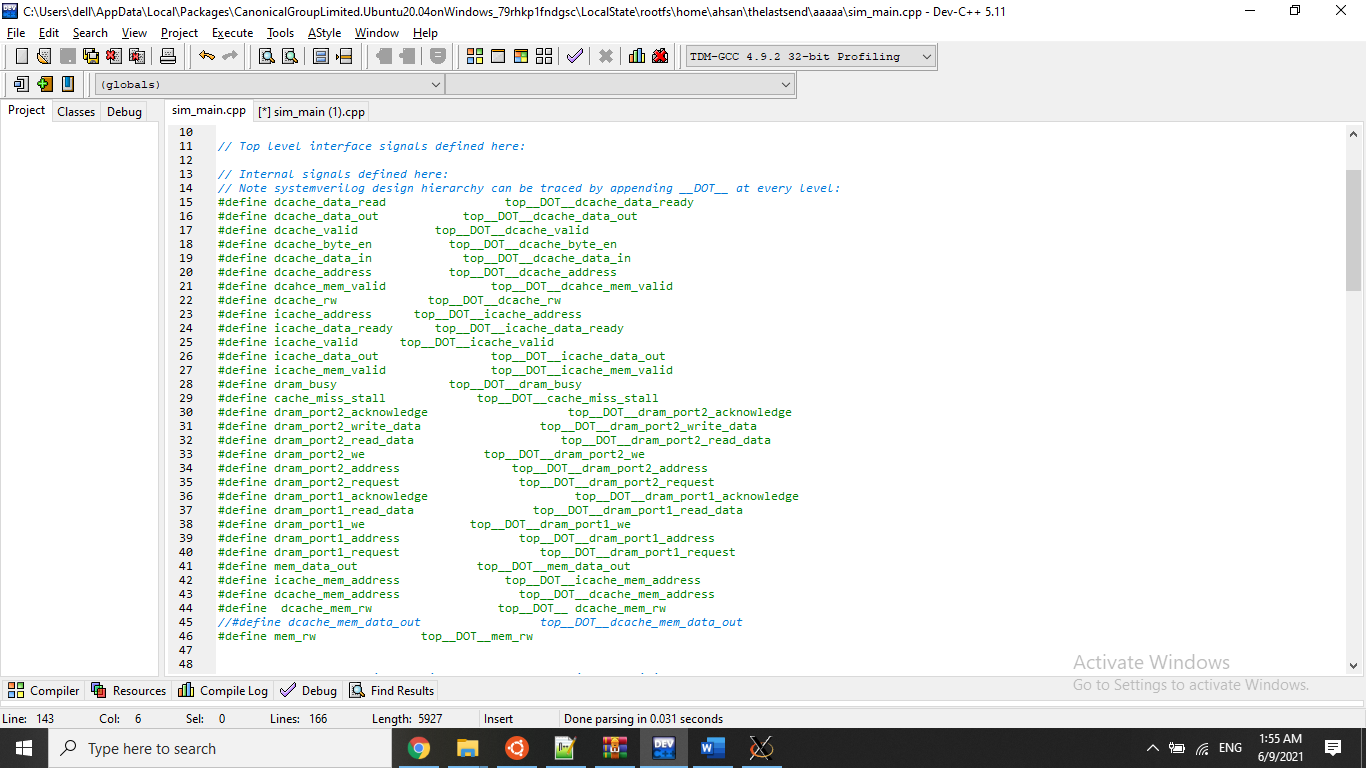
# Lab 4 Report

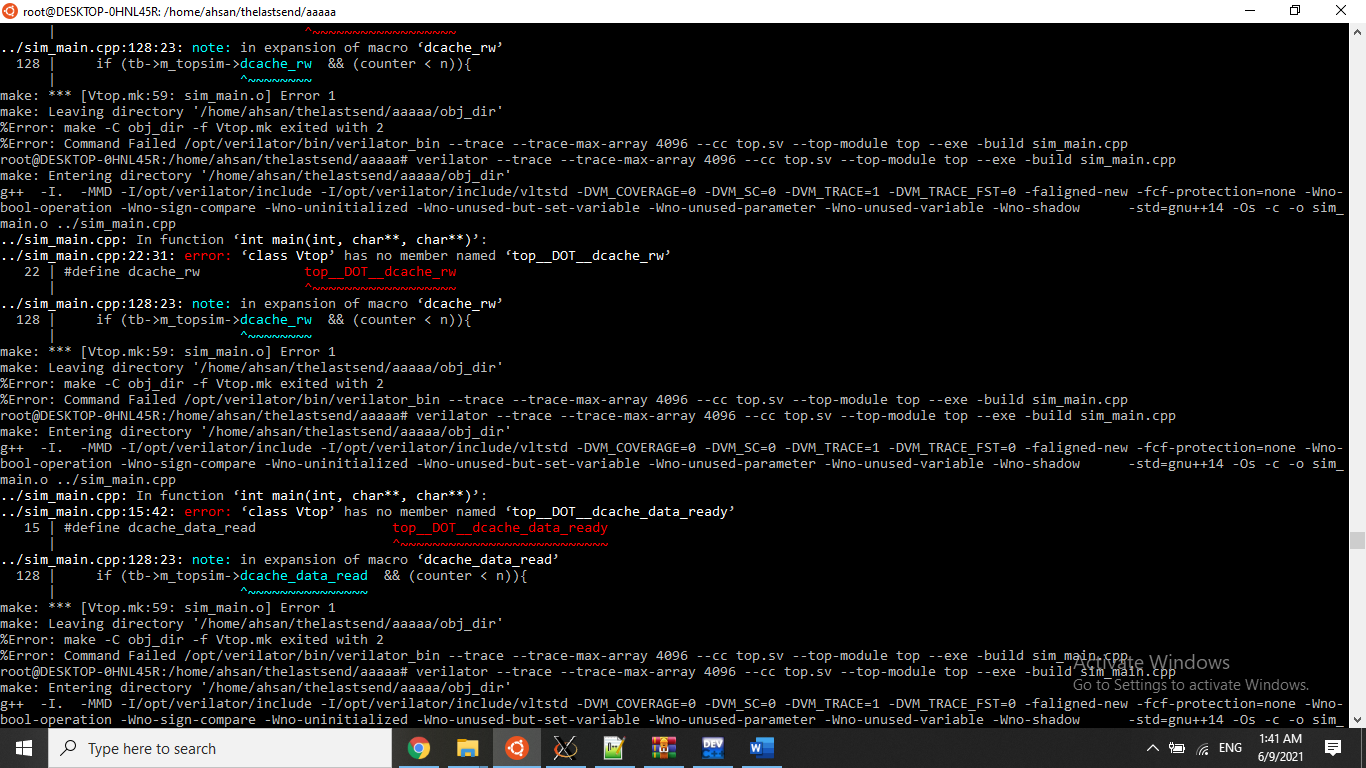
As said in the Demo, to complete the report since we had a functional CPU with integrated memory hierarchy. Unfortunately, due to issues arising in the Verilator part, I could not provide useful results. Before submitting the report on Monday, we had the Verilator for the CPU with the required parameters calculated for without the Memory Hierarchy, however we could prepare the Verilator code for Debugging with the Memory Hierarchy, due to the errors mentioned in Appendix A of this report.

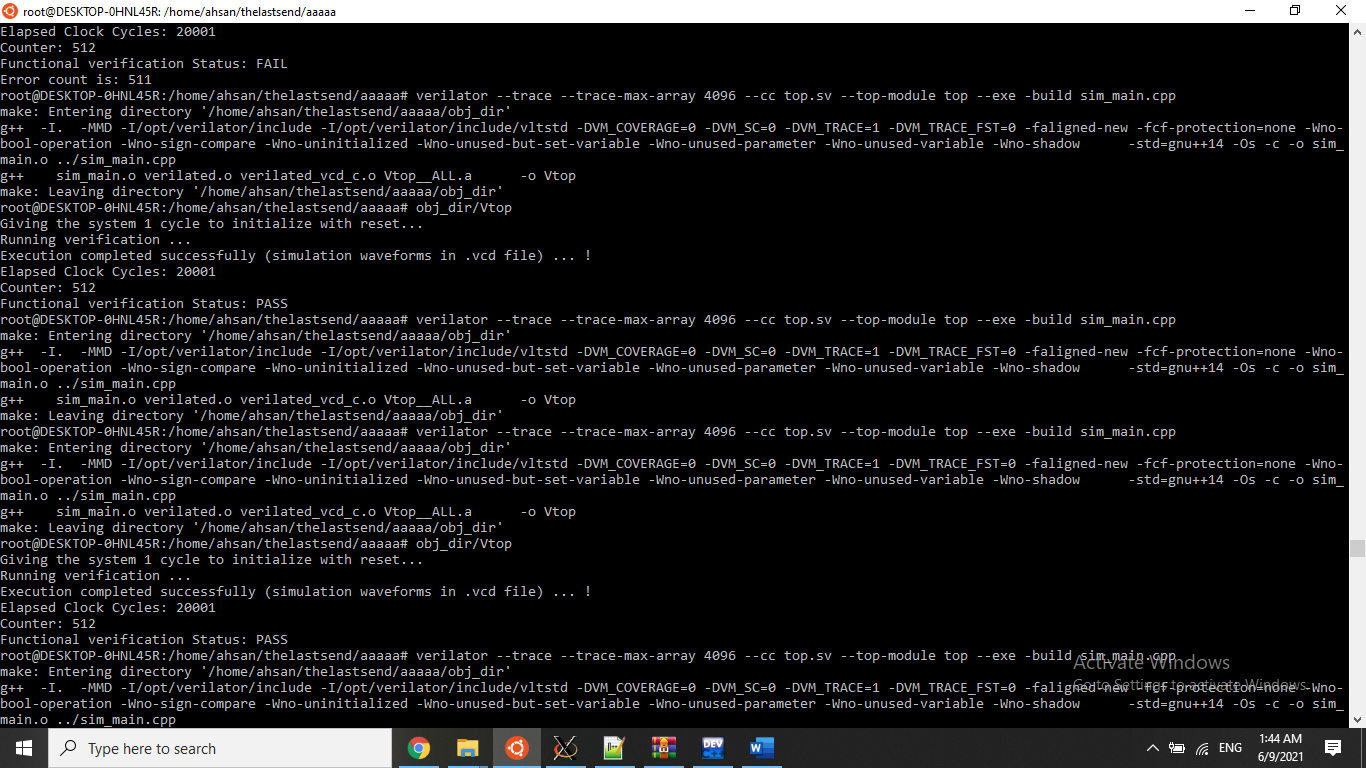
For some reason, even though in our top module we have initialized the parameters, but Verilator is not picking them up, therefore we could not calculate the parameters for functional verification.

Writing back to the DRAM is working now, however it is writing just the “first word” of block instead of writing the whole block to the DRAM.

# Appendix A

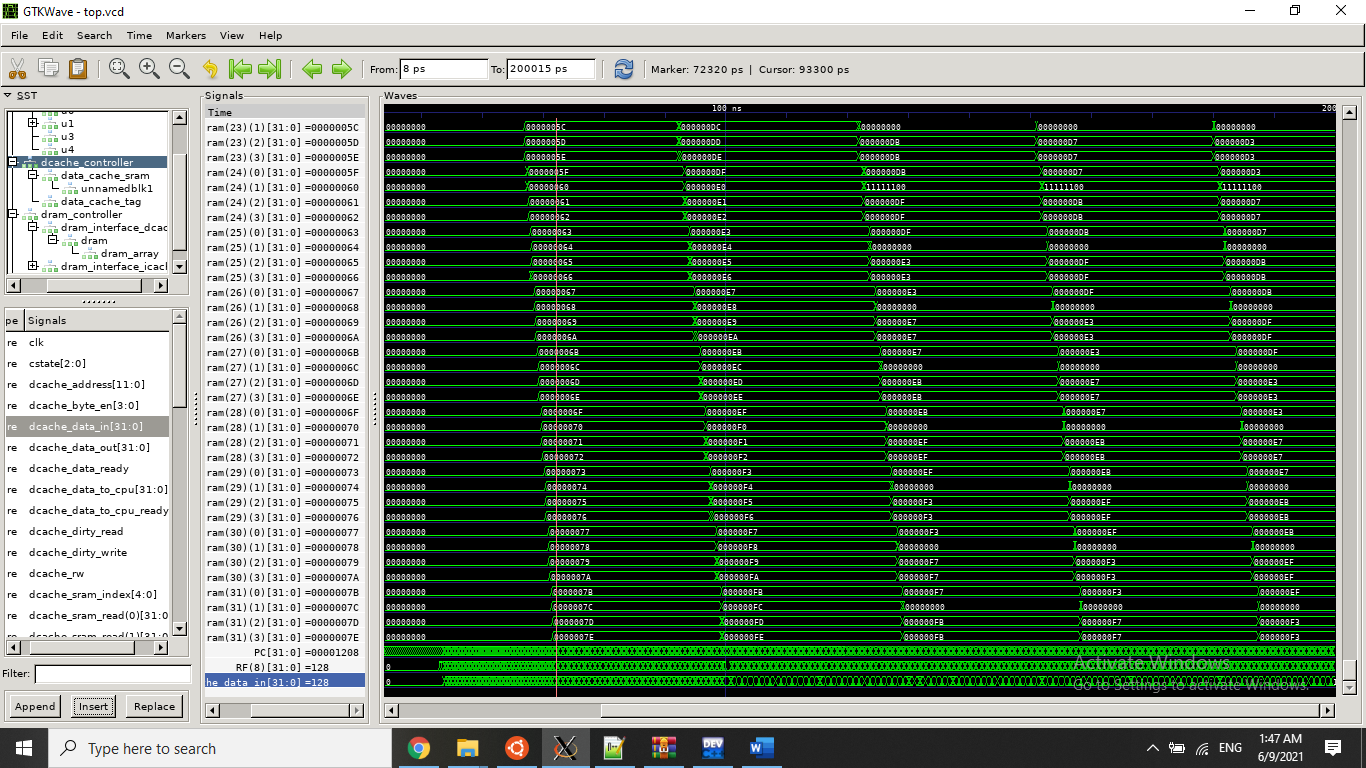






Without proper debugging, Verilator can generate the vcd file. It is used to show the GTKWave simulation to show the DRAM problem of not writing the whole block from the Data Cache below:

The SRAM at counter 128, all blocks are filled (Write back to DRAM starts) :



Write back to DRAM (at counter 128):

