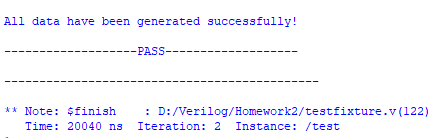
HOMEWORK 2

Student ID: P76087081 Name: Tran Thi Ai

**Description of your circuit:**

(Please describe the function and dataflow of the circuit.)



This is my result.

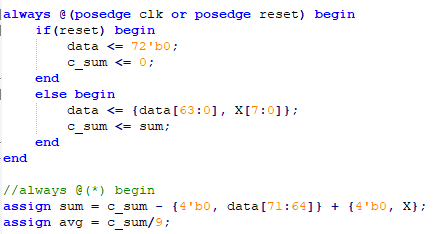
In order to calculate Y, this circuit is in after checking, the calculation of Yi is started. However, at the time point after checking, 9 numbers are stored in Register File and implement calculation sum. The steps are as follows:

Step 1: At this stage, the Sum value in the Register Sum is read out and subtracted from the Xi-9 in the Register File and then waits for the next stage Xi value to enter. The input X is changed to the next at the negative edges of the clock.

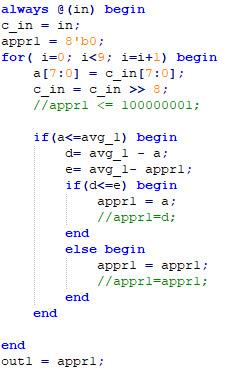
Step 2: Xi value waits outside the Register File for clock positive edge trigger to prepare to write to Register File.

After Sum i-1 and Xi-9 are subtracted add Xi to Xi-8 ~ Xi sum value Sum i and wait for clock positive edge trigger outside Register Sum to prepare to write Register Sum.

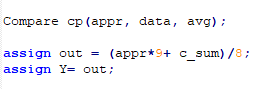
The sum value is calculated by a dividing circuit.



The Compare is a circuit compares the numbers with avg and out1 is records the respective comparison results. Which largest number in the numbers less than or equal to average number.



Finally divide by 8 to be Y.



**Lesson learn**

(Please write down the experience of completing this assignment, what you learned, and the points of difficulty.)

Though this homework, I could learn more commands and the difference between = and <= in verilog, it helps me understand than about commands and use testbench better. Beside I learned how to use sub-module in order to solve the problems easy than. Especial, I improve my skill using ModelSim software.

I am still not proficient in using sub-module. I need to interested in focus of each commands. Therefore, I had many difficulties in implementing it.