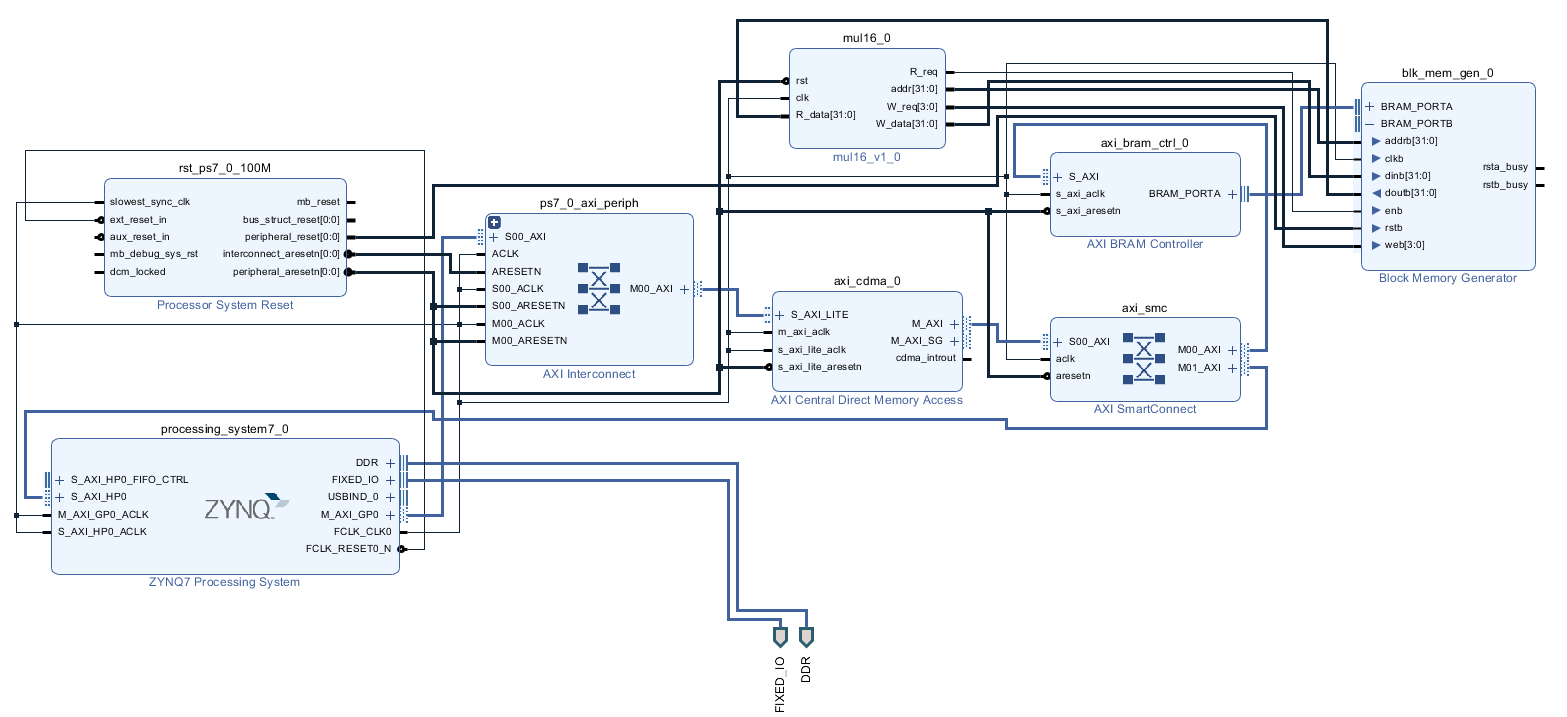
HOMEWORK 4

Student ID: P76087081 Name: Tran Thi Ai

**Block design Screenshot:**

(Please attach a screenshot and describe the block design function.)

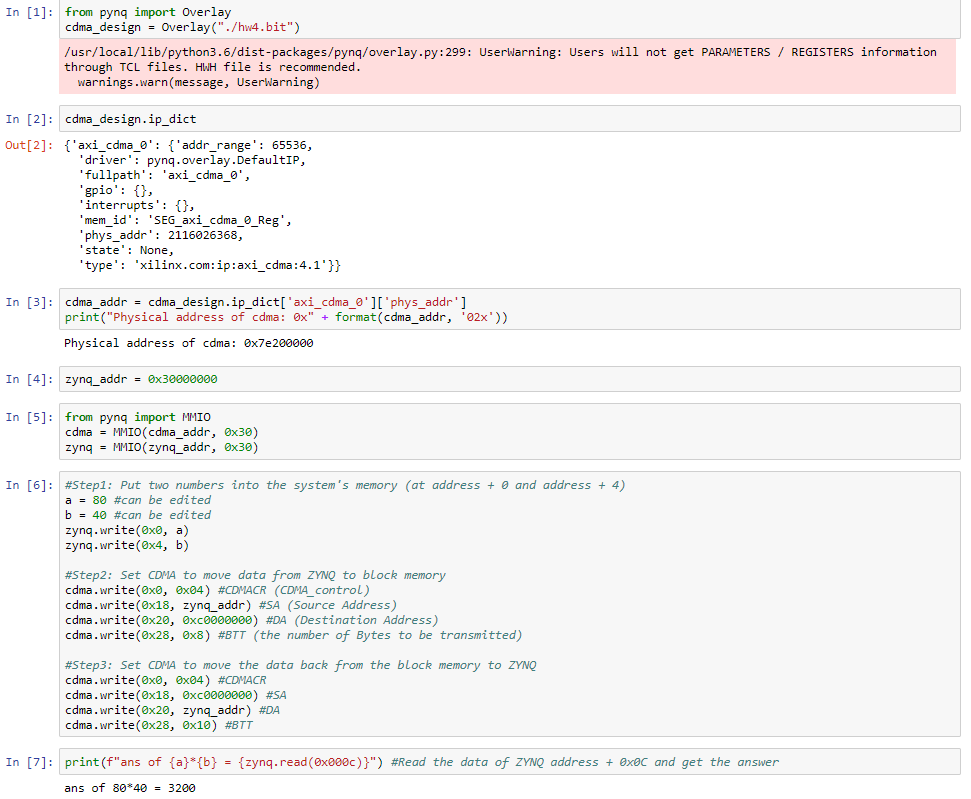


This is the block design.

This system transfers data from CDMA to Block memory. After the hardware is calculated, the data is moved back to ZYNQ by CDMA. This operation provides mul16.v. AXI bram controller mainly transfers the block memory read/write signal to AXI format, so that block memory can communicate with AXI BUS. Take ZYNQ as master and CDMA as slave, transmit control data through AXI BUS, tell CDMA where to send it. Use CDMA as master, ZYNQ and block memory as slave to transfer data. Mul16 read the block memory address 0x00 and 0x04 data, multiply it into 0x0C so read the block memory 0x0C. The mul16 clk and other ip aclk pins can be connected to the same clk signal, rst is triggered by the negative edge, and other ips can be connected to the process\_reset of the Process System Reset.

**Jupyter python code:**

(Please describe the function and execution flow of the jupyter python code.)



The first we put the two numbers into the system’s memory. After that we set cdma to move data from ZYNQ to block memory. Start cdma by writing CDMA\_control to 0x04, write Source Address to the address where ZYNQ has just written data. Write Destination Address to the address of axi\_bram, write BTT to the number of Bytes to be transmitted which can not be less than 8 because at least two words of data must be transferred. Then we set CDMA to move the data back from the block memory to ZYNQ. Start cdma writing CDMA\_control to 0x04, write Source Address to the address of axi\_bram, write Destination Address of the address of ZYNQ. Write BTT to the number of Bytes to be transmitted, which cannot be less than 16, because at least 4 words of data must be transferred. After writing cdma\_BTT, CDMA will start transmitting.

**Lesson learn**

(Please write down the experience of completing this assignment, what you learned, and the points of difficulty.)

Through this homework, I learned how to use the AXI Central Direct Memory Access to transfer data between the Block Memory and the ZYNQ CPU.

The difficulty point I encountered was that it is hard to build the system. Fortunately, I was finding the way myself through watching some guided video on Youtube.