2020 Digital IC Design Homework 3: Approximate Average

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	132264 (ns)

(your pre-sim result)

```
# ------------------------------------------------
#
# ------------------------------------------------
#
# All data have been generated successfully!
#
# -------------------PASS--------------------
#
# ------------------------------------------------
#
# ** Note: $finish    : D:/13_Digital_IC_Design/DIC_
#    Time: 200400 ns  Iteration: 2  Instance: /test
```

(your post-sim result)

```
VSIM 36> run -all
# ------------------------------------------------
#
# ------------------------------------------------
#
# All data have been generated successfully!
#
# -------------------PASS--------------------
#
# ------------------------------------------------
#
# ** Note: $finish    : D:/13_Digital_IC_Design/DIC_HW3,
#    Time: 132264 ns  Iteration: 2  Instance: /test
```

Synthesis Result

Total logic elements	515 / 68,416 (< 1 %)
Total memory bit	0 / 1,152,000 (0 %)
Embedded multiplier 9-bit element	0 / 300 (0 %)

(your flow summary)

Flow Summary

Flow Status	Successful - Thu Apr 23 13:59:11 2020
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	CS
Top-level Entity Name	CS
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	515 / 68,416 (< 1 %)
Total combinational functions	515 / 68,416 (< 1 %)
Dedicated logic registers	84 / 68,416 (< 1 %)
Total registers	84
Total pins	20 / 622 (3 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

In order to calculate Y, this circuit is in after checking, the calculation of Yi is started. However, at the time point after checking, 9 numbers are stored in Register File and implement calculation sum. The steps are as follows:

Step 1: At this stage, the Sum value in the Register Sum is read out and subtracted from the Xi-9 in the Register File and then waits for the next stage Xi value to enter. The input X is changed to the next at the negative edges of the clock.

Step 2: Xi value waits outside the Register File for clock positive edge trigger to prepare to write to Register File.

After Sum i-1 and Xi-9 are subtracted add Xi to Xi-8 ~ Xi sum value Sum i and wait for clock positive edge trigger outside Register Sum to prepare to write Register Sum.

The sum value is calculated by a dividing circuit.

The Compare is a circuit compares the numbers with avg and out1 is records the respective comparison results. Which largest number in the numbers less than or equal to average number.

```
always @(in) begin
c_in = in;
apprl = 8'b0;
for( i=0; i<9; i=i+1) begin
    a[7:0] = c_in[7:0];
    c_in = c_in >> 8;
    //apprl <= 100000001;

    if(a<=avg_1) begin
        d= avg_1 - a;
        e= avg_1- apprl;
        if(d<=e) begin
            apprl = a;
            //apprl=d;
        end
        else begin
            apprl = apprl;
            //apprl=apprl;
        end
    end

end
out1 = apprl;
```

Finally divide by 8 to be Y.

```
`timescale 1ns/10ps
`define CYCLE  66           // Modify your clock period here

`define INFILE "in.dat"
`define OUTFILE "out_golden.dat"
```

This is the clock cycle modified when post-sim.

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*