2020 Digital IC Design Homework 1: 4-bit binary adder-subtractor

NAME	Tran Thi Ai
Student ID	P76087081

Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	9316 (ns)

(your pre-sim result)

```
#         502 data is correct
#         503 data is correct
#         504 data is correct
#         505 data is correct
#         506 data is correct
#         507 data is correct
#         508 data is correct
#         509 data is correct
#         510 data is correct
#         511 data is correct
#         512 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
# ** Note: $finish    : D:/13_Digital_IC_Design/DIC_HW1/AS_tb.v(63)
```

(your post-sim result)

```
#         502 data is correct
#         503 data is correct
#         504 data is correct
#         505 data is correct
#         506 data is correct
#         507 data is correct
#         508 data is correct
#         509 data is correct
#         510 data is correct
#         511 data is correct
#         512 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
# ** Note: $finish    : D:/13_Digital_IC_Design/DIC_HW1/modlu/AS_tb.v(63)
#    Time: 9316 ns  Iteration: 0  Instance: /AS_tb
```

Synthesis Result

Total logic elements	8 / 68,416 (< 1 %)
Total memory bit	0 / 1,152,000 (0 %)
Embedded multiplier 9-bit element	0 / 300 (0 %)

(your flow s

Flow Summary

Flow Status	Successful - Sat Apr 11 18:39:50 2020
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	AS
Top-level Entity Name	AS
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	8 / 68,416 (< 1 %)
Total combinational functions	8 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	14 / 622 (2 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

In my design, I use structural description to design 4-bit binary adder-subtractor. The first, I design a full adder and then I design 4-bit binary adder-subtractor. The operations of both addition and subtraction can be performed by a one common binary adder. Such binary circuit can be designed by adding an XOR gate with each full adder. Lets consider the 4-bit parallel binary adder/subtractor which has two 4-bit inputs as A3A2A1A0 and B3B2B1B0. The circuit consists of 4 full adders since we are performing operation on 4-bit numbers. The mode input control line sel is connected with carry input of the least significant bit of the full adder. This control line decides the type of operation, whether addition or subtraction. The first full adder has control line directly as its input, the input A0 is directly input in the full

adder. The third input is the XOR of B0 and sel. The two outputs produced are S0 and C1.

When sel = 1, the circuit is a subtractor and when sel = 0, the circuit becomes adder. The Ex-OR gate consists of two inputs to which one is connected to the B and other to input sel.

A1, A2, A3 are direct inputs to the second, third and fourth full adders. Then the third input is the B1, B2, B3 Ex-OR with sel to the second, third and fourth full adder respectively. Finally, we create an Ex-OR with the inputs C3 and C4, the output is Overflow.

```
`timescale 10ns / 1ps
`define CYCLE 1.8
`define A_dat "./A.txt"
`define B_dat "./B.txt"
`define O_dat "./O.txt"
`define SUM_dat "./SUM.txt"
module AS_tb;
```

This is the clock cycle modified when post-sim

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*