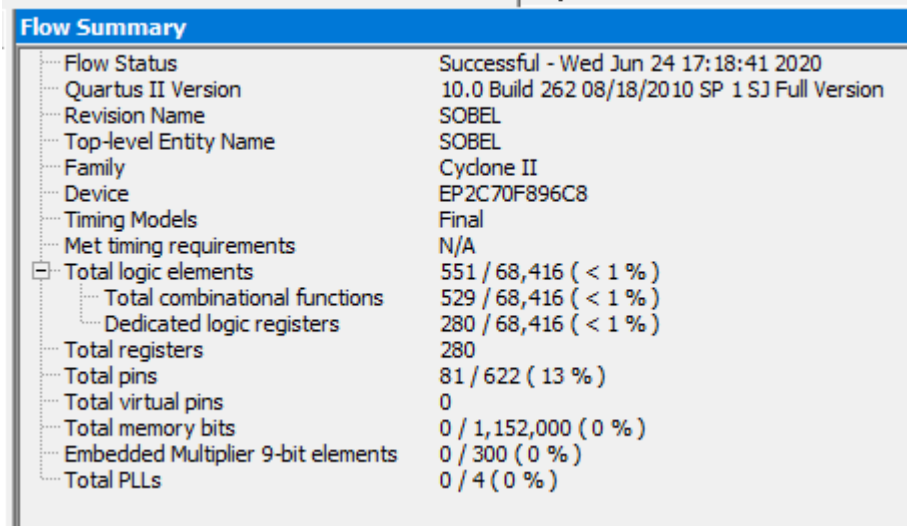


2020 Digital IC Design Homework 5: Sobel

NAME	Tran Thi Ai				
Student ID	P76087081				
Simulation Result					
Functional simulation	Level A	Gate-level simulation	Level A	Gate-level simulation time	27739457491 ps
(your pre-sim result)			(your post-sim result)		
<pre>Sobel X is correct ! Sobel Y is correct ! Sobel combine is correct ! ----- SUMMARY ----- Congratulations! Sobel X data have been generated successfully! The result is PASS!! Congratulations! Sobel Y data have been generated successfully! The result is PASS!! Congratulations! Sobel combine data have been generated successfully! The result is PASS!! ** Note: \$finish : D:/13_Digital_IC_Design/hw5/Ai/model1/testfixture.v(198) Time: 18492980 ns Iteration: 0 Instance: /testfixture</pre>			<pre>Sobel X is correct ! Sobel Y is correct ! Sobel combine is correct ! ----- SUMMARY ----- Congratulations! Sobel X data have been generated successfully! The result is PASS!! Congratulations! Sobel Y data have been generated successfully! The result is PASS!! Congratulations! Sobel combine data have been generated successfully! The result is PASS!! ** Note: \$finish : D:/13_Digital_IC_Design/hw5/Ai/model2/testfixture.v(198) Time: 27739457491 ps Iteration: 0 Instance: /testfixture</pre>		
Synthesis Result					
Total logic elements			551 / 68,416 (< 1 %)		
Total memory bit			0 / 1,152,000 (0 %)		
Embedded multiplier 9-bit element			0 / 300 (0 %)		
(your flow summary)					
					
Description of your design					

My design implement an image edge detection system, use Gx and Gy to convolve the image to obtain the sobelX image and sobelY image and then add sobelX image and sobelY image together and divide by 2 for the output image of sobelCombine. My circuit use Sobel operator is one of the operators in image processing, also known as Sobel-Federman operator or Sobe filter, which is often used to do edge detection in the field of image processing and computer vision. of the operators in image processing, also known as Sobel-Federman operator or Sobe filter, which is often used to do edge detection in the field of image processing and computer vision. Csel is the signal indicates which operation output memory of the Sobel circuit the current write or read data. In the operation sequence, the SOBEL circuit uses the iaddr signal to send the address of the image data to testfixture. After the negative edge of each clock, the testfixture will send the pixel data of the address into the SOBEL circuit by the idata signal. After the calculation is finished, the busy signal should set to 0, and then it will start the verification. After obtaining the graphs of Sobel X and Sobel Y, use (Sobel X + Sobel Y) / 2 and then round-up for the SobelCombine. After the calculation is finished, the busy signal should set to 0, and then it will start the verification. the output data memories L0_MEM0, L0_MEM1, and L0_MEM2 of each layer are all in RAM models and have the identical control method and timing sequence. All of them can perform writing and reading operations. The csel signal selects the memory corresponding to each layer output. The cwr signal enables the write operation of the memory selected, and the crd as the read enable signal.

```
`timescale 1ns/10ps
`define CYCLE      30.0
`define End_CYCLE  100000000
```

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*