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Application note

Introduction to USB Type-C® Power Delivery for STM32 MCUs and MPUs

Introduction

This application note is a guideline for using USB Type-C® Power Delivery with STM32 MCUs and MPUs in conjunction with the TCPP01-M12 for power sink, TCPP02-M18 for power source, and TCPP03-M20 for dual-role power protection circuits. Some basic concepts of the two new USB Type-C® and USB Power Delivery standards are also introduced.

USB Type-C® technology offers a single-platform connector carrying all the necessary data. This new reversible connector makes plug insertion more user friendly. Using the Power Delivery protocol allows negotiation of up to 100 W power delivery to supply or charge equipment connected to a USB port. The objective is to reduce the need for cabling and connectors, and to facilitate the use of universal chargers.

The USB Type-C® connector provides native support of up to 15 W (up to 3 A at 5 V), extendable to 100 W (up to 5 A at 20 V) with the optional USB Power Delivery feature.

1 General information

This document applies to STM32 MCUs and MPUs, based on Arm® Cortex®-M processor.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

1.1 Acronyms and abbreviations

Acronym	Meaning
AMS	Atomic message sequence
APDO	Augmented power delivery object
BMC	Bi-phase mark coding
BSP	Board support package
CAD	Cable detection module
DFP	Downstream facing port
DPM	Device policy manager
DRP	Dual-role power
DRS	Data role swap
GP	General purpose
GUI	Graphical user interface
HAL	Hardware abstraction layer
HW	Hardware
LL	Low layer
MSC	Message sequence chart
OVP	Over-voltage protection
PDO	Power delivery object
PE	Policy engine
PRL	Physical protocol layer
PRS	Power role swap
SNK	Power sink
SRC	Power source
UCPD	USB Type-C Power Delivery
UCSI	USB Type-C® Connector System Software Interface
UFP	Upstream facing port
VDM	Vendor defined messages
FWUP	Firmware update
PPS	Programmable power supply
TCPM	Type-C port manager
TCPC	Type-C port controller
TVS	Transient voltage suppression

1.2 Reference documents

Table 1. STMicroelectronics ecosystem documents

Reference	Document title
STMicroelectronics ecosystem documents	
[1]	Managing USB Power Delivery systems with STM32 microcontrollers, UM2552
[2]	STM32CubeMonitor-UCPD software tool for USB Type-C® Power Delivery port management, UM2468
[3]	TCPP01-M12 USB Type-C® port protection, DS12900
[4]	TCPP02-M18 USB Type-C® port protection, DS13787
[5]	TCPP03-M20 USB Type-C® port protection, DS13618
[6]	USB Type-C® protection and filtering, AN4871
[7]	STM32CubeMonitor-UCPD software tool for USB Type-C® Power Delivery port management, DB3747
[8]	USB Type-C® and Power Delivery DisplayPort Alternate Mode, TA0356
[9]	Overview of USB Type-C® and Power Delivery technologies, TA0357
[10]	STM32MP151/153/157 MPU lines and STPMIC1B integration on a battery powered application, AN5260
[11]	USB hardware and PCB guidelines using STM32 MCUs, AN4879
[12]	Getting started with the X-NUCLEO-DRP1M1 USB Type-C® Power Delivery dual role port expansion board based on TCPP03-M20 for STM32 Nucleo, UM2891
[13]	Getting started with the X-NUCLEO-SRC1M1 USB Type-C® Power Delivery source expansion board based on TCPP02-M18 for STM32 Nucleo, UM2973
[14]	STM32 USB Power Delivery landing page *https://www.st.com/content/st_com/en/ecosystems/stm32-usb-c.html*
[15]	STM32 USB Power Delivery wiki page *https://wiki.st.com/stm32mcu/wiki/Introduction_to_USB_Power_Delivery_with_STM32*
USB specification documents	
[16]	USB2.0 Universal Serial Bus Revision 2.0 Specification
[17]	USB3.1 Universal Serial Bus Revision 3.2 Specification
[18]	USB BC Battery Charging Specification Revision 1.2
[19]	USB BB USB Device Class Definition for Billboard Devices
[20]	Universal Serial Bus Power Delivery Specification, Revision 2.0, Version 1.3, January 12, 2017
[21]	Universal Serial Bus Power Delivery Specification, Revision 3.1, Version 1.7, January 2023
[22]	Universal Serial Bus Type-C Cable and Connector Specification 2.0, August 2019
[23]	USB Billboard Device Class Specification, Revision 1.0, August 11, 2014, http://www.usb.org/developers/docs
[24]	USB Type-C® Connector System Software Interface Specification, requirements specification (UCSI), January 2020, revision 1.2

2 USB Type-C in a nutshell

The USB Implementers Forum (USB-IF) introduces two complementary specifications:

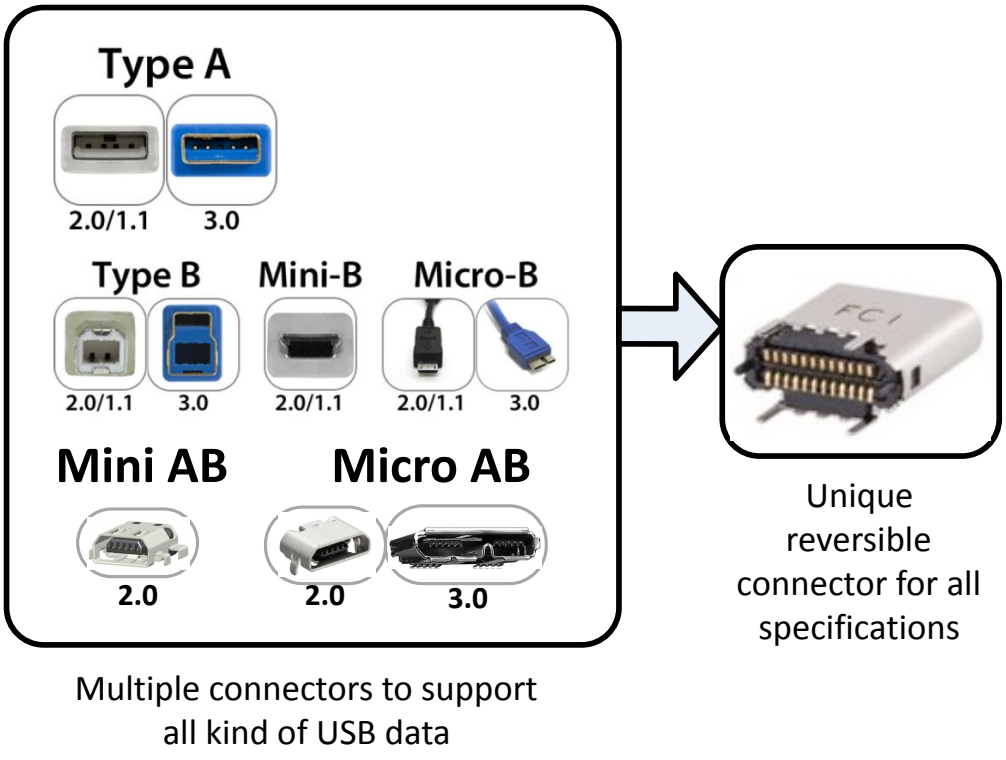
- The USB Type-C® cable and connector specification release 1.3 details a reversible, slim connector system based on high-speed USB2.0 signals and two super-speed lanes at up to 10 Gbit/s, which can also be used to support alternate modes.
- The USB Power Delivery (PD) specification revisions 2.0 and 3.0 detail how a link can be transformed from a 4.5 W power source (900 mA at 5 V on VBUS), to a 100 W power or consumer source (up to 5 A at 20 V).

The new 24-pin USB Type-C® plug is designed to be non-polarized and fully reversible, no matter which way it is inserted.

It supports all the advanced features proposed by Power Delivery:

- negotiating power roles
- negotiating power sourcing and consumption levels
- performing active cable identification
- exchanging vendor-specific sideband messaging
- performing alternate mode negotiation, allowing third-party communication protocols to be routed onto the reconfigurable pins of the USB Type-C® cable

Figure 1. USB connectors



The following points should also be noted:

- USB Type-C® cables use the same plug on both ends.
- USB Type-C® supports all prior protocols from USB2.0 onward, including the driver stack and power capability.
- The new connector is quite small (it is 8.4 mm wide and 2.6 mm high).

As shown in Figure 1. USB connectors, the new USB Type-C® plug covers all features provided by previous plugs, which ensure flexibility and simplifies the application.

A USB Type-C® port can act as host only, device only, or have dual function. Both data and power roles can independently and dynamically be swapped using USB Power Delivery commands.

2.1 USB Type-C® vocabulary

The terminology commonly used for USB Type-C® system is:

- **Source**: A port power role. Port exposing Rp (pull-up resistor, see Figure 3. Pull up/down CC detection) on CC pins (command control pins, see Section 4 CC pins), and providing power over VBUS (5 V to 20 V and up to 5 A), most commonly a Host or Hub downstream-facing port (such as legacy Type-A port).
- **Sink**: A port power role. Port exposing Rd (Pull down resistor. See Figure 3. Pull up/down CC detection) on CC pins and consuming power from VBUS (5 V to 20 V and up to 5 A), most commonly a device (such as a legacy Type-B port)
- **Dual-role power (DRP) port**: A port that can play source or sink power roles, reversible dynamically.
- **Downstream-facing port (DFP)**: A port data role. A USB port at higher level of USB tree, such as a USB host or a hub expansion.
- **Upstream-facing port (UFP)**: A port data role. A USB port at lower level of USB tree, such as a USB device or a hub master port.

2.2 Minimum mandatory feature set

It is not mandatory to implement and support all of the advanced features that are defined within Type-C and Power Delivery specifications.

The mandatory functions to support are:

- cable attach and detach detection
- plug orientation/cable twist detection
- USB2.0 connection

3 Connector pin mapping

The 24-pin USB Type-C® connector includes:

- symmetric connections:
  - USB2.0 differential pairs (D+/D-)
  - power pins: VBUS/GND
- asymmetric connections
  - two sets of TX/RX signal paths which support USB3.1 data speed
  - configuration channels (CC lines) which handle discovery, configuration and management of USB Type-C® Power Delivery features
  - two side-band use signals (SBU lines) for analog audio modes or alternate mode

Figure 2. Receptacle pinout

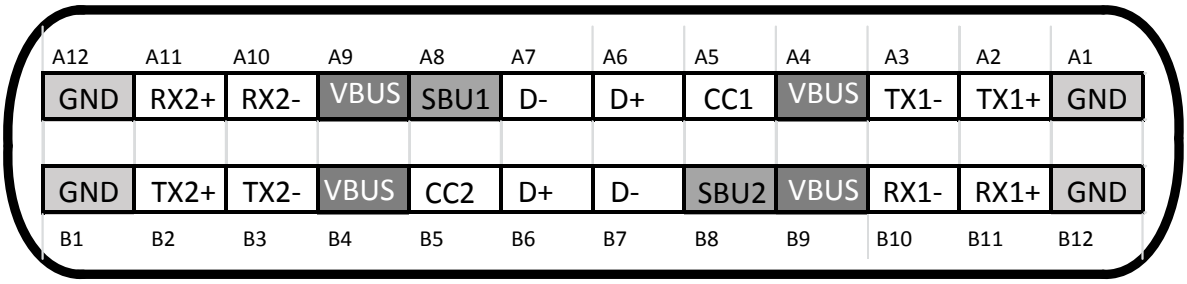


Table 2. USB Type-C receptacle pin descriptions

Pin	Name	Description	Comment
A1	GND	Ground return	up to 5 A split into 4 pins
A2	TX1+	USB3.0 datalines or alternate	10 Gbit/s TX differential pair in USB3.1
A3	TX1-		
A4	VBUS	Bus power	100 W max power split into 4 pins
A5	CC1 or VCONN	Configuration channel or power for active or electronically marked cable	In VCONN configuration, min power is 1 W
A6	D+	USB2.0 data lines	-
A7	D-		
A8	SBU1	Side band use	Alternate mode only
A9	VBUS	Bus power	100 W max power split into 4 pins
A10	RX2-	USB3.0 datalines or alternate	10 Gbit/s RX differential pair USB3.1
A11	RX2+		
A12	GND	Ground return	up to 5 A split into 4 pins
B1	GND	Ground return	up to 5 A split into 4 pins
B2	TX2+	USB3.0 datalines or alternate	10 Gbit/s TX differential pair in USB3.1
B3	TX2-		

Pin	Name	Description	Comment
B4	VBUS	Bus power	100 W max power split into 4 pins
B5	CC2 or VCONN	Configuration channel or power for active or electronically marked cable	In VCONN configuration, min power is 1 W
B6	D+	USB2.0 datalines	-
B7	D-		-
B8	SBU2	Side band use	Alternate mode only
B9	VBUS	Bus power	100 W ma power split into 4 pins
B10	RX1-	USB3.0 datalines or alternate	10 Gbit/s RX differential pair in USB3.1
B11	RX1+		
B12	GND	Ground return	Up to 5 A split into 4 pins

3.1 VBUS power options

VBUS provides a path to deliver power between a host and a device, and between a charger and a host or device.

Power options available from the perspective of a device with a USB Type-C® connector are listed below.

Table 3. Power supply options

Mode of operation	Nominal voltage	Maximum current	Note
USB2.0	5 V	500 mA	Default current based on specification
USB3.1	5 V	900 mA	
USB BC1.2	5 V	1.5 A	Legacy charging
Current @1.5 A	5 V	1.5 A	Support high-power devices
Current @3 A	5 V	3 A	
USB PD	5 V to 20 V	5 A	Directional control and power level management

Note: USB Type-C® to Type-C™ cable assembly needs VBUS to be protected against 20 V DC at the rated cable current (3 A or 5 A).

4 CC pins

There are two CC pins (CC1 and CC2) in the Type-C connector, but only one CC pin is present on the cable plug at each end of the cable (they are connected in common through the cable). On both CC1 and CC2, a source must expose Rp pull up resistors, whereas a sink must expose Rd pull down resistors. Electronic cables need to provide a resistor, Ra, to ground on V_{CONN}.

From a source point of view, the state of attached devices can be determined by referring to Table 4.

Table 4. Attached device states - source perspective

CC1	CC2	State
Open	Open	Nothing attached
Rd	Open	Sink attached
Open	Rd	
Open	Ra	Powered cable without sink attached
Ra	Open	
Rd	Ra	Powered cable with sink, VCONN-powered accessory (VPA), or VCONN-powered USB device (VPD) attached.
Ra	Rd	
Rd	Rd	Debug accessory mode attached
Ra	Ra	Audio adapter accessory mode attached

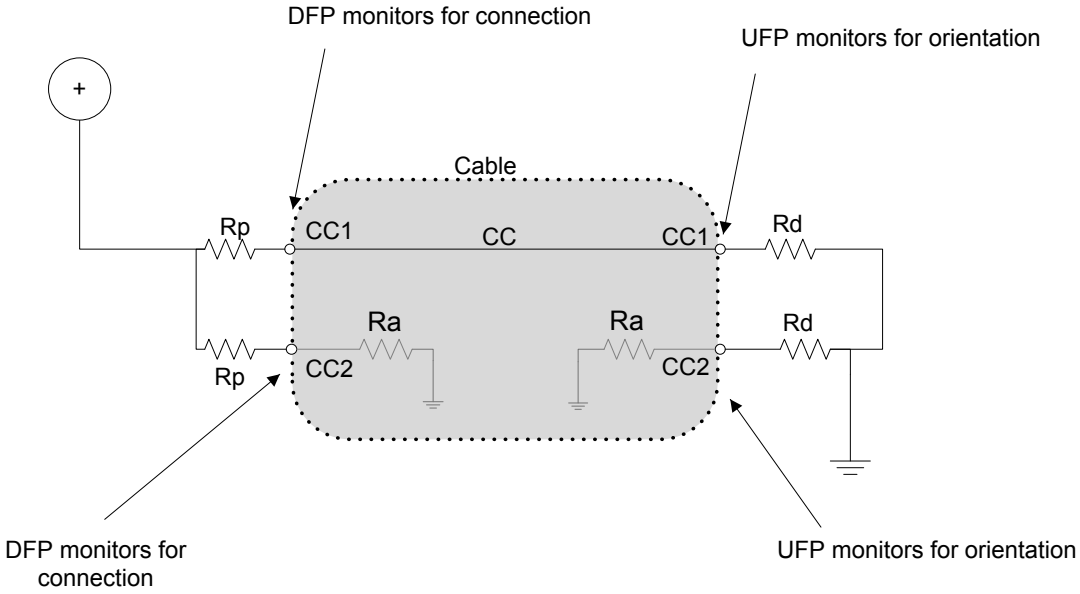
4.1 Plug orientation/cable twist detection

As a USB Type-C® cable plug can be inserted in the receptacle in either orientation, it is mandatory to first detect the orientation. The detection is done through the CC lines using the Rp/Rd resistors.

Initially a DFP presents Rp terminations on its CC pins and a UFP presents Rd terminations on its CC pins.

To detect the connection, the DFP monitors both CC pins (see figure 4-30 in [22]).

Figure 3. **Pull up/down CC detection**



4.2 Power capability detection and usage

Type-C offers increased current capabilities of 1.5 A and 3 A in addition to the default USB standard.
The current supply capability of the port to the device depends on the Rp pull up resistor value on the DFP.
High current (5 A) capability is negotiated using the USB Power Delivery protocol.
Table 5 shows the possible values, as per [22].

Table 5. DFP CC termination (Rp) requirements

V_{BUS} power	Current source to 1.7 V - 5.5 V	Rp pull up to 4.75 V - 5.5 V	Rp pull up to 3.3 V +/-5%
Default USB power	80 mA ± 20%	56 kΩ ± 20% (1)	36 kΩ ± 20%
1.5 A @5 V	180 mA ± 8%	22 kΩ ± 5%	12 kΩ ± 5%
3.0 A @5 V	330 mA ± 8%	10 kΩ ± 5%	4.7 kΩ ± 5%

1. *For Rp when implemented in the USB Type-C plug on a USB Type-C to USB 3.1 Standard-A Cable Assembly, a USB Type-C to USB 2.0 Standard-A Cable Assembly, a USB Type-C to USB 2.0 Micro-B Receptacle Adapter Assembly or a USB Type-C captive cable connected to a USB host, a value of 56 kΩ ± 5% shall be used, in order to provide tolerance to IR drop on V_{BUS} and GND in the cable assembly.*

The UFP must expose Rd-pull down resistors on both CC1 and CC2 to bias the detection system and to be identified as the power sink, as per [22].

Table 6. UFP CC termination (Rd) requirements

Rd implementation	Nominal value	Can detect power capability?	max voltage on CC pin
± 20% voltage clamp	1.1 V	No	1.32 V
± 20% resistor to GND	5.1 kΩ	No	2.18 V
± 10% resistor to GND	5.1 kΩ	Yes	2.04 V

The UFP, in order to determine the DFP power capability, monitors the CC line voltages accurately, as per [22].

Table 7. Voltage on sink CC pins (multiple source current advertisements)

Detection	Min voltage (V)	Max voltage (V)	Threshold (V)
vRa	-0.25	0.15	0.2
vRd-Connect	0.25	2.04	-
vRd-USB	0.25	0.61	0.66
vRd-1.5	0.70	1.16	1.23
vRd-3.0	1.31	2.04	-

5 Power profiles

The USB Power Delivery protocol enables advanced voltage and current negotiation, to deliver up to 100 W of power, as defined in [21] and reported in the following figure:

Figure 4. Power profile

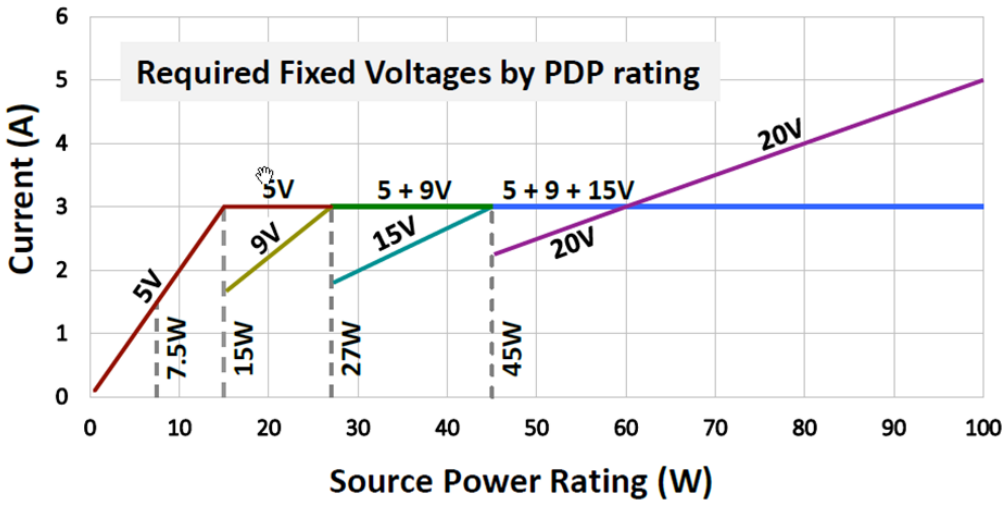


Table 8 shows the permitted voltage source and programmable power supply (PPS) selections, as a function of the cable current rating.

Table 8. Fixed and programmable power supply current and cabling requirements

Power range	Fixed voltage source				Programmable power supply (PPS)			
	5 V	9 V	15 V	20 V	5 V (3.3 to 5.9 V)	9 V (3.3 to 11 V)	15 V (3.3 to 16 V)	20 V (3.3 to 21 V)
With 3 A cable								
0 W < PDP <= 15 W	PDP / 5	-	-	-	PDP / 5	-	-	-
15 W < PDP <= 27 W	3.0 A	PDP / 9	-	-	3.0 A	PDP / 9	-	-
27 W < PDP <= 45 W	3.0 A	3.0 A	PDP / 15	-	3.0 A	3.0 A	PDP / 15	-
45 W < PDP <= 60 W	3.0 A	3.0 A	3.0 A	PDP / 20	3.0 A	3.0 A	3.0 A	PDP / 20
With 5 A cable								
60 W < PDP <= 100 W	3.0 A	3.0 A	3.0 A	PDP / 20	3.0 A	3.0 A	3.0 A	PDP / 20

Further information is available in [21] and [22].

6 USB Power Delivery 2.0

In USB Power Delivery, pairs of directly attached ports negotiate voltage, current and/or the direction of power, and data flow over the USB cable. The CC wire is used as a BMC-coded communication channel.

The mechanisms used operate independently of other USB power negotiation methods.

6.1 Power Delivery signaling

All communications are done through a CC line in half-duplex mode at 300 Kbit/s.

Communication uses BMC encoded 32-bit 4b/5b words over CC lines.

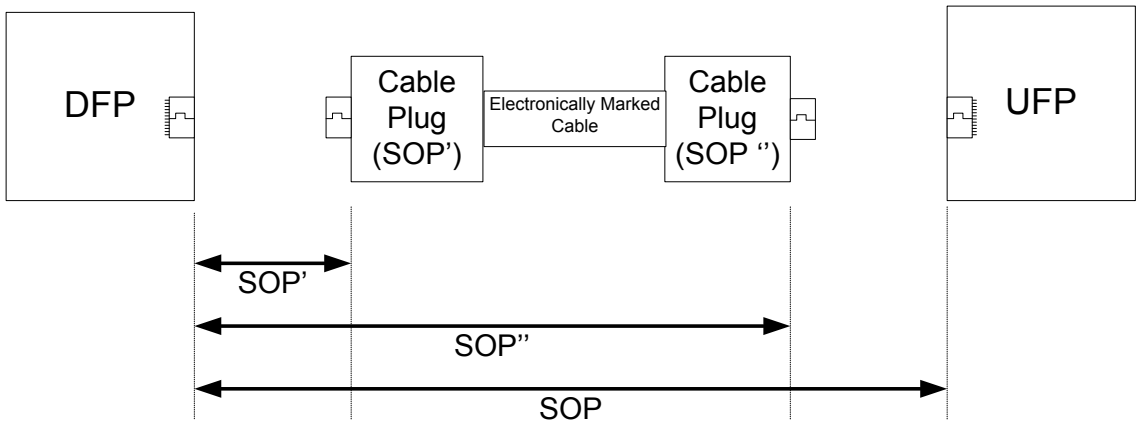
6.1.1 Packet structure

The packet format is:

- Preamble: 64-bit sequence of alternating 0s and 1s to synchronize with the transmitter.
- SOP*: start of packet. Can be SOP, SOP' (start of packet sequence prime) or SOP" (start of packet sequence double prime), see Figure 5. SOP* signaling.
  - SOP packets are limited to PD capable DFP and UFP only
  - SOP' packets are used for communication with a cable plug attached to the DFP
  - SOP" packets are used for communication with a cable plug attached to the UFP.

  A cable plug capable of SOP' or SOP" communication must only detect and communicate with packets starting with SOP' or SOP".
- Message data including message header which identifies type of packet and amount of data
- CRC: error checking
- EOP: end of packet, unique identifier.

Figure 5. SOP* signaling



6.1.2 K-codes

K-codes are special symbols provided by the 4b/5b coding. They signal hard reset, cable reset, and delineate packet boundaries.

6.2 Negotiating power

The DFP is initially considered as a bus master.

The protocol layer allows the power configuration to be dynamically modified.

The power role, data role and VCONN swap are possible independently if both ports support dual power role functionality.

The default voltage on VBUS is always 5 V and can be reconfigured as up to 20 V.

The default current capability is initially defined by the Rp value, and can be reconfigured as up to 5 A for an electronically marked USB PD Type-C cable.

The protocol uses start-of-packet (SOP) communications, each of which begins with an encoded symbol (K-code).

SOP communication contains a control or data message.

The control message has a 16-bit fixed size manages data flow.

The data message size varies depending on its contents. It provides information on data objects.

7 USB Power Delivery 3.0

From the power point of view, there are no differences between USB PD 2.0 and USB PD 3.0. All USB PD 3.0 devices are able to negotiate power contracts with USB PD 2.0 devices, and vice-versa. USB PD 3.0 adds the following key features:

- Fast role swap
- Authentication
- Firmware update
- Programmable power supply (PPS) to support sink directed charging

The following is a summary of the major changes between the USB PD 3.0 and USB PD 2.0 specifications:

- Support for both Revision 2.0 and Revision 3.0 operation is mandated to ensure backward compatibility with existing products.
- Profiles are deprecated and replaced with PD power rules.
- BFSK support deprecated including legacy cables, legacy connectors, legacy dead battery operation and related test modes.
- Extended messages with a data payload of up to 260 bytes are defined.
- Only the VCONN source is allowed to communicate with the cable plugs.
- Source coordinated collision avoidance scheme to enable either the source or sink to initiate an atomic message sequence (AMS).
- Fast role swap defined to enable externally powered docks and hubs to rapidly switch to bus power when their external power supply is removed.
- Additional status and discovery of:
  - Power supply extended capabilities and status
  - Battery capabilities and status
  - Manufacturer defined information
- Changes to fields in the passive cable, active cable and AMA VDOs indicated by a change in the structured VDM version to 2.0.
- Support for USB security-related requests and responses.
- Support for USB PD firmware update requests and responses.

System policy now references USBTypeCBridge 1.0.

8 Alternate modes

All the hosts and devices (except chargers) using a USB Type-C® receptacle shall expose a USB interface.

If the host or device optionally supports alternate modes:

- The host and device shall use USB Power Delivery structured vendor defined messages (structured VDMs) to discover, configure and enter/exit modes to enable alternate modes.
- It is strongly encouraged that the device provide equivalent USB functionality where such exists for the best user experience.
- Where no equivalent USB functionality is implemented, the device must provide a USB interface exposing a USB billboard device class to provide information needed to identify the device. A device is not required to provide a USB interface exposing a USB billboard device class for non-user facing modes (for exmple diagnostic modes).

As alternate modes do not traverse the USB hub topology, they must only be used between a directly connected host and device.

8.1 Alternate pin reassignments

In Figure 6, pins highlighted in yellow are the only pins that may be reconfigured in a full-feature cable.

Figure 6. Pins available for reconfiguration over the full featured Cable

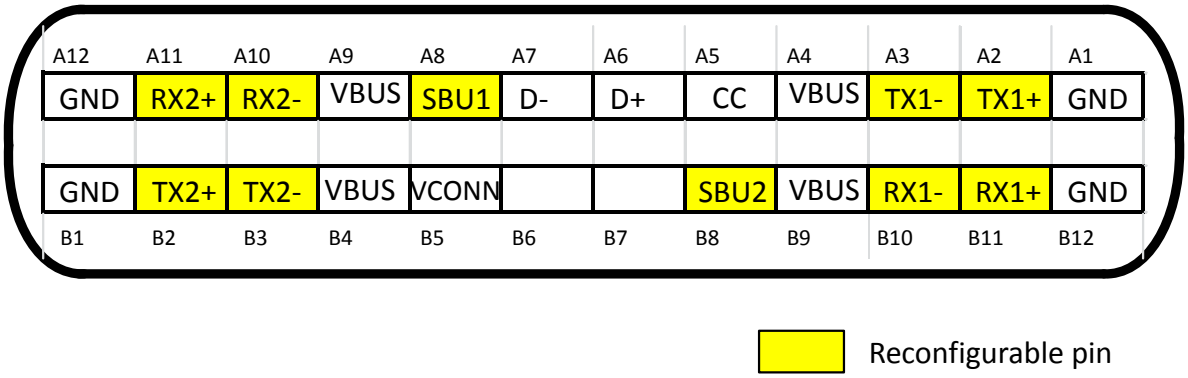
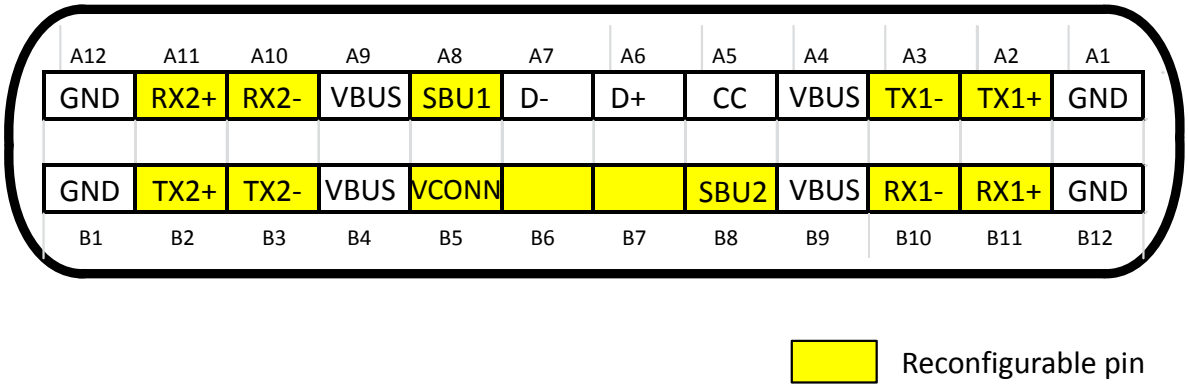


Figure 7 shows pins available for reconfiguration for direct connect applications. There are three more pins than in Figure 6 because this configuration is not limited by the cable wiring.

Figure 7. **Pins available for reconfiguration for direct connect applications**



Note: SBU may be left open if no alternate mode is supported. When alternate mode is supported, add a resistor superior to 4 MΩ to ensure USB safe state.

8.2 Billboard

The USB Billboard Device Class definition describes the methods used to communicate the alternate modes supported by a device container to a host system.

This includes string descriptors to provide support details in a human-readable format.

For more details, refer to [23].

9 Product offer

STM32 MCUs and STM32 MPUs handle USB Type-C / USB Power Delivery interfacing by using the STM32 integrated UCPD (USB Type-C Power Delivery) peripheral, or a set of general-purpose (GP) peripherals. See USB Type-C and Power Delivery application page.

Figure 8. USB Type-C Power Delivery block diagram

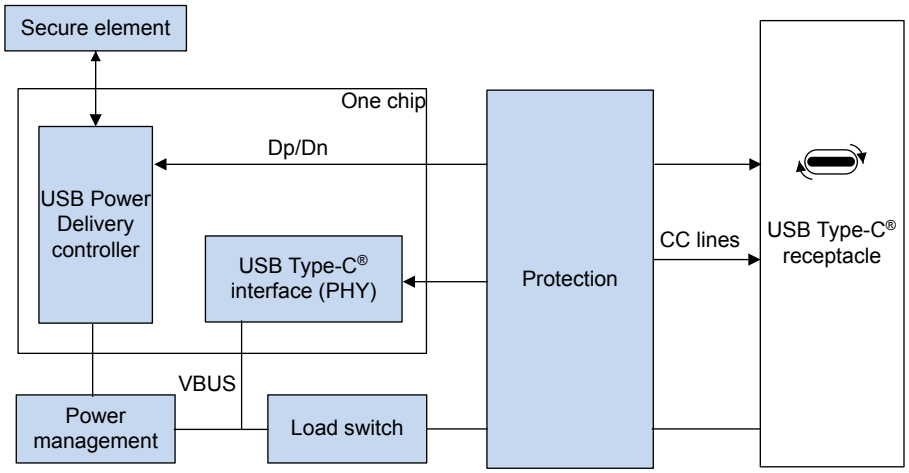


Figure 9. STM32G0 Discovery kit USB Type-C analyser

STM32 MPU product specificities

For the STM32 MPU products, take into the consideration the following:

- USB is only supported on Cortex-A7 core. No support on Cortex-M4 core.
- For compatibility with Linux framework, USB Type-C is managed by external devices. Refer to MB1272-DK2-C01 board schematics on , CN7 implementation with STUSB1600 chipset (as opposed to CN6 implementation with ADC).

For more information, refer to section *USB port using USB Type-C® receptacle* in [9].

10 Type-C with no Power Delivery

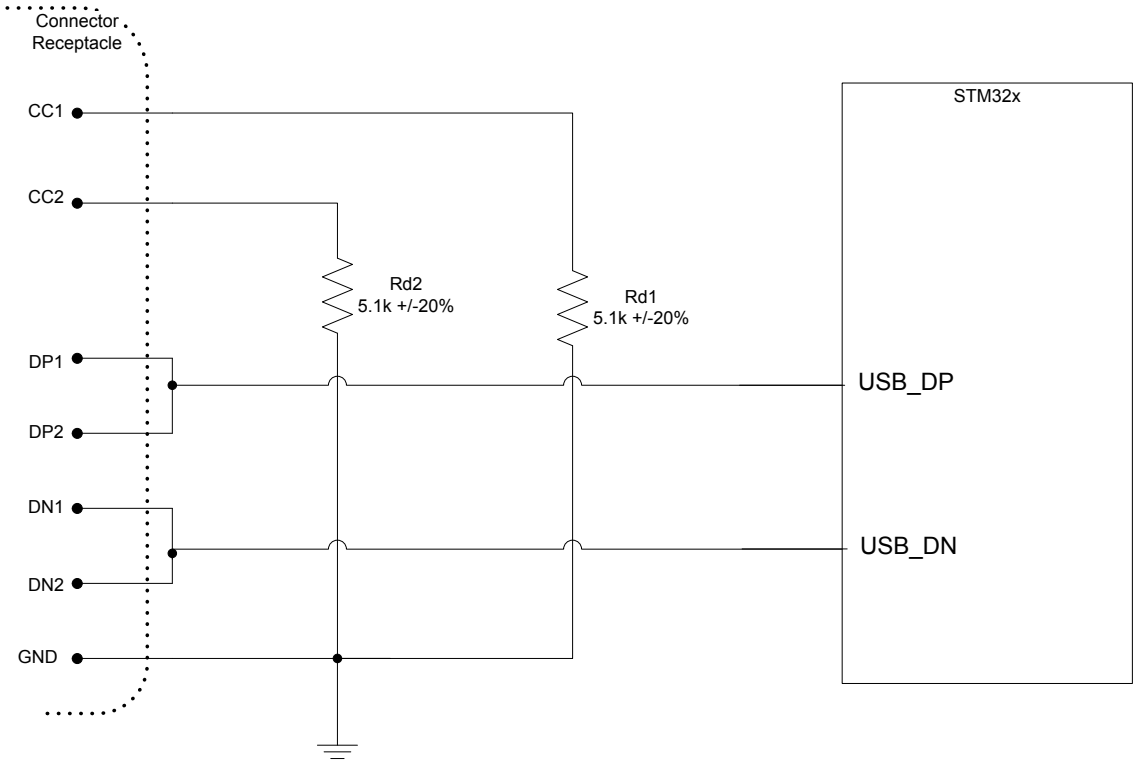
This chapter may not fully apply to STM32 MPU products. Refer to Section 9 Product offer for their specificities.

10.1 STM32 USB2.0-only device conversion for USB Type-C platforms

A USB2.0 legacy device needs to present itself as a UFP by means of an Rd pull-down resistor between the CC line and ground. It is assumed here that the maximum legacy USB 2.0 device current is needed, and it is therefore not necessary to monitor the CC lines.

Since the plug is reversible, the two DP/DN pairs need to be connected to each other as close as possible to the receptacle, before being routed to the STM32 device.

Figure 10. Legacy device using USB Type-C receptacle



10.2 STM32 USB2.0 host conversion for USB Type-C platforms

This use case describes how to exchange a USB2.0 standard A receptacle for a USB Type-C® receptacle.

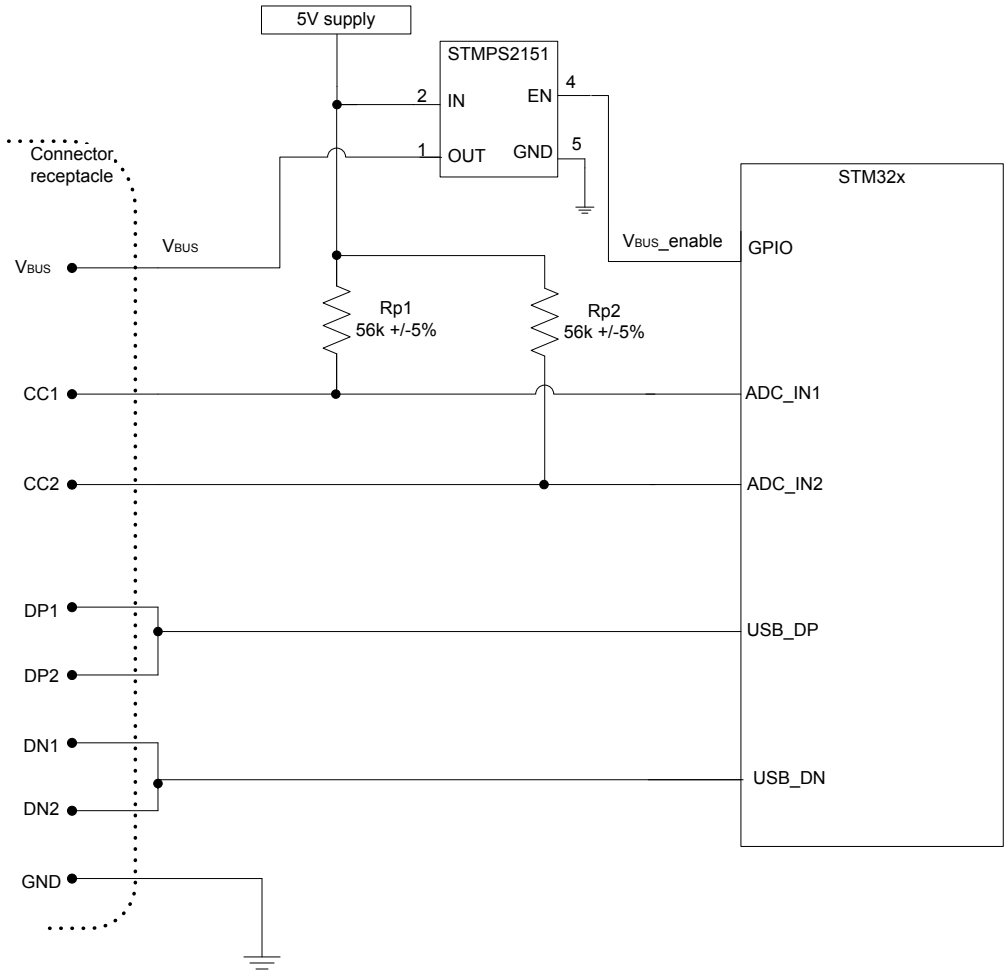
As the platform is designed for USB2.0, the maximum current capacity is 500 mA. If a higher supply current is available in the application, the Rp resistors can be adjusted to give 1.5 A or 3 A capability.

A USB2.0 legacy host needs to be configured as a DFP by means of a Rp pull up resistor between the CC line and the 5 V supply.

As the plug is reversible, the two DP/DN couples need to be connected in pairs as close as possible to the receptacle, before being routed to the STM32 device.

Monitoring CC lines through the ADC_IN inputs allow device-attachment detection and enabling of VBUS on the connector.

Figure 11. **Legacy host using USB Type-C receptacle**



10.3 STM32 legacy USB2.0 OTG conversion for USB Type-C platforms

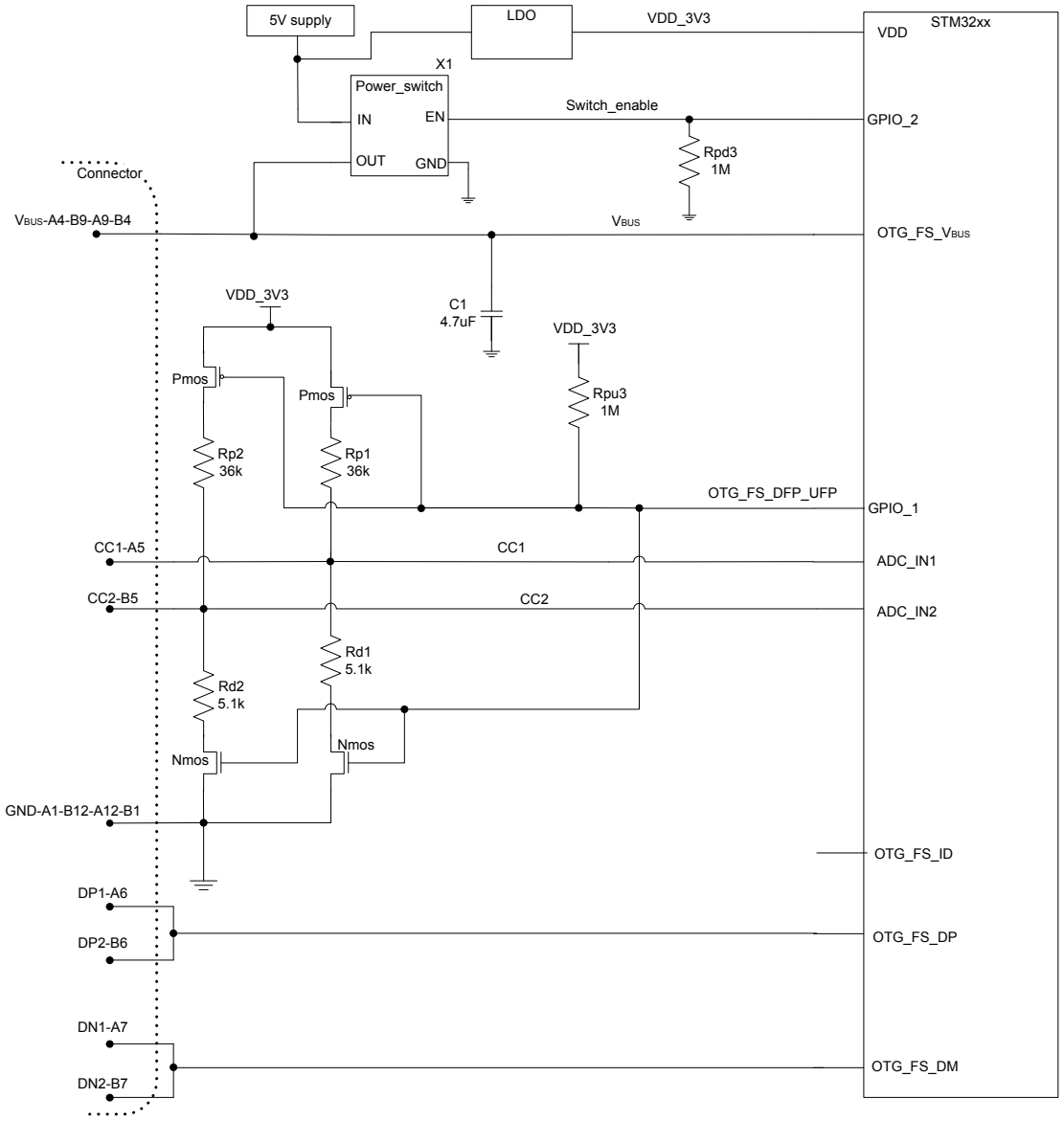
This use case explains how to exchange USB2.0 micro-AB receptacle for a USB Type-C® receptacle.

In this use case the platform is designed for USB2.0, so the maximum current capacity is 500 mA. If a higher supply current is available in the application, the Rp resistors can be adjusted to give 1.5 A or 3 A capability.

A legacy OTG platform starts to work as host or device depending on the USB_ID pin impedance to ground provided by the cable.

USB Type-C® is fully reversible, so the cable does not provide any role information. The role needs to be detected by sensing the CC lines (for example by using the ADC through its ADC_IN1 and ADC_IN2 inputs to detect the CC line level).

Figure 12. Legacy OTG using USB Type-C receptacle



The suggested sequence is:

1. Connect GPIO1 to OTG_FS_DFP_UFP driving a high level, and GPIO2 to Switch_enable driving a low level, to identify the platform as UFP.
2. If VBUS is detected, the platform starts with the USB2.0 controller acting as a device.
3. If no VBUS is detected after 200 ms minimum, OTG_FS_DFP_UFP is pulled down to be identified as a DFP through the Rp resistors, and to check whether a UFP is connected by comparing the ADC_IN1 and ADC_IN2 voltages to the expected threshold on the CC lines. Power switch X1 is kept disabled.
4. If UFP connection is detected, Switch_enable is pulled up to provide VBUS on the connector, and the platform starts with the USB2.0 controller acting as host.

Because of the plug reversibility, the two DP/DN pairs need to be connected as pairs as close as possible to the receptacle, before routing to the STM32 device.

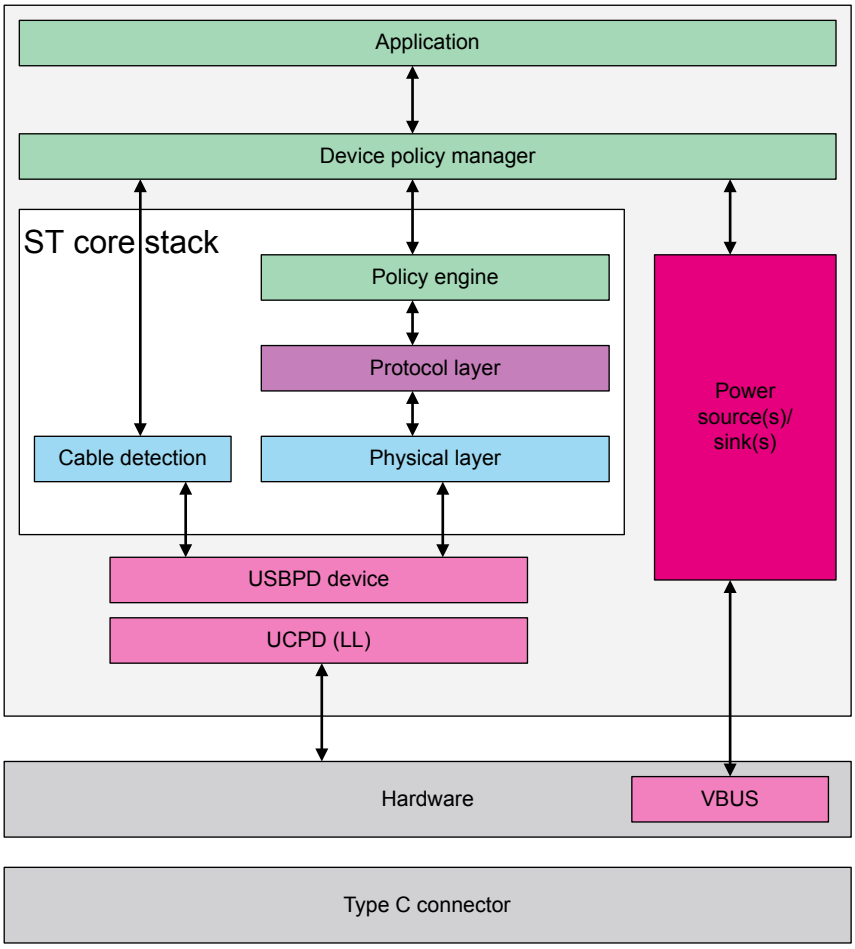
11 Type-C with Power Delivery using integrated UCPD peripheral

This chapter may not fully apply to STM32 MPU products. Refer to Section 9 Product offer for their specificities.

11.1 STM32 MCU software overview

STMicroelectronics delivers a proprietary USB Power Delivery stack based on the USB.org specification. The stack architecture overview is shown below.

Figure 13. USB Power Delivery stack architecture



Two parts are fully managed by STMicroelectronics (USB PD core stack and USB PD devices), so the user only needs to focus development effort on two other parts:

- User application part: called the 'device policy manager' inside the USB organization specification. STMicroelectronics delivers an application template to be completed according to the application need.
- Hardware part: the effort is mainly focused on energy management, which depends on the resource materials chosen by the user to manage Type-C power aspects.

This document provides hardware implementation guidelines for the use of the STM32 resources (ADC, GPIO, and so on), but the reference for power constraints for the developers is chapter 7 in *Power supply' of the Universal Serial Bus Power Delivery Specification*. Also refer to [1] for further information.

Note: The STMicroelectronics core stack is delivered as a certified library to follow the USB Power Delivery requirements (USB Power Delivery protocol, State machine specification). API description is defined in this document [1].

11.2 STM32 MPU software overview

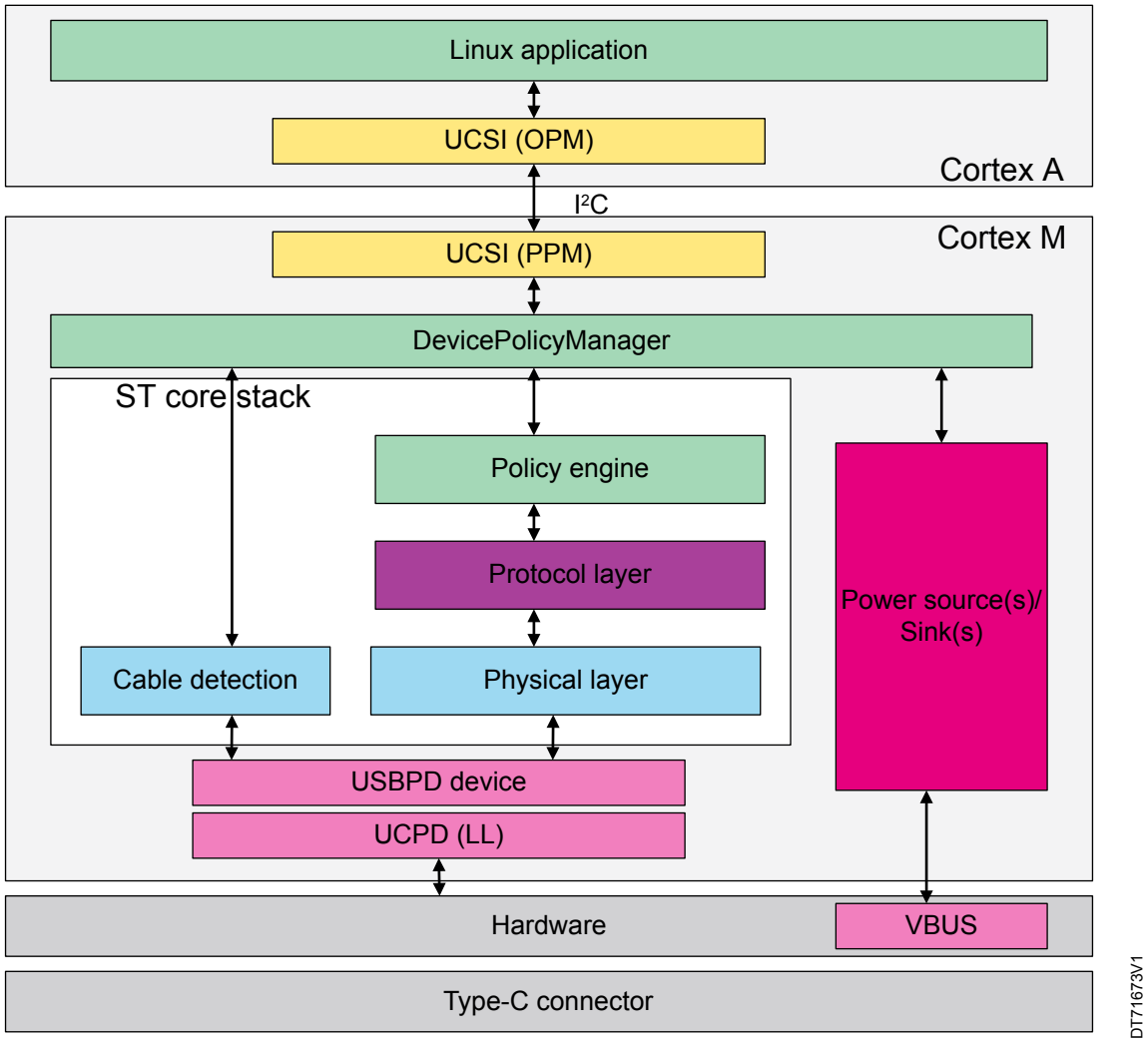
The power delivery controller can be monitored using *USB Type-C® Connector System Software Interface* [24].

The kernel driver of the UCSI layer is available in Linux Community on top of DevicePolicyManager (DPM).

All schematics available for the STM32 MCU integrated UCPD peripheral can be applied.

The hardware link used for the UCSI communication can be an I²C bus.

Figure 14. STM32 MPU software overview



Resources

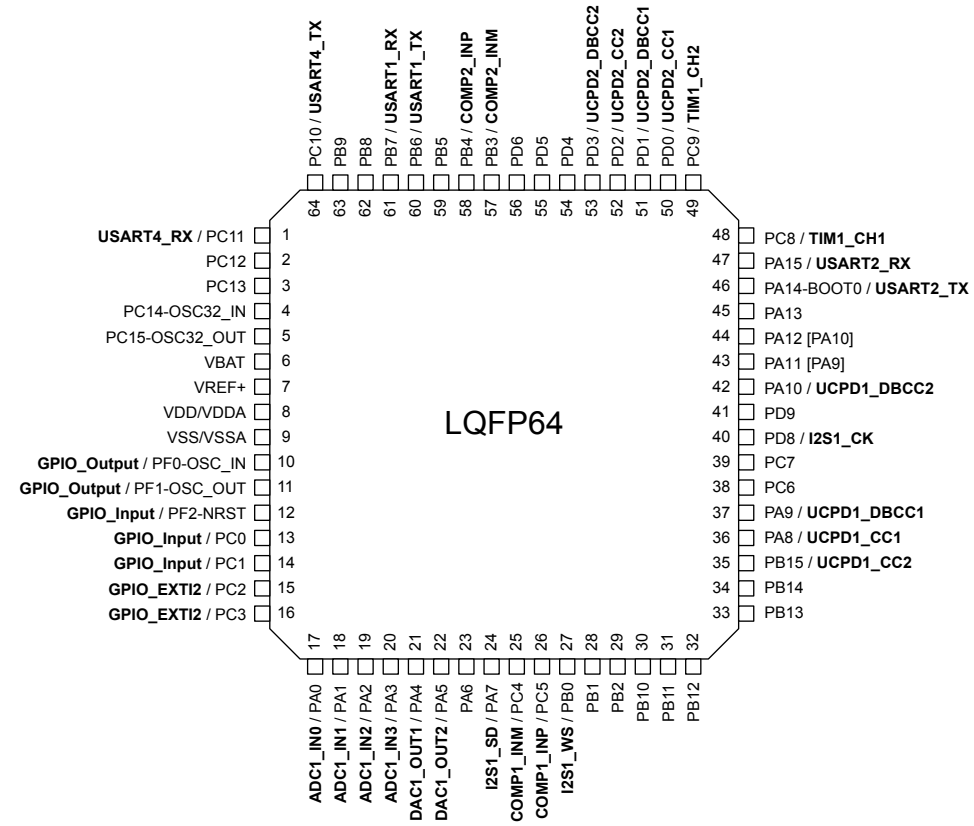
X-CUBE-UCSI is a STMicroelectronics original initiative. It is used for USB Type-C® and power delivery software expansion for STM32Cube.

X-CUBE-UCSI package consists of libraries, drivers, sources, APIs, and application examples running on STM32G0 32-bit microcontroller. This microcontroller acts as an UCSI Platform Policy Manager (PPM) on the STM32MP135F-DK board. The PPM is a combination of hardware and firmware that manages the USB Type-C® connectors on the platform. The STM32MP13 has a role of UCSI OS Policy Manager (OPM) to interface with the PPM, via I²C with the UCSI interface.

11.3 Hardware overview

Using the STM32 UCPD peripheral, flexible and scalable architectures can be achieved. STM32 GP peripherals such as PWM, ADC, DAC, I2C, SPI, UART, COMP, OPAMP, RNG, and RTC can be used. See the STM32CubeMx pinout tools for detailed information.

Figure 15. Device pinout example



The following sections show how to implement each power mode from the hardware point of view. All information concerning the software implementation is available in the reference specification.

11.3.1 DBCC1 and DBCC2 lines

Recap of *Dead battery* functionality in Type-C systems

A USB Type-C sink supporting the *Dead battery* function keeps pulling the attached CC line(s) down as per Table 9 even when unpowered. According the USB Type-C standard, this can be implemented as a resistor or a voltage clamp, as shown in the following table. Thanks to this, the USB Type-C source attached to the sink can detect that the sink is unpowered (which corresponds to dead battery for battery-powered application). The USB Type-C source (for example a battery charger) can then supply power through the VBUS line.

Table 9. USB Type-C sink behavior on CC lines

State	Pull-down function on CC lines	
	Sink without *Dead battery* support	Sink with *Dead battery* support
Unpowered	None	5.1 kΩ resistor or a voltage clamp (*DB*)
Powered	5.1 kΩ	5.1 kΩ resistor

When the USB Type-C sink is back to powered, it changes the value of its Rd pull-down resistance to one of values specified for normal operation.

Upon transiting from *Dead battery* state to VBUS-powered state, the Type-C specification requires that the switch of the Rd value from *DB* to *"operating"* does not transit through a state without any pull-down resistance. It accepts a short transient during which the value of Rd is out of specified operating values. Refer to *Termination parameters* section of the *USB Type-C* specification for full requirements.

Implementation on STM32 devices with integrated UCPD peripheral

The devices incorporate the Rp and Rd function of the CCx (x = 1 or 2) pins to fulfill the USB Type-C requirements. For the *Dead battery* support, the DBCCx (x = 1 or 2) pins must externally be connected with their respective CCx pins.

Control paths (1) to (3) shown in Figure 16 through Figure 19 manage the switching between Rp and Rd functionality on the CCx pins, according to the application topology and state.

When the STM32 device is unpowered, a voltage exceeding 1 V on the DBCCx pins acting as inputs activates, through the control path (3), the *Dead battery* pull-down functionality (*DB*) on their respective CCx pin. It is maintained until the device is powered and the software disables it through the control path (1). The *DB* disable action activates Rd or Rp value for normal operation that the software application should set beforehand.

When the device is used as USB Type-C source or as a USB Type-C sink without *Dead battery* support, the DBCCx pins can be used as GPIOs controlled through the control path (2). In such applications, a weak external pull-down resistor (for example 100 kΩ) on the DBCCx pin ensures that *DB* pull-down functionality is not activated on the corresponding CCx pin when the device is powered down.

DBCCx usage in non-protected application

When the device is unpowered, the DBCCx pins act as inputs. A high level on a DBCCx has the consequence of exposing Rd = *DB* on the corresponding CCx pin to signal dead battery state. For the device acting as sink to support the *Dead battery* function when directly connected with a USB Type-C source, the DBCCx pins must be shorted with their corresponding CCx pins. As soon as the device is powered, the Rd exposed on its CCx pins automatically transits to the value defined through the control registers, as shown in Figure 16. The termination in this configuration must be of Rd (pull-down) type.

Figure 16. **Non-protected sink application supporting *Dead battery* feature**

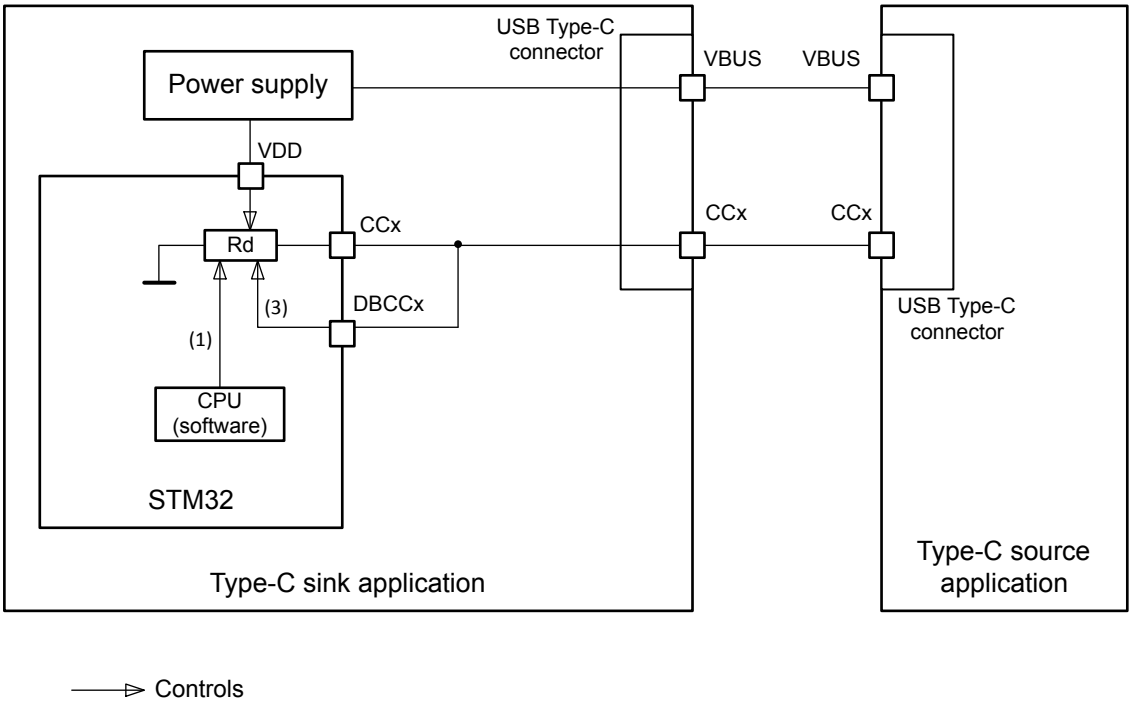


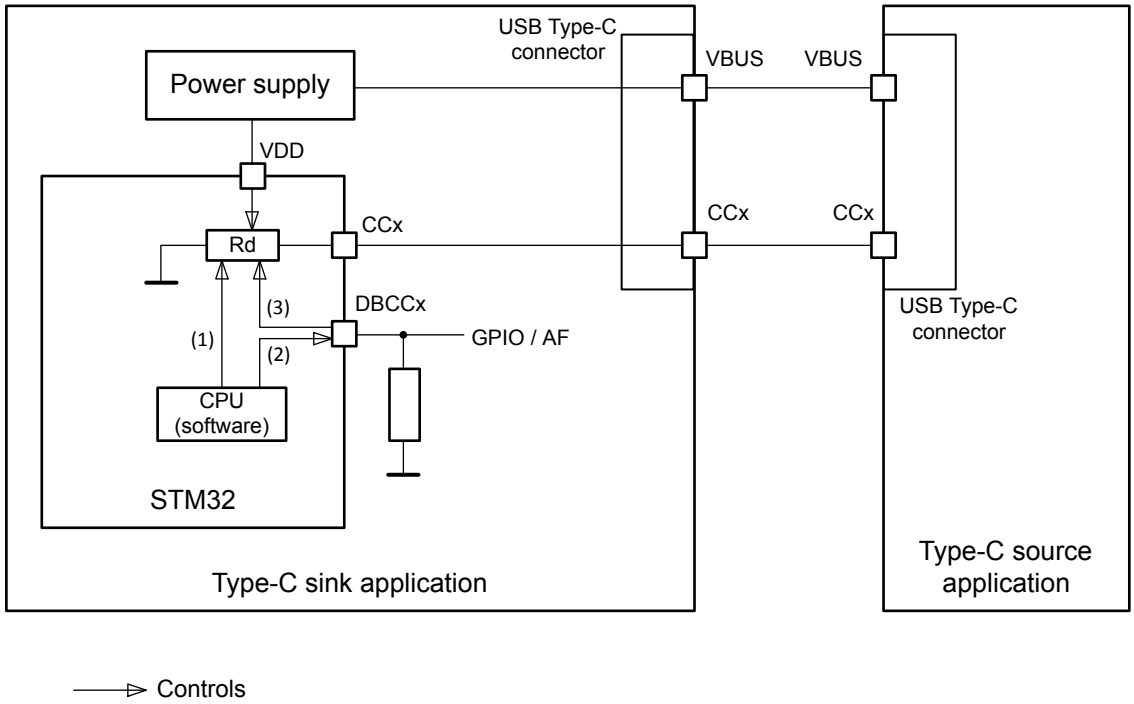
Table 10. **Non-protected sink - sequence of exiting *Dead battery* mode**

Sequence	VBUS	VDD	Rd value	Comment
Step 0	0 V	0 V	*DB*	-
Step 1	5 V	0 V	*DB*	VBUS arrives
Step 2	5 V	3.3 V	default Rd	device supply arrives
Step 3	5 V	3.3 V	as selected by SW	upon write to ANAMODE

When the device acts as a USB Type-C source, the Rd on CCx pins must never be set to *DB* value. This is ensured by keeping the DBCCx pins separate from their corresponding CCx pins and by pulling them down through a high-value (such as 100 kΩ) external pull-down resistor, which in the unpowered state ties them low. The solution also fits a non-protected non-*Dead-battery* sink application.

In both cases, when the device is powered, the DBCCx pins can be used as I/Os, as shown in Figure 17.

Figure 17. **Non-protected sink not supporting *Dead battery* feature**



DBCCx usage in protected application

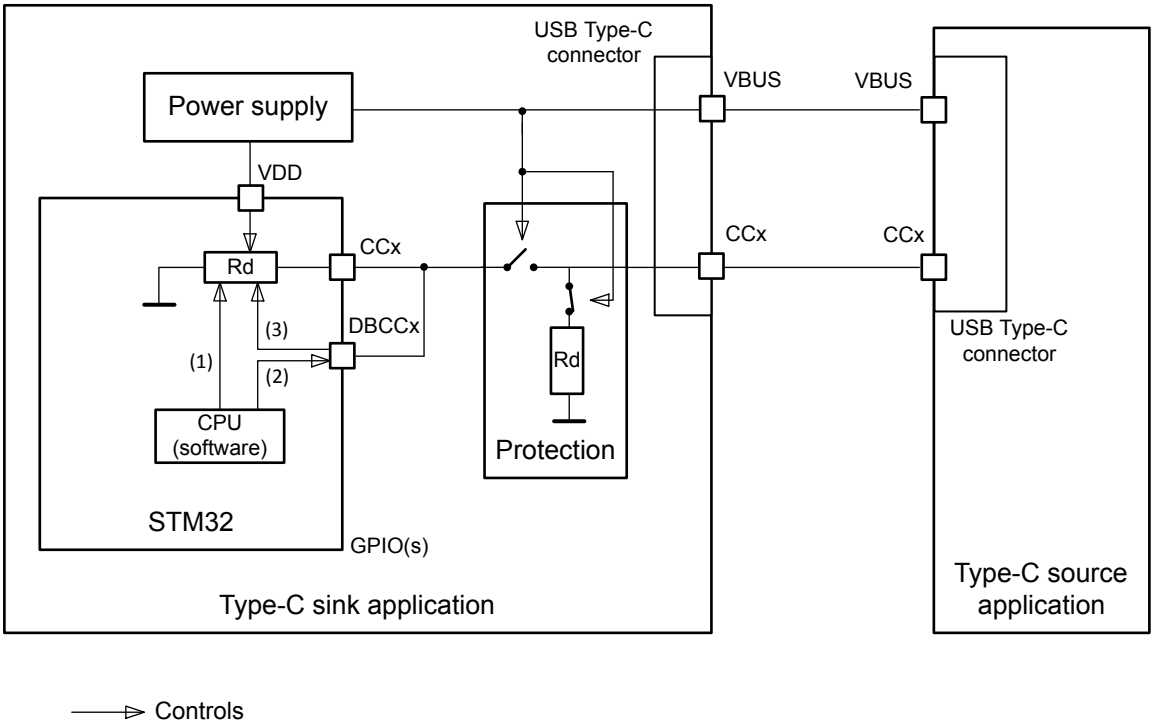
A protection circuit (such as TCPP01-M12) can be placed between the STM32 device and the Type-C connector of the application. When active, it separates the device CCx pins from the CCx lines to protect the device against electrical stress such as ESD on the Type-C connector of the application that may be destructive when no or a non-terminated cable is connected. When deactivated, it connects the device CC pins to the Type-C connector.

Typically, the protection circuit is supplied from the VBUS line. It may be activated/deactivated through either a dedicated command or as function of its power supply. In the latter case, it isolates the CCx pin of the device from the Type-C connector when unpowered (protection active), and it couples the CCx pin of the devices with the Type-C connector when powered (protection inactive or bypass).

For applications supporting *Dead battery* feature, the active protection circuit on a CCx line must expose a Rd = *DB* to the Type-C connector CCx line. Its activation/deactivation must be based on its powering state (VBUS voltage). As soon as the USB Type-C source provides supply/charging voltage on VBUS, the protection circuit is deactivated (its Rd deconnected and the CCx line connected with the device CCx pin). However, as the STM32 device may not yet be supplied at that instant, it must take over the *Dead battery* signaling (expose Rd = *DB* on the CC pin) from the protection circuit. This is why the DBCCx pin must be shorted with the corresponding CCx pin and it cannot be used for other purposes.

The following figure shows a typical application with protection, supporting *Dead battery* feature.

Figure 18. **Protected sink application supporting *Dead battery* feature**



The following table shows *Dead battery* mode exit sequence for a USB Type-C sink application with a protection circuit. The term *connected/isolated* means *CCx pins connected / non-connected with Type-C source CCx lines.* The protection circuit state *active* means *protection activated, Rd = DB of the protection circuit exposed to Type-C source.* The protection circuit state *bypass*means *protection circuit deactivated, not affecting the CC line and connecting the device CCx pins with the Type-C source CCx lines.*

Table 11. **Protected sink application - sequence of exiting *Dead battery* mode**

Sequence	VBUS	VDD	Protection circuit state	Device CC pins/Rd value	Comment
Step 0	0 V	0 V	active	isolated/*DB*	-
Step 1	5 V	0 V	bypass	connected/*DB*	VBUS arrives
Step 2	5 V	3.3 V	bypass	connected/ default Rd	device supply arrives
Step 3	5 V	3.3 V	bypass	connected / as selected by SW	upon write to ANAMODE
Step 4	5 V	3.3 V	bypass, low power	connected / as selected by SW	upon I2C write to protection circuit

The protection circuit of applications not supporting *Dead battery* feature does not incorporate the *DB* pull-down device.

It can be activated/deactivated based on its supply voltage (Figure 19) or by software through a dedicated input (Figure 20 - control path (4)). The latter allows the device to set up, through the ANAMODE bitfield, the desired Rd value before the protection is deactivated. In both cases, the DBCCx lines can be used as I/Os. The following figures show examples of the application topology for either case.

Figure 19. **Protected sink application not supporting *Dead battery* feature - activation through supply**

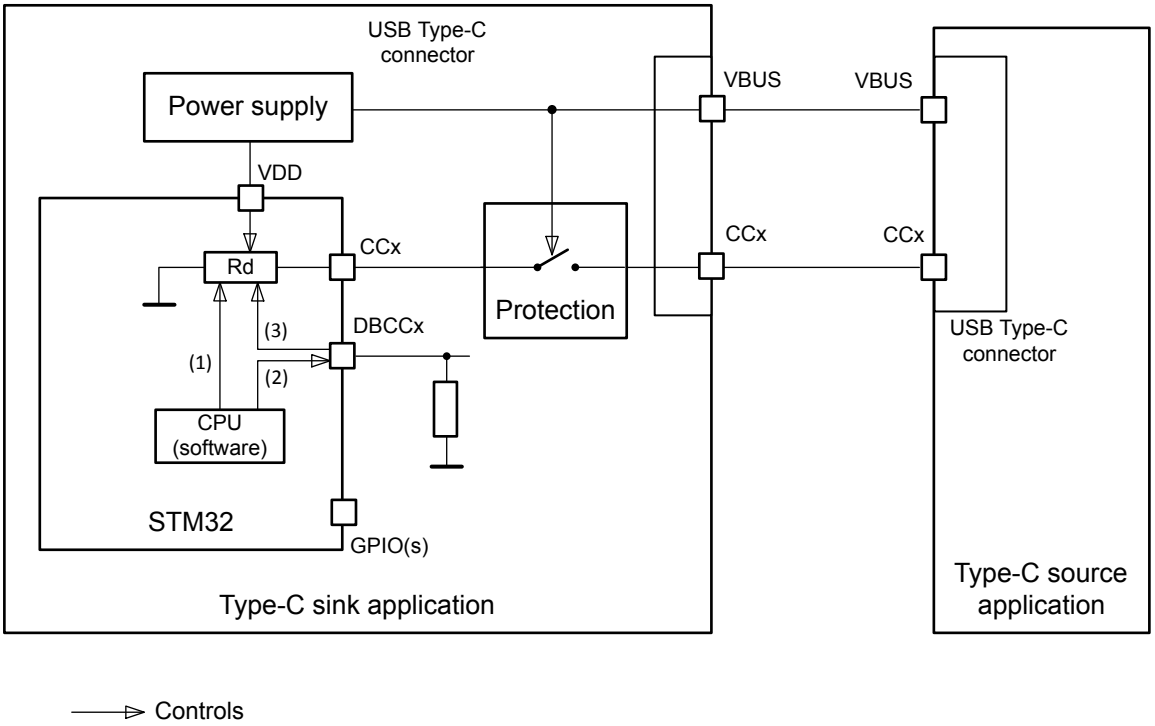
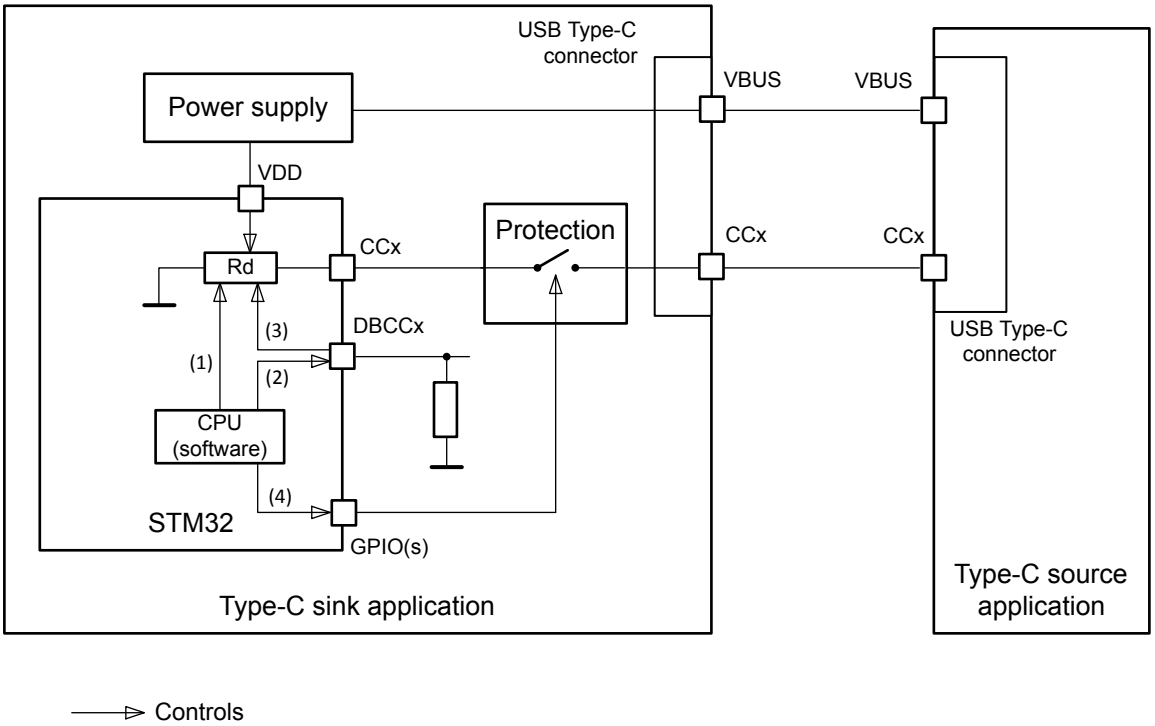


Figure 20. **Protected sink application not supporting *Dead battery* feature - activation through dedicated input**



Summary of application topologies

The following table lists the principal topologies of USB Type-C application with compatible STM32 microcontrollers.

Table 12. Summary of principal Type-C application topologies

Application			DBCCx		Note
Protected[1]	*Dead battery* compliant	Sink/source	Shorted with CCx	Reusable	
No	Yes	Sink	Yes	No	-
No	No	Sink	No	Yes	Application must ensure low level on DBCCx when the device is unpowered.
Yes	Yes	Sink	Yes	No	Protection circuit deactivated when supplied
Yes	No	Sink	No	Yes	Protection circuit deactivated when supplied: the application must ensure low level on DBCCx when the device is unpowered.
					Protection circuit deactivated by software: the default Rd is never exposed to Type-C source.
No	Not applicable	Source	No	Yes	Rp exposed on CCx when the device is powered. The application must ensure low level on DBCCx when the device is unpowered.

1. *Pertains to CCx line*

11.3.2 Sink port

The USB Type-C Power Delivery sink (SNK) port exposes pull-down resistors (Rd) to the CC lines, and it consumes power from the VBUS line (5 V to 20 V and up to 5 A).

From a sink point of view:

Mandatory

- Type-C port asserts Rd (pull-down resistor) on CC lines
- VBUS sensing
- Source detach detection, when VBUS moves outside the vSafe5V range

Optional

- Sink power from VBUS

Optional protection

- OVP as defined by usb.org:
  - In the attach state, a sink should measure the VBUS voltage level.
  - An STM32 general-purpose ADC can perform this measurement.
- Protection and EMI filtering on CC1, CC2, and VBUS lines. See Section 14 Recommendations

The features are summarized in the following table:

Table 13. Sink features

Feature	STM32 peripherals involved	number of STM32 pins	External components or devices	Comments	Signal name
Protocol					
Communication channels CC1 and CC2	UCPD: CC1, CC2	2	-	Mandatory. Able to handle Rd and Rp	CC1, CC2
Dead battery	UCPD: DBCC1, DBCC2	2	-	Handles Rd	DBCC1, DBCC2
VBUS level, vSafe5V, measurement	ADC	1	Resistor divider bridge with or without op-amp for safety purpose	Mandatory only for OVP protection purpose	V_SENSE
Power					
Sink power from VBUS	-	-	DC/DC from VBUS to 3.3 V (VDD)	Optional, LDO, DC/DC, SMPS	-
Extra Power switch	GPIO	1	Power switch	Optional, MOSFET or power switch can be use	SNK_EN
Protection					
CC1 and CC2	-	-	See Section 14 Recommendations	Optional	CC1 and CC2 on Type-C side
VBus	-	-	See Section 14 Recommendations	Optional	VBUS on Type-C side
Software					
Message repetition	TIM	-	-	Used to drive timing repetition 1200 µs et 900 µs	See UM2552 for details
Message transmissions	DMA	-	-	For TX et RX transfer	See UM2552 for details

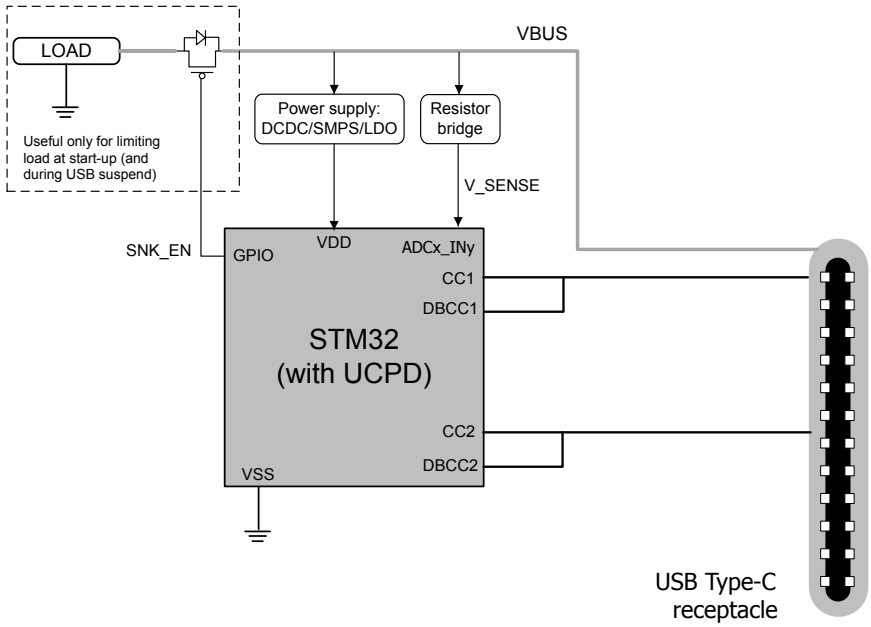
The following architecture schematics explain how to implement various sink modes.

11.3.2.1 *VBUS-powered sink*

From the STM32 point of view, VDD is generated from VBUS. An external LDO, DC/DC converter, or SMPS is used, and an optional power-switch wire on VBUS can power extra load. The SNK_EN GPIO pin controls this optional power-switch.

Regarding the protocol, two dedicated STM32 UCPD pins, DBCC1 and DBCC2, set Rd on the CC1 and CC2 lines. The DBCC lines must be wired to CC lines. No software action is needed, as Rd is present on the CC lines through the DBCC lines, with or without the STM32 power supply (VDD). After STM32 power-up, the USB-PD software stack switches the resistor connection from the DBCC to the CC lines.

Figure 21. Unprotected VBUS-powered (Dead battery) sink connections



Signal description

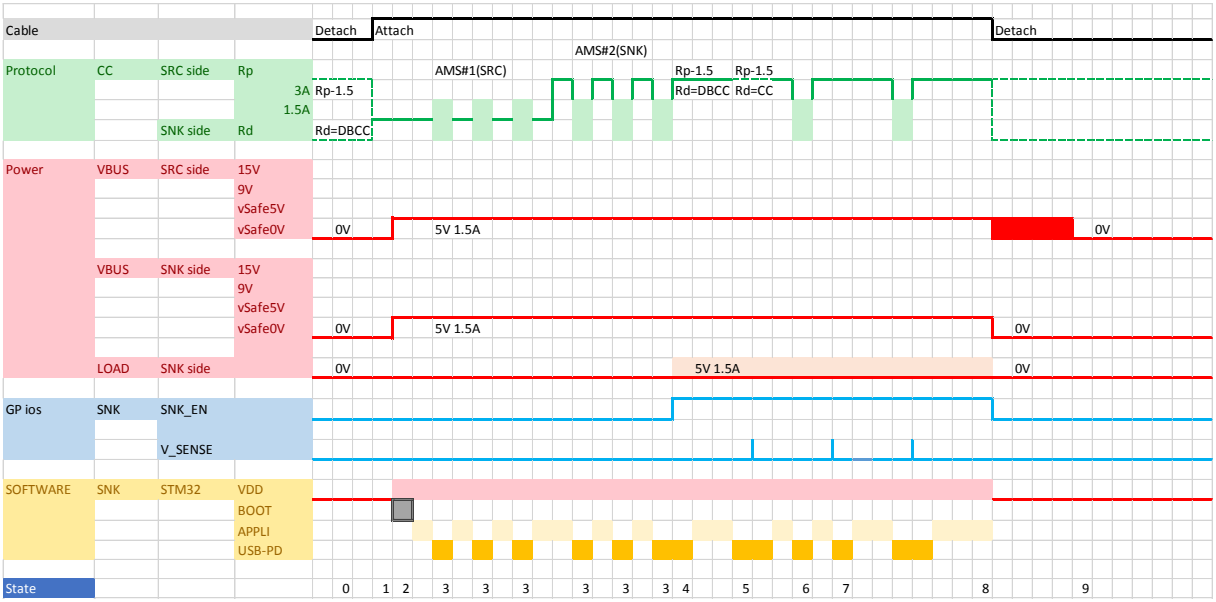
- CC1 and CC2 communication channel signals wired to dedicated Type-C connector pins
- The DBCC1 dead-battery signal is wired to CC1. This handles Rd when the STM32 is not powered via the CC1 line.
- The DBCC2 dead-battery signal is wired to CC2. This handles Rd when the STM32 is not powered via the CC2 line.

Optional:

- V_SENSE wired to an ADC through a resistor divider. VBUS voltage measurement for OVP and safety purposes. The software stack, using the HAL_ADC driver, measures the VBUS voltage level.
- SNK_EN signal GPIO connects and disconnects an optional VBUS load.

Time line

Figure 22. VBUS-powered sink timeline



The states are described below. Actions in italics are GPIO-based (ADC, IO, and so on):

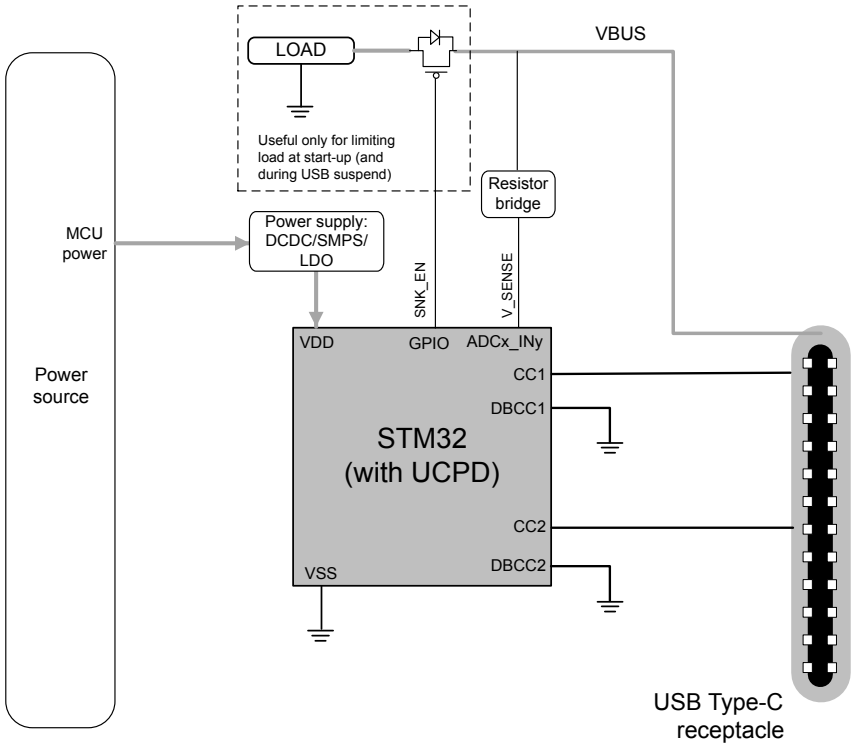
- **State 0**: No connection between equipment
  - Detach state
  - *Rp = 1.5A Rd = 5.1K (DBCC pin)*
- **State 1**: Connect cable; VBUS is in Attach state
- **State 2**: STM32 boot, start application and initialize USB-PD software
- **State 3**: Port partner starts AMS power negotiation
- **State 4**: *USB-PD: use Rd from CC instead of DBCC*
- **State 5**: SNK detects the attachment
- **State 6**: *USB-PD: Enable load using SNK_EN GPIO and a contract is established*
- **State 7**: *USB-PD SW: OVP and safety are looking for V/I VBUS senses*
- **State 8**: Disconnect cable, VBUS is OFF on the sink side
- **State 9**: Source discharges VBUS to vSafe0V

11.3.2.2 *Separately powered sink*

The STM32 device is powered from a separate AC/DC or DC/DC converter, SMPS, LDO, or battery, and not from VBUS. An additional load can optionally be powered from VBUS through a power switch controlled by the SNK_EN GPIO.

Regarding the protocol, the CC1 and CC2 lines set Rd. The DBCC1 and DBCC2 lines must be connect to GND.

Figure 23. SNK external power connections



Signal description

- CC1 and CC2 communication channel signals wired to dedicated Type-C connector pins
- DBCC1 signal wired to GND (as dead-battery mode is not used)
- DBCC2 signal wired to GND (as dead-battery mode is not used)

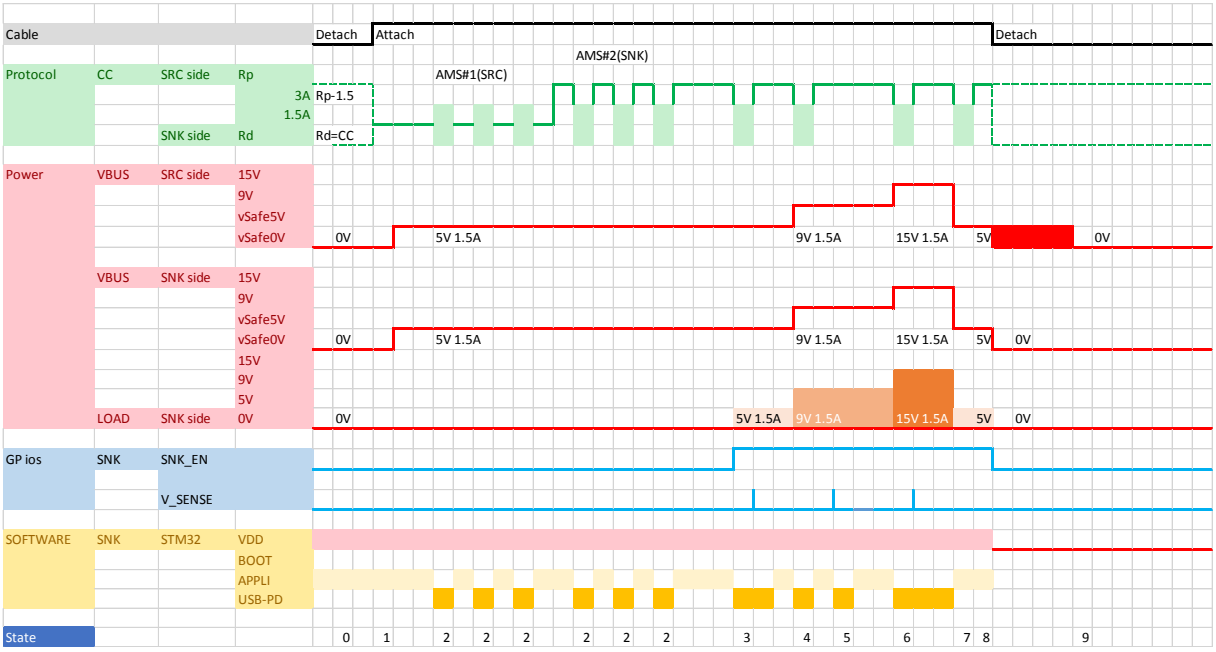
Optional:

- V_SENSE signal wired to an ADC through a resistor divider
- VBUS voltage is measured for OVP and safety purposes
- The software stack, using the HAL_ADC, measures the VBUS voltage level

SNK_EN signal GPIO pin connects and disconnects an optional VBUS load.

Time line

Figure 24. Sink external power time line



The states are described below. Actions in italics are GPIO-based (ADC, IO and so on)

- **State 0**: No connection between equipment
  - Detach state
  - *Rp = 1.5 A Rd = 5.1 K (CC pin)*
- **State 1**: Connect cable. VBUS is in Attach state.
- **State 2**: AMS between SRC and SNK.
- **State 3**: USB-PD: Enable load using SNK_EN GPIO pin.
- **State 4** SNK requests 9 V.
- **State 5**: *USB-PD SW: OVP and safety are looking for V/I VBUS senses*.
- **State 6**: SNK requests 15 V.
- **State 7**: SNK requests 5 V.
- **State 8**: Disconnect cable, VBUS is off on the sink side.
- **State 9**: Source discharge VBUS to vSafe0V.

11.3.3 Source port

The USB Type-C Power Delivery source (SRC) port exposes pull-up resistor (Rp) to the CC lines and it provides power over VBUS (5 V to 20 V and up to 5 A).

From a source point of view:

Mandatory

- Type-C port asserts Rp on CC lines
- Feed power to VBUS
- During detach or communication failure, the source reduces VBUS to vSafe0V.
  An STM32 GP GPIO discharges VBUS using an external MOSFET.

Optional

- An STM32 GP ADC can do these measurements using a shunt or resistor bridge.

Optional protection

- Protection and EMI filtering on CC1, CC2 and V_{BUS} lines. See Section 14 Recommendations.

Source features

The features are summarized in Table 14.

Table 14. Source features

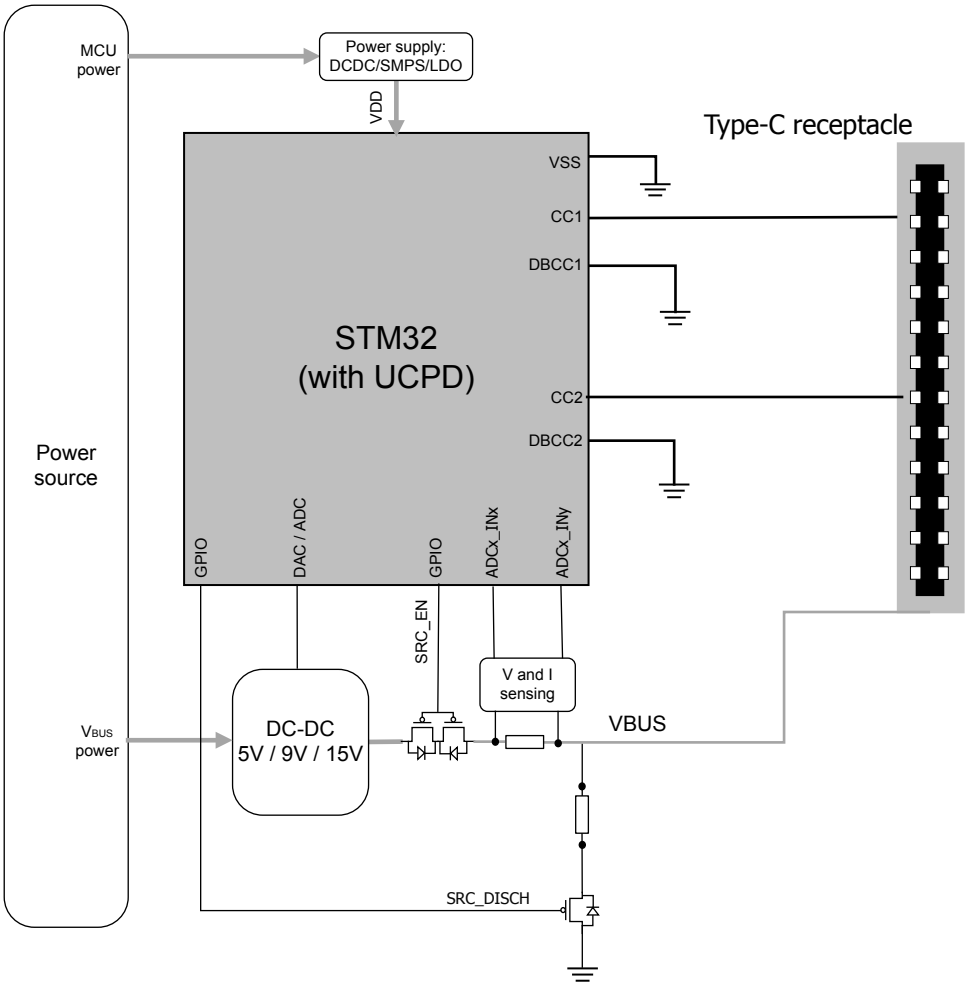
Feature	STM32 Peripherals involved	Number of STM32 pins	External components or devices	Comments	Signal name
Protocol					
CC1 and CC2 communication channels	UCPD: CC1, CC2	2	-	Mandatory	CC1 CC2
Dead Battery support	UCPD: DBCC1, DBCC2	2	-	Mandatory	DBCC1 DBCC1
VBUS level, vSafe0V, measurement	ADC	1	Resistor bridge with or without op-amp for safety purpose	Mandatory(1)	V_SENSE
Power					
Provide power from VBUS	GPIO	1	Power switch	Mandatory, Dual-MOSFET can be used	SRC_EN
Discharge VBUS to vSafe0V	GPIO	1	MOSFET + charge resistors	Mandatory	SRC_DISCH
ISense measurement	ADC	1	Op-amp + shunt resistors	Optional	I_SENSE
CC1 and CC2			See Section 14 Recommendations		CC1 and CC2 on Type-C side
Protection					
VBUS	-	-	See Section 14 Recommendations	-	VBUS on Type-C side
Software					
Message repetition	TIM	-	-	Used to drive timing repetition 1200 µs et 900 µs	See [1] for details
Message transmissions	DMA	-	-	For TX et RX transfer	See [1] for details

1. *For certification purposes, vsafe0V must be checked.*

Figure 25 explains how to handle Source (SRC) mode. From the STM32 point of view, power is provided by an external source such as an AC/DC, DC/DC, SMPS, LDO, or battery.

Rp management is handled by the UCPD software stack. In this case, the DBCC lines must not be wired to the CC1 and CC2 lines. The DBCC1 and DBCC2 pins are wired to GND.

Figure 25. **Source architecture**



Note: The VCONN circuit is not shown in this figure. See Section 13.1 Sourcing power to VBUS
.

Signal description

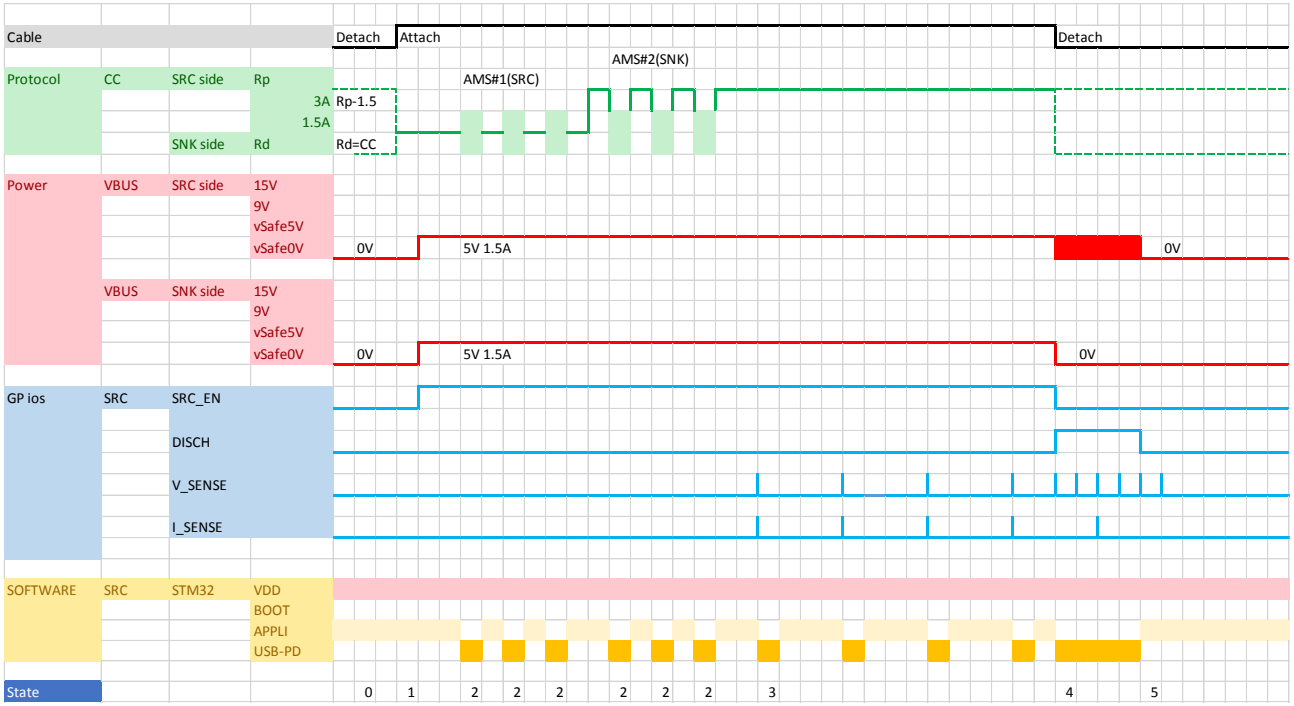
- CC1 and CC2 communication channel signals wired to dedicated Type-C connector pins
- the DBCC1 signal is wired to GND
- the DBCC2 signal is wired to GND

Optional:

- V_SENSE signal wired to an ADC through a resistor divider. VBUS voltage measurement for OVP and safety purposes. Software stack, using the HAL_ADC driver to measure the VBUS voltage level.
- In the case of negative VBUS transitions, for example 15 V to 5 V or 9 V to 5 V, a discharge path can be used before the load switch (controlled by SRC_EN) to reduce the time needed for this transition and to stay in specification.

Time line

Figure 26. SRC (source) mode power timings



The states are described below. Actions in italics are GPIO-based (ADC, IO, and so on):

- **State 0**: No connection between equipment
  - Detach state
  - *Rp = 1.5 A, Rd = 5.1 kΩ (CC pin)*
- **State 1**: Connect cable. VBUS is on
  - Attach state
  - *USB-PD switches on VBUS using the SRC_EN GPIO pin*
  - Capability exchange
- **State 2**: AMS between SRC and SNK
- **State 3**: *USB-PD SW: OVP and safety are looking for V/I VBUS senses*
- **State 4**: Disconnect cable, VBUS is OFF on the sink side
  - *USB-PD initiates VBUS discharge using the DISCH GPIO pin, until VBUS reaches vSafe0V*
- **State 5**: Source VBUS discharged to vSafe0V

11.3.4 Dual-role power port

Dual-role power (DRP) port refers to a USB Power Delivery port that can operate as either a source or a sink. The role of the port is fixed to either source or sink, or may alternate between the two port modes. Initially, when operating as a source, the port also takes the DFP role, and when operating as a sink, the port takes the UFP role. The port role may be changed dynamically to reverse either power or data roles.

From a dual-role power port point of view:

Mandatory

- Type-C port asserts Rp on CC lines when in source mode
- Type-C port assert Rd on CC lines when in sink mode
- Feed power to VBUS
- During detach or communication failure, the source takes VBUS down to vSafe0V
  - An STM32 GP GPIO discharges VBUS using an external MOS

Optional

- Measure VBUS voltage and current values
  - A STM32 GP ADC can do this measurement using a shunt, or a resistor bridge
- Get power from VBUS
- Source 'detach' detection, when VBUS moves outside vSafe5V range
- Manage fast role swap (FRS) protocol. (USB-PD 3.0 only)

Optional protection

- Protection and EMI filtering on CC1, CC2 and VBUS lines. See Section 14 Recommendations.

Features

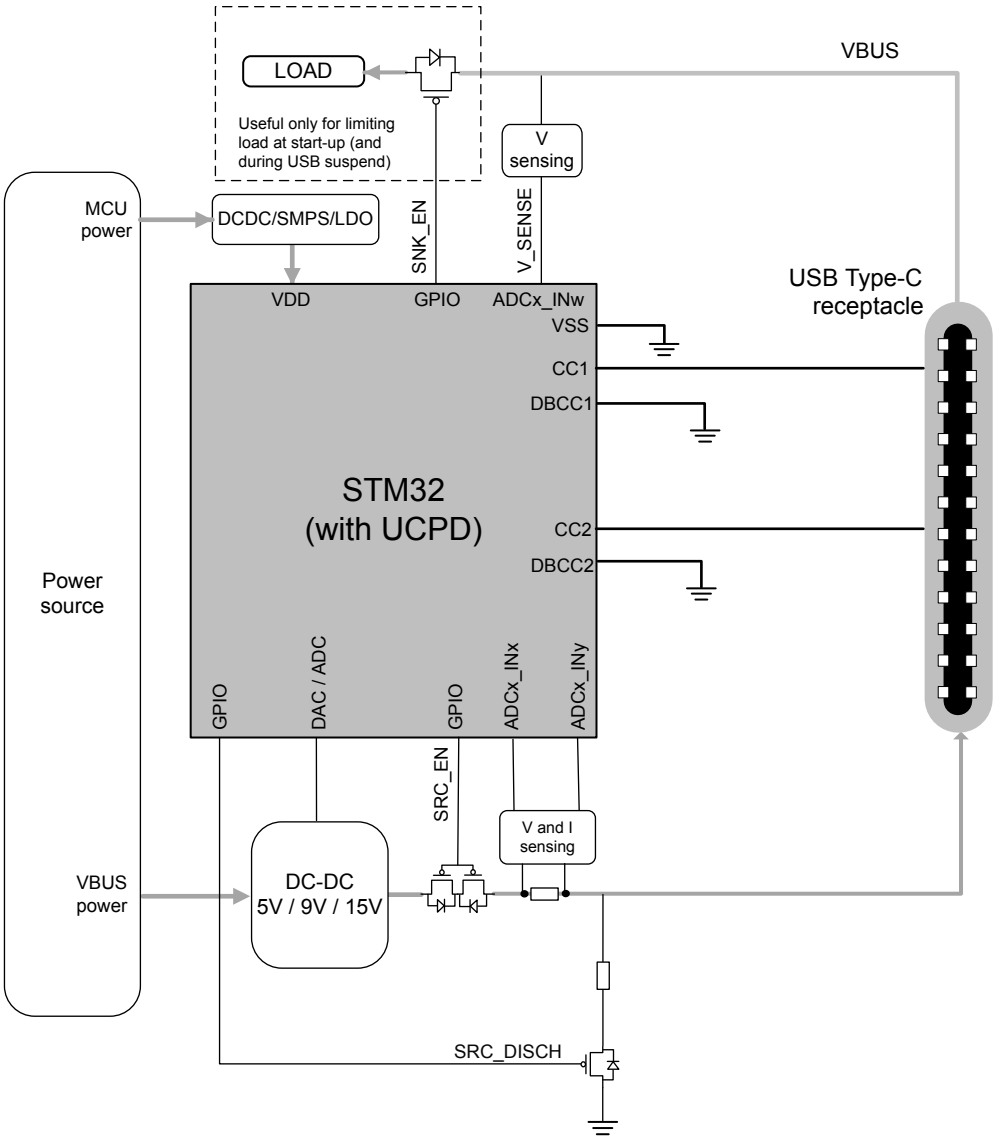
The features are summarized in Table 15:

Table 15. Dual-role power port features

Feature	STM32 Peripherals involved	Number of STM32 pins	External components or devices	Comments	Signal name
Protocol					
CC1 and CC2 communication channels	UCPD: CC1, CC2	2	-	Mandatory Able to handle Rd & Rp	CC1 CC2
Dead Battery	UCPD: DBCC1, DBCC2	2	-	Mandatory Wire to GND	DBCC1 DBCC1
VBUS Level, vSafe0V, vSafe5V , measurements	ADC	1	Resistor divider bridge with or without op-Amp for safety purpose	Mandatory for OVP protection purpose	V_SENSE
Fast Role Swap	UCPD: FRSTX1, FRSTX2	2	MOS to drive CC lines to GND	Mandatory	FRSTX1 FRSTX2
On Power level	-	-	-	-	-
Provide power from VBUS	GPIO	1	Power switch	Mandatory, MOS can be use	SRC_EN
Extra Power switch	GPIO	-	Power switch	Optional, MOS can be use	SNK_EN
Discharge VBUS to vSafe0V	GPIO	1	MOS + charge Resistors	Mandatory	SRC_DISCH
ISense measurement	ADC	1	OpAmp + shunt Resistors	Optional	I_SENSE
Protection					
CC1 and CC2	-	-	See chapter xxx	Optional	CC1 and CC2 on Type-C side
VBUS	-	-	See chapter xxx	Optional	VBUS on Type-C side
Software					
same as previous	-	-	-	-	-

Figure 27 shows the connections used in DRP mode.

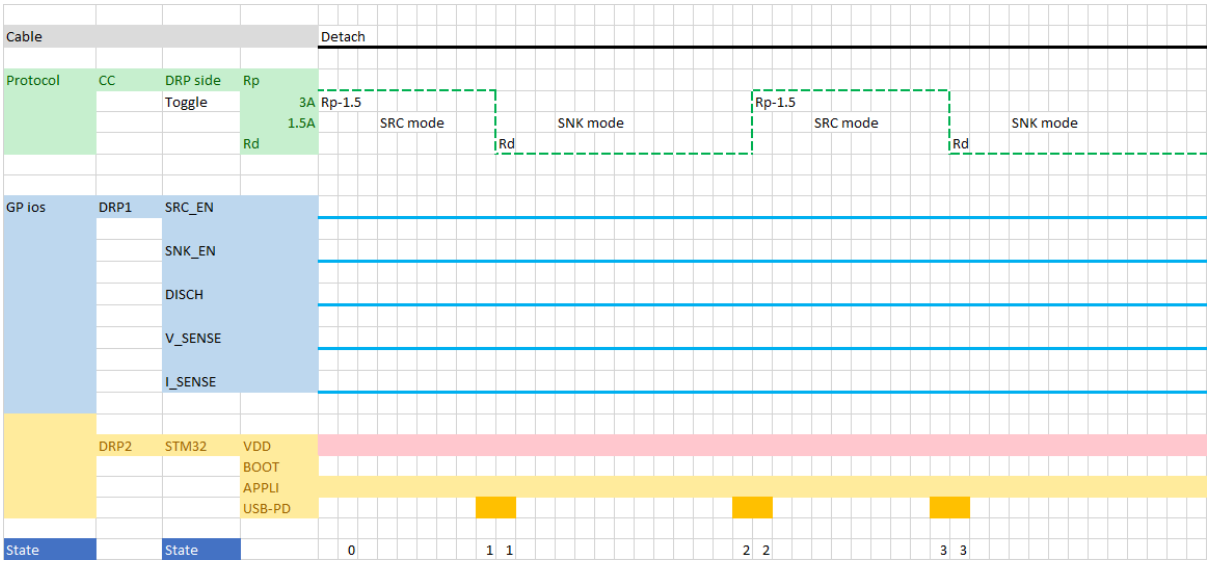
Figure 27. DRP connections



Note: the VCONN circuit is not shown in this figure. See Section 13.1 Sourcing power to VBUS.
The signal descriptions are given in Section 11.3.2 Sink port and Section 11.3.3 Source port.

Time line

Figure 28. DRP with FRS mode time line example



The steps in italics are based on GPIOs (ADC, IO, and so on).

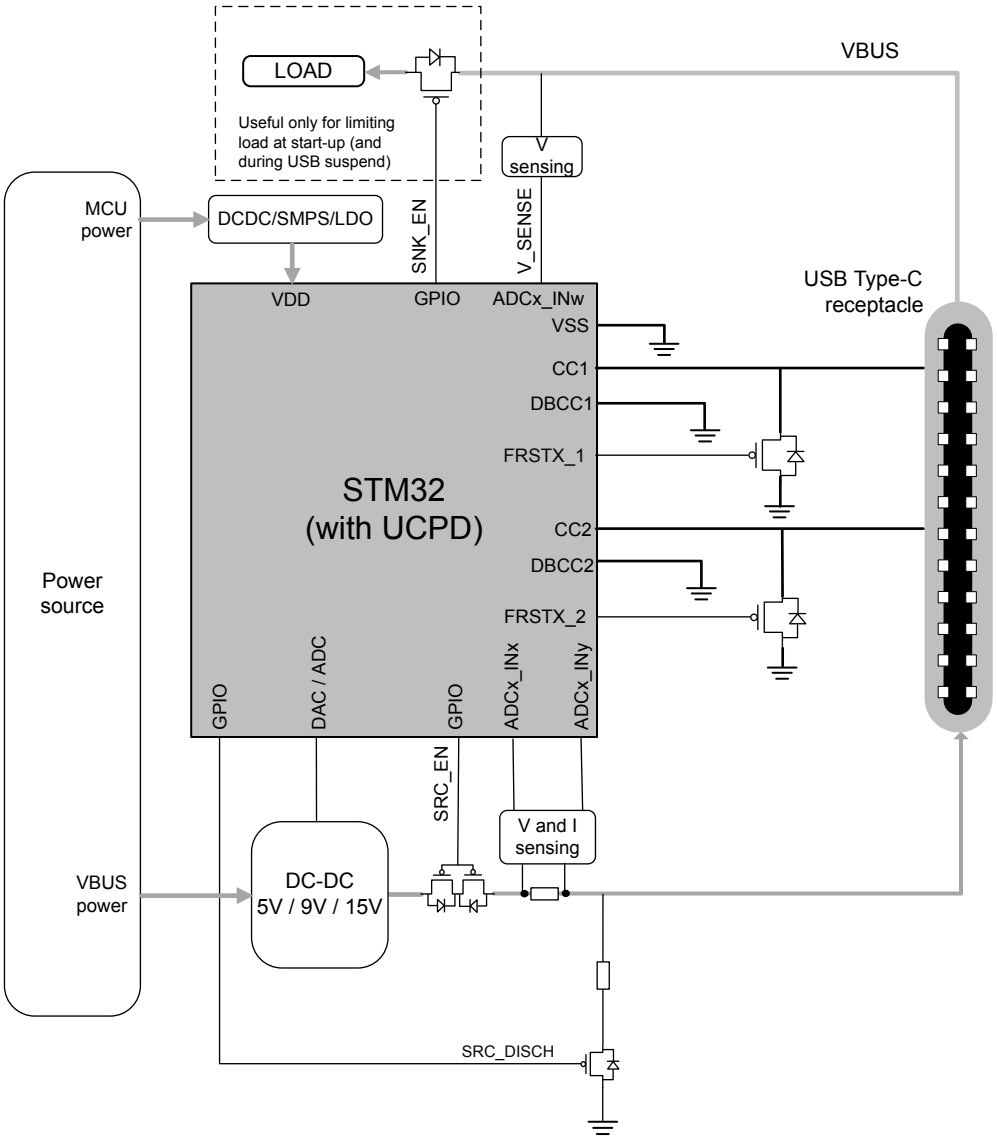
- **State 0**: No connection between equipment
  - Detach state
  - *DRP = SRC role Rp = 1.5 A (CC pin)*
- **State 1**: USB-PD stack decide to move from SRC to SNK role
  - *DRP = SNK role Rd = 5.1K (CC pin)*
- **State 2**: USB-PD stack decide to move from SNK to SRC role
  - *DRP = SRC role Rp = 1.5A (CC pin)*
- **State 3**: USB-PD stack decide to move from SRC to SNK role
  - *DRP = SNK role Rd = 5.1K (CC pin)*

11.3.5 Dual-role power port with FRS

In this configuration, the STM32 device is supplied from a separate source such as an AC/DC or DC/DC converter, SMPS, LDO, or battery. The UCPD peripheral handles Rp and Rd through software. The power role, source or sink, can be changed on-the-fly without any cable disconnect when both devices are DRP ports.

Fast role swap (FRS) function allows any source with sudden power loss (for example mains power) to signal the condition to a sink with fast role swap capability far more rapidly than without FRS. As FRS signaling/detection works during messaging and regardless of the collision control, it takes no longer than 50 µs. Once the sink detects the FRS signaling, it prepares to detect the VBUS level drop. Then it switches its role to SRC, taking over the VBUS drive within a delay (for example 150 µs) specified by the FRS procedure.

Figure 29. DRP with FRS VBUS = 5 V / 9 V / 15 V connections



Note that the VCONN circuit is not shown in this figure. See Section 13.1 Sourcing power to VBUS.

Signal description

- The CC1 and CC2 communication channel signals wired to dedicated Type-C connector pins
- The DBCC1 signal is wired to GND.
- The DBCC2 signal is wired to GND.
- The SRC_EN signal GPIO pin is used to switch-on VBUS using an external MOSFET or power switch.
- The SRC_DISCH signal GPIO pin initiates the discharge of VBUS on detach. An external MOSFET can be used.
- The FRSTX1 and FRSTX2 fast role swap signals are wired to external MOSFETs to drive the CC lines.
- The V_SENSE signal is wired to an ADC through a resistor divider. The VBUS voltage measurement for OVP and safety purpose. The software stack, using the HAL_ADC driver, measures the VBUS voltage level.
- The I_SENSE signal is wired to an ADC through a resistor shunt. VBUS current measurement for safety purposes. The software stack, using the HAL_ADC driver, measures the VBUS current level.
- The SNK_EN signal GPIO pin is used to connect and disconnect an optional VBUS load.

Time line

Figure 30. DRP with FRS - time line example

The steps in italics are based on GPIOs (ADC, IO, and so on)

- **State 0**: No connection between equipment
  - Detach state
  - *Rp = 1.5A Rd = 5.1K (CC pin)*
- **State 1**: Connect cable
  - *VBUS is on DRP1 set SRC_EN GPIO pin*
- **State 2**: Capabilitiy exchanges
  - DRP2 switches the on load on V_{BUS} using the SNK_EN GPIO pin
- **State 3**: *FRSTX (fast role swap) start*
- **State 4**: DRP1 moves V_{BUS} to vSafe0V
- **State 5**: The DISXH GPIO pin initiates the DRP1 discharge
- **State 6**: End of V_{BUS} discharge
- **State 7**: Role swap between DRP1 and DRP2
- **State 8**: *DRP2 enables V_{BUS} using the SRC_EN GPIO pin*
- **State 9**: *DRP1 uses the SNK_EN GPIO pin on the V_{BUS} load ON*
- **State 10**: Disconnect cable
- **State 11**: End of discharge

12 Type-C with Power Delivery using a general-purpose peripheral

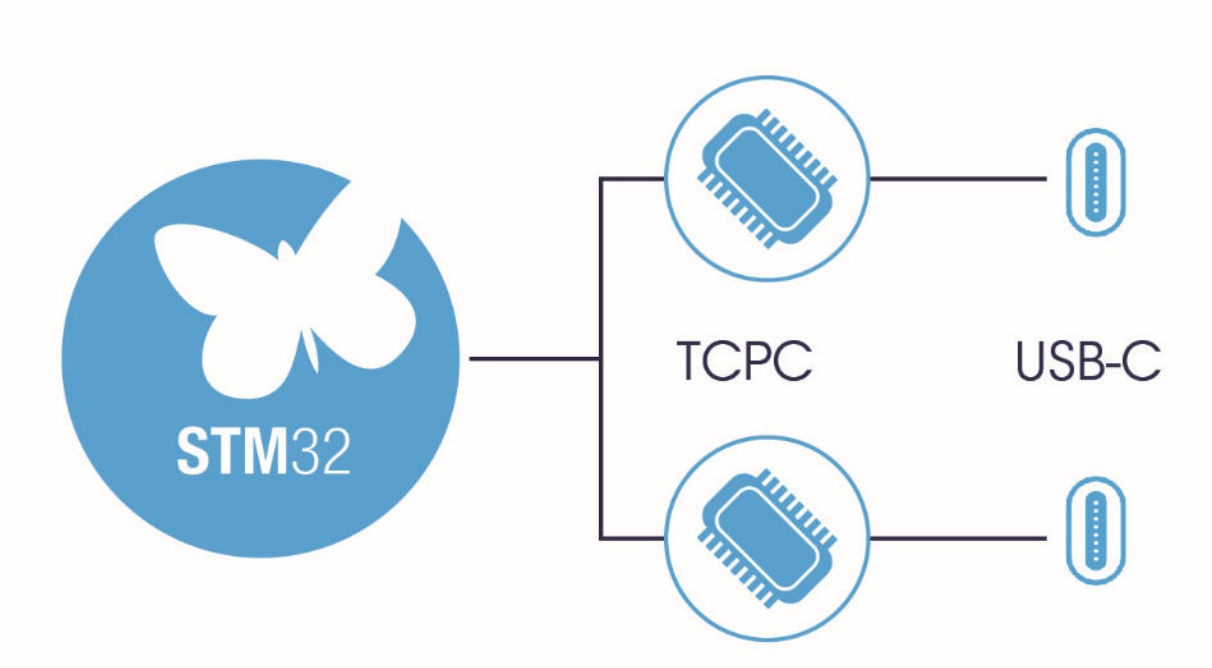
This chapter may not fully apply to STM32 MPU products. Refer to Section 9 Product offer for their specificities.

12.1 Software overview

The software architecture is the same as that described in Section 11.1 STM32 MCU software overview.

12.2 Hardware overview

Figure 31. Hardware view for Type-C Power Delivery with a general-purpose peripheral



Using a general-purpose peripheral, the TCPM/TCPC interfaces are a convenient way of handling USB Power Delivery. STM32 MCUs and STM32 MPUs using a communication bus can handle all TCPM/TCPC companion chips.

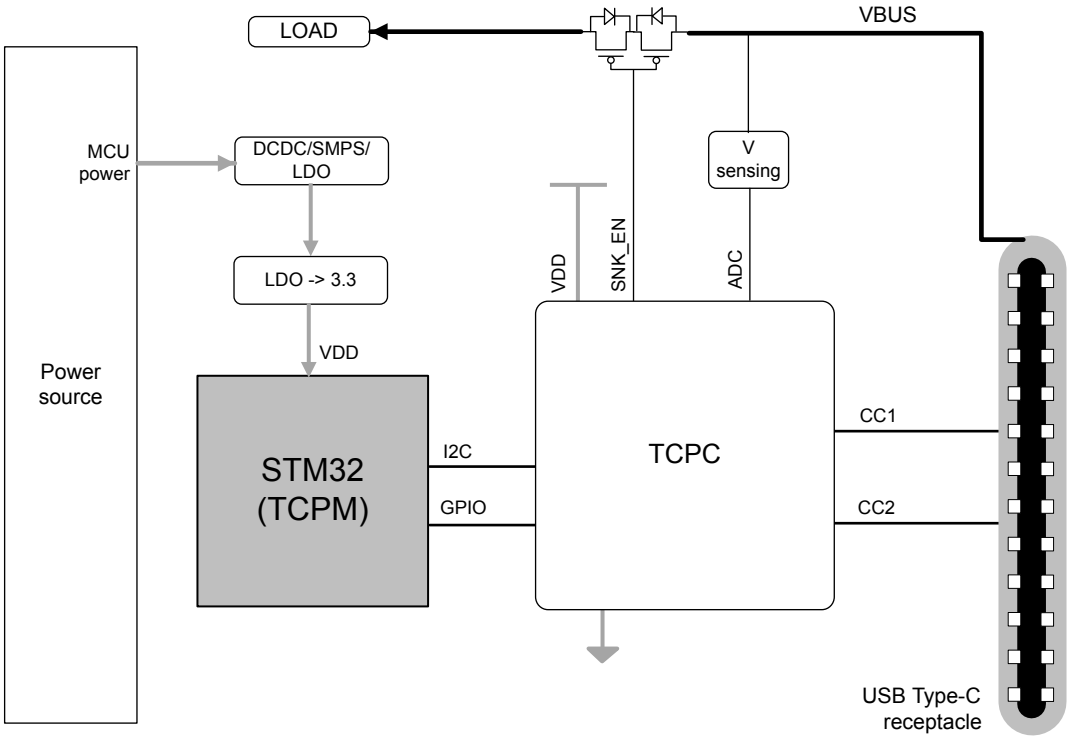
Usually the I2C, SPI or GPIOs are used to handle communication messages and exceptions.

12.2.1 Sink port using TCPM/TCPC interface

In sink (SNK) mode, the Type-C port must expose Rd (pull-down resistor) on CC lines and takes power from VBUS. The sink detects source attachment when VBUS reaches vSafe5V. Detection requires an ADC for example.

The STM32 communicates with the TCPM/TCPC interface, typically using the I2C bus. In some cases an SPI, ADC, DAC, or GPIO completes the communication between the STM32 general-purpose MCU and the TCPM/TCPC external component.

Figure 32. Sink port using TCPM/TCPC interface

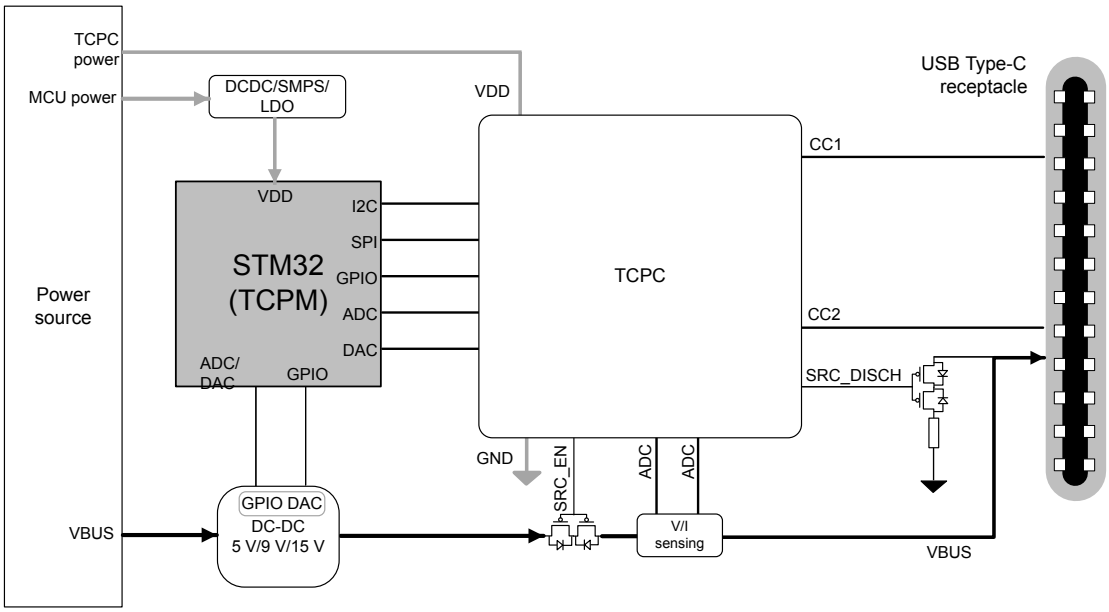


12.2.2 Source port using TCPM/TCPC interface

In source (SRC) mode, the Type-C port must expose Rp (pull-up resistor) to the CC lines and provide power through VBUS. During detach or communications failures, the source must reduce VBUS to vSafe0V. This means that a device must discharge VBUS.

The STM32 (acting as TCPM) usually communicates with TCPM/TCPC interfaces using the I2C bus. In some cases an SPI, ADC, DAC, or a GPIO complete the communication between the STM32 general-purpose MCU and TCPM/TCPC external components.

Figure 33. Source mode using TCPM/TCPC interface

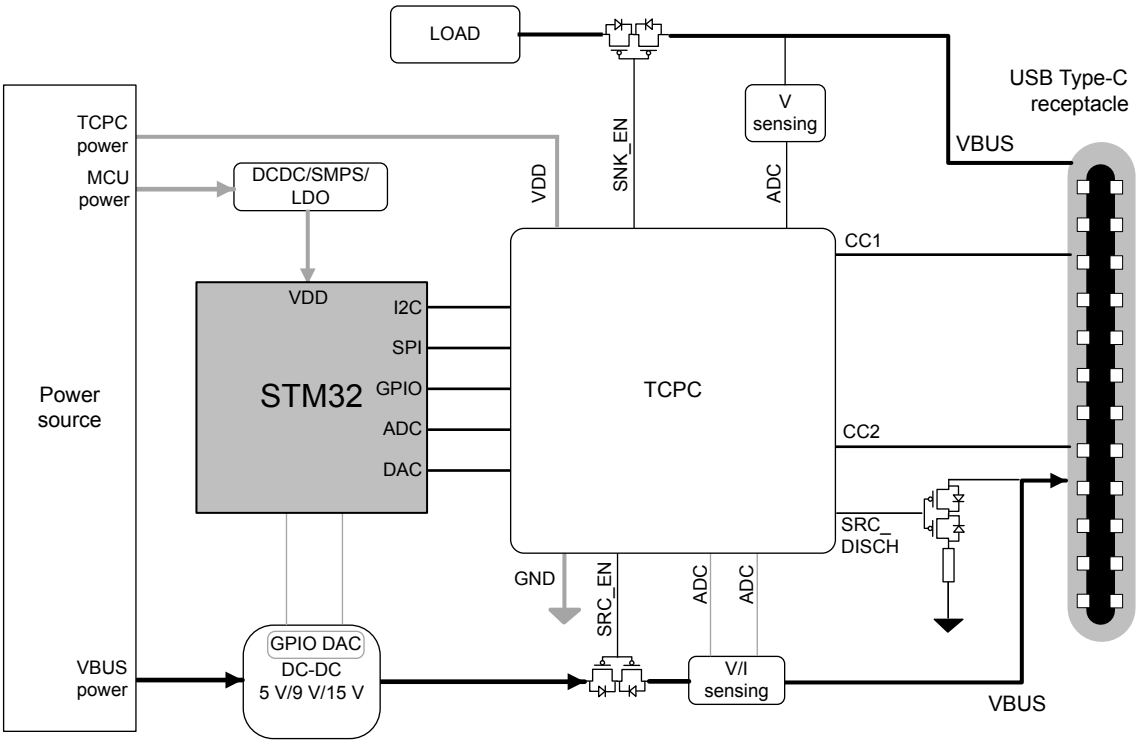


12.2.3 Dual-role power port using TCPM/TCPC interface

A dual-role power (DRP) port can operate as either a source (SRC) or a sink (SNK). The role of the port can be fixed to either source or sink, or it can alternate between the two port states. Initially when operating as a source, the port also takes role of a downstream facing port (DFP), and when operating as a sink, the port takes the role of an upstream facing port (UFP). The port role may change dynamically to reverse either power or data roles.

The STM32 usually communicates with the TCPM/TCPC interface using the I^2C bus. In some cases, an SPI, ADC, DAC, or GPIO completes communications between the STM32 general-purpose MCU and the TCPM/TCPC external component.

Figure 34. Dual-role power port using TCPM/TCPC interface



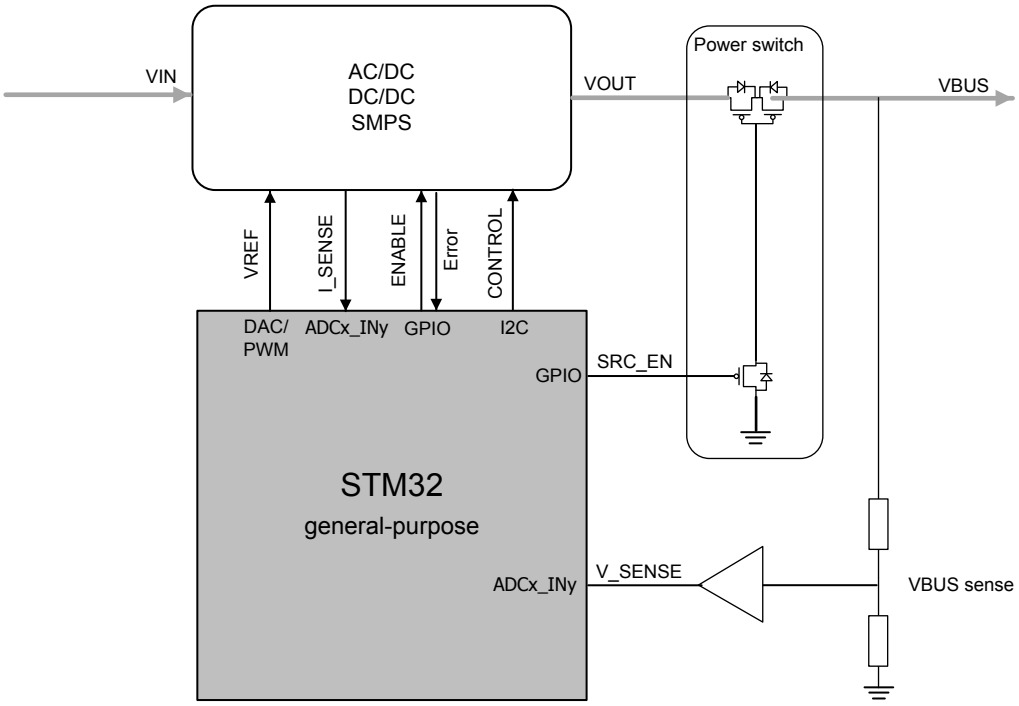
13 Dedicated architecture proposals and solutions

This chapter may not fully apply to STM32 MPU products. Refer to Section 9 Product offer for their specificities.

13.1 Sourcing power to VBUS

SRC port and DRP acting as Power Delivery source provide power to the VBUS line. Commonly used power stages include DC/DC converter, AC/DC converter, and switched-mode power supply (SMPS), with or without a battery. A power switch connects their output (VOUT) to the VBUS line. The general-purpose STM32 ADC, DAC, GPIO, and I2C peripherals allow flexible and scalable power stage control, as shown in the following figure.

Figure 35. Sourcing power to VBUS



Signal description

- ADC: VBUS voltage and current measurement
- GPIO: power switch control, power stage enable, error sensing
- PWM or DAC: voltage reference to the power stage
- I2C: digital control of a power stage with I^2C-bus.

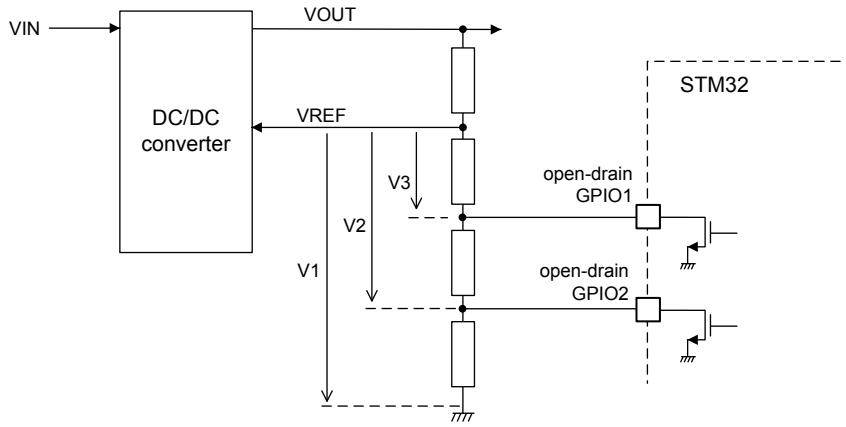
In a STM32G0 implementation, the DC/DC converter is driven by a PWM generated with a timer (available in the STM32,). The aim is to determine the PWM corresponding to the requested voltage. An iteration algorithm estimates the target PWM, and a voltage measurement confirms whether the expected value is reached.

13.2 DC/DC output control with GPIOs

Control through a resistor bridge switched with GPIOs

The VREF line voltage is set with a resistor bridge dividing the VOUT line voltage. The division ratio is switched to the desired value with open-drain GPIOs, as shown in the following figure.

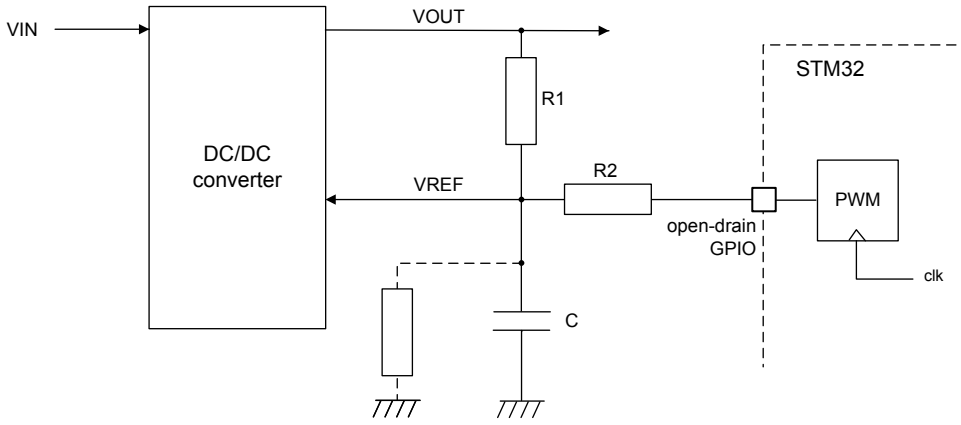
Figure 36. Setting V_{Ref} with a switched resistor bridge



Control with a GPIO acting as a PWM output

The VREF line voltage is set with a resistor bridge R1/R2 dividing the VOUT line voltage, and with an open-drain PWM GPIO output connecting the bottom of the resistor bridge to ground during a portion of time defined with the duty cycle. The voltage in the middle point of the resistor bridge is smoothed to its mean level with a capacitor that forms, with the resistors of the resistor bridge, a low-pass RC filter. Varying the PWM duty cycle varies the VOUT line voltage.

Figure 37. Setting V_{Ref} with a PWM GPIO



Control with a GPIO acting as a DAC output

The VREF line voltage can be driven by an STM32 DAC output.

13.3 Applying V_{CONN} on CC lines

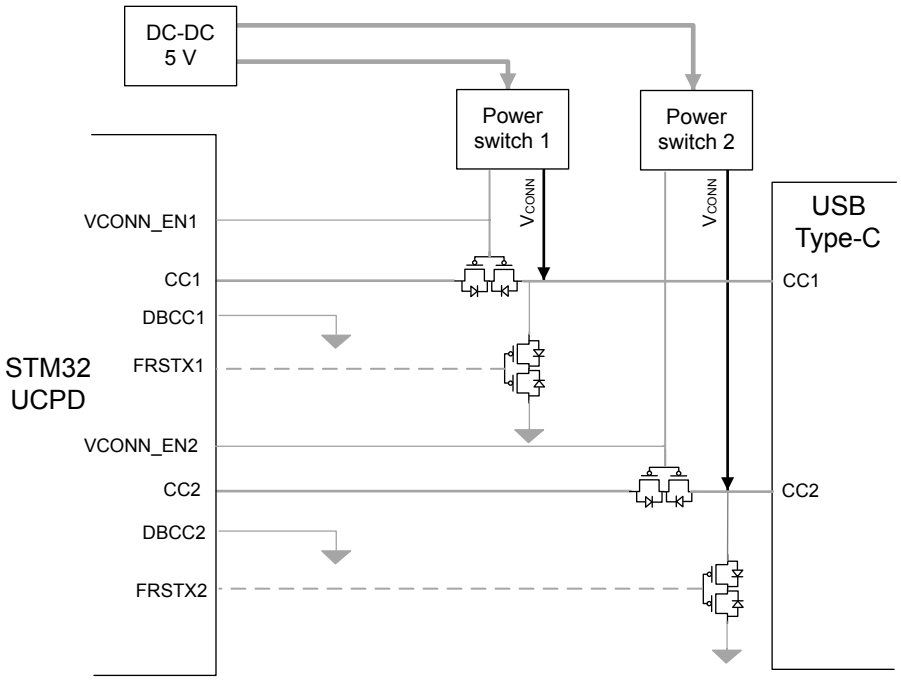
An SRC port or a DRP playing the role of source must support VCONN function in the following cases:

- to supply or draw more than 3 A
- to support USB3

A single V_{CONN} voltage generator is present in the system. Two power switches apply the V_{CONN} (5 V) to either the CC1 or CC2 pin, and simultaneously, two MOSFETs isolate the STM32 UCPD CC1 and CC2 pins from the CC lines. Two FRS commutation MOSFETs discharge the CC lines when the power switches stop applying V_{CONN} to the CC lines.

This implies the use of at least two GPIOs to control VCONN_EN1 and VCONN_EN2, as shown in the following figure.

Figure 38. Applying V_{CONN} on CC lines



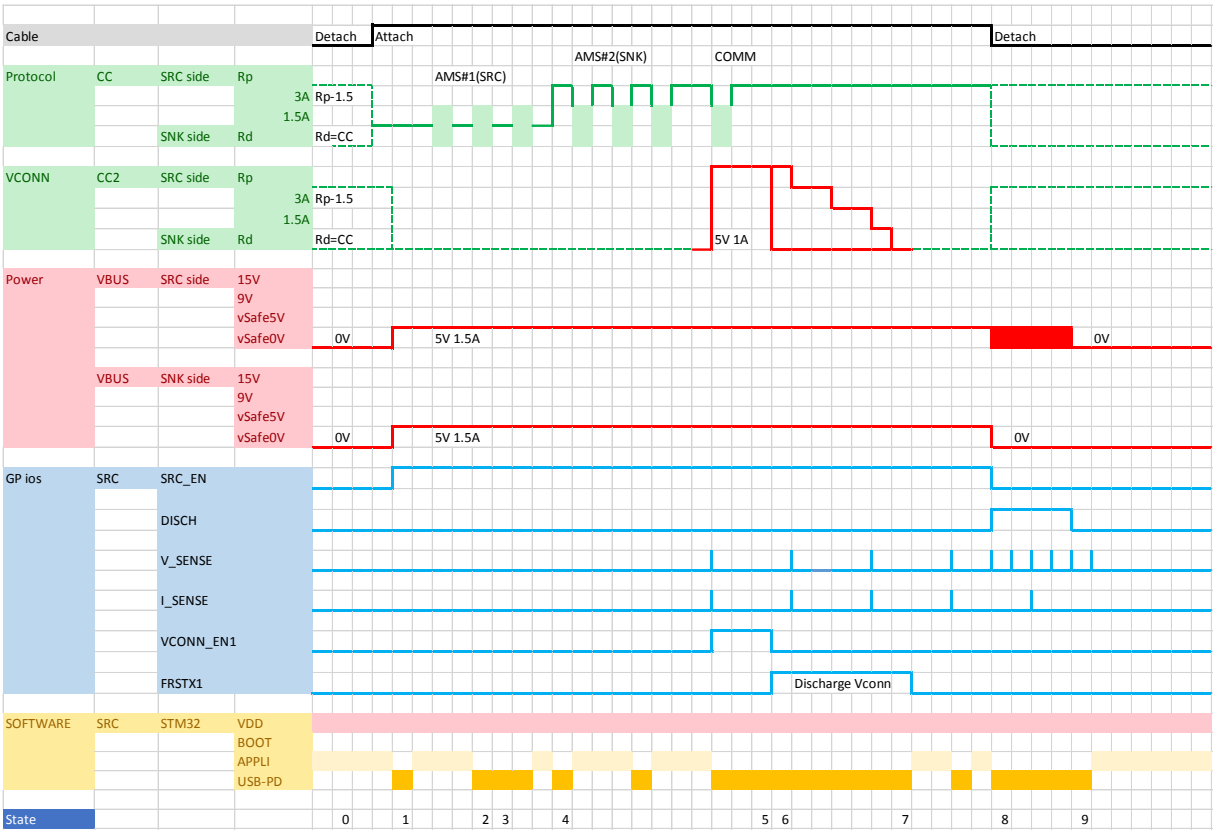
Signal description

Two GPIOs (shown as VCONN_EN1 and VCONN_EN2 in the figure) control the switch to apply V_{CONN} to the CC lines and the simultaneous isolation of the STM32 CC pins from the CC lines.

For software details, see [1].

13.3.1 Time line

Figure 39. **Applying V_{CONN} - time line example**



The sequence is as follows, where actions in italics are based on GPIOs (ADC, IO, and so on):

- **State 0**: No connection between equipment
  - Detach state
  - *Rp = 1.5A Rd = 5.1K (CC pin)*
- **State 1**: Connect cable. VBUS is turned on using the SRC_EN GPIO. Attach state.
  - *USB-PD switch on VBUS using SRC_EN GPIO pin*
  - capabilities exchanged
- **State 2**: Request VCONN ON
- **State 3**: Enable VCONN using VCONN_EN1/2 GPIOs
- **State 4**: *USB-PD SW: OVP and safety are looking for V/I VBUS senses*
- **State 5**: Request VCONN ON
- **State 6**: Disable VCONN using VCONN_EN1/2 GPIOs
  - *Start discharging CC1/2 line using FRSTX pin or a GPIO*
- **State 7**: Disconnect cable, VBUS is OFF on the sink side
  - *USB Power Delivery uses the DISCH GPIO pin to initiate the VBUS discharge until the VBUS voltage reaches vSafe0V*
- **State 8**: The VBUS voltage reaches vSafe0V

13.4 FRS signalling

FRS signaling is only required for Type-C DRP role swapping. Only a DRP operating as a power source optionally sends FRS signals on power-outage detection.

FRS signaling (TX): UCPD peripheral requires external hardware to pull the CC line strongly to GND

- This implies two external NMOS transistors, controlled by the STM32 UCPD peripheral
- One per CC line, controlled with GPIO set to the corresponding FRSTX1 or FRSTX2 AF

FRS detection (RX): The detection of FRS signaling is internal. It can be enabled by software.

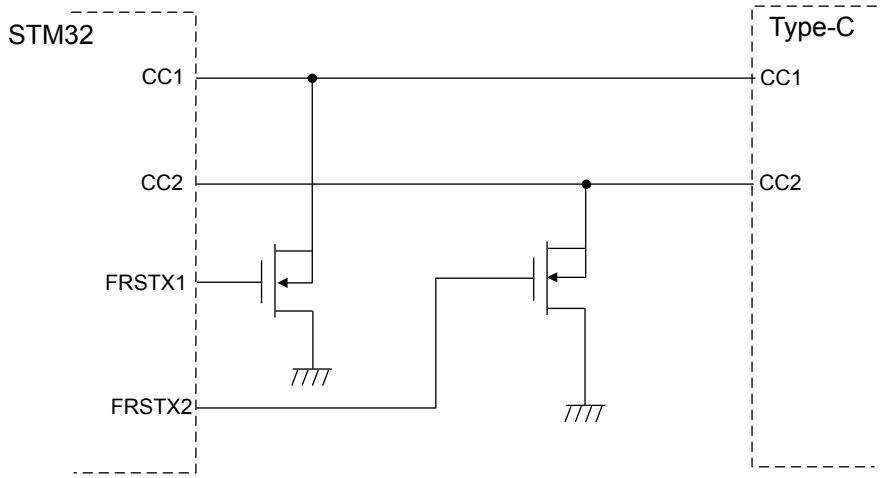
- Software uses a UCPD interruption.

The UCPD peripheral provides a control bit (FRSTX) that is available through alternate-function multiplexing. It is only written to 1 to start the 'FRS signaling' condition. The condition is auto-cleared in order to respect the required timing. See the relevant STM32 MCU or MPU product datasheet for further details. This behavior is introduced in Power Delivery 3.0, is optional, and only applies to DRP roles. It allows a fast solution to swap power roles for a source that loses its ability to supply power.

A DRP in source (SRC) mode signals 'FRS' as an alert condition in order to swap power roles (that is, the VBUS source) as quickly as possible. Typically, this is useful in the absence of a local battery.

When the VCONN feature is used, FRSTX1 and FRSTX2 discharge the CC1 and CC2 lines through MOSFETs.

Figure 40. Fast role-swap DRP mode circuit



13.5 Monitoring VBUS voltage and current

Protection and safety

A DC/DC converter circuit, such as the L7987, is used to generate VBUS and VCONN, and includes built-in OTP / OVP / OCP generation. These errors can be handled in software at the user application level for safety purposes. To do this, the DC/DC fault output signal can be routed to EXTI on the STM32 side.

PD protocol

A SNK port or a DRP in the role of power sink measures the VBUS level to handle REQUEST_ACCEPT / PS_RDY / DETACH protocol messages on the software side. For this purpose, one ADC is required on the STM32 side.

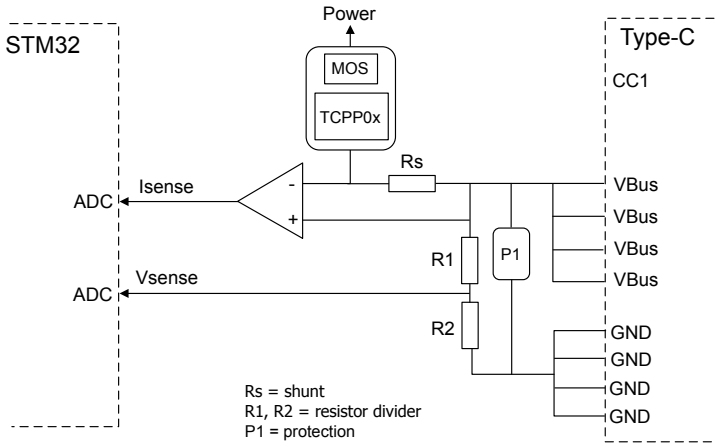
A SRC port or a DRP in the role of power source provides power to the VBUS and keeps its voltage within the specified target (through monitoring it and controlling the DC/DC converter), for PDO or APOD uses cases.

Method

To measure optional VBUS current, use a low resistance shunt. To measure VBUS voltage, use a basic resistor bridge. Optionally add an operational amplifier for OVP and safety purposes.

Note: TSC1641, TSC2011 and TSC2012 precision bidirectional current sense amplifier can be used. See datasheets on www.st.com.

Figure 41. VBUS voltage and current monitoring circuit



Note: Extra protection (P1 in Figure 41) in can be added on Isense and Vsense. See Section 14 Recommendations.

13.6 Dual-role power port

Dual-role power port application examples based on STM32G0 and TCPP03 STMicroelectronics part numbers are given be in Figure 42 and Table 16.

The NUCLEO-G071RB and X-NUCLEO-DRP1M1 can be used for fast prototyping.

Figure 42. STM32G0 pin/resource assignments

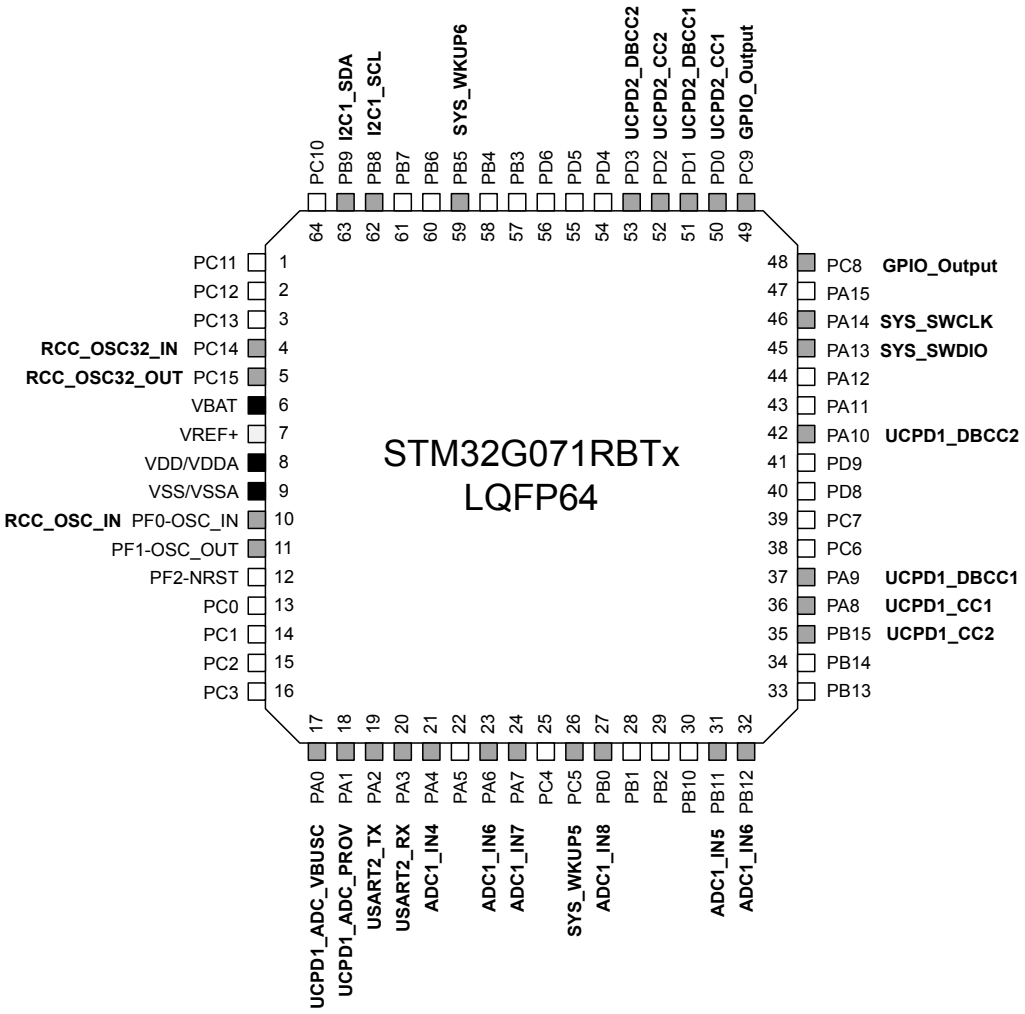


Table 16. STM32G0 resources

Item	X-NUCLEO G0-1 Address: 0x68	X-NUCLEO G0-2 Address: 0x6A	STM32G0 IOs UCPD1 left - UCPD2 right		Comment
I2C1 SCL	CN10-3(1)		PB8		-
I2C1 SDA	CN10-5(1)		PB9		-
CC1	C10-23/C10-17(1)	CN7-9(1)	PA8	PD0	-
CC2	C10-26/C10-27(1)	CN7-4(1)	PB15	PD2	-
GPIO FIgn	CN10-37(1)	CN10-29(1)	PC5	PB5	Wake-up GPIO
ADC Vbusc	CN7-28(1)	CN10-13(1)	PA0/IN0	PA6/IN6	-
ADC Prov	CN7-30(2)	CN10-15(2)	PA1/IN1	PA7/IN7	-
ADC Cons	CN7-32(2)	CN10-17(2)	PA4/IN4	PB0/IN8	-
ADC Isense	CN7-36(2)	CN10-38(2)	PB11/IN15	PB12/IN16	-
ENABLE	CN10-2	CN10-1	PC8	PC9	Vddl via GPIO
D+	CN10-12	-	PA12	N/A	Only 1 port on ST32G0
D-	CN10-14	-	PA11	N/A	
CC1 DB	CN10-21(2)	CN7-10(2)	PA9	PD1	-
CC2 DB	CN10-33(2)	CN7-11(2)	PA10	PD3	-
USART2	ST-link part(3)		PA2-PA3		For traces
LED	CN10-11(3)		PA5		For debug

1. *Mandatory*
2. *Optional*
3. *For debug purposes*

14 Recommendations

14.1 ESD/EOS protection devices for USB Type-C®

Dedicated ESD and EOS protection can be used on:

- V_{BUS} power delivery signals
- D+/D-
  USBLC6-2P6 if RF is close to connector, then ECMF2-40A100N6.
- Tx/Rx SuperSpeed
  HSP051-4xx if RF is close to connector, then ECMF4-40A100N10.
- Common Criteria lines
  ESDA25L if 20 V compliant
  ESDA6V1 if 5 V compliant, otherwise short-to-V_{BUS} with voltage higher than 5 V that destroys the line.
  TCPP series embeds ESD and OVP protection for STM32 (FT I/O).
- SBU lines
  ESDA25L if 20 V compliant
  ESDA6V1if 5 V compliant, then short-to-V_{BUS} with voltage higher than 5 V that destroys the line.

For further information, refer to Section 1.2 and to www.st.com (search Type-C protection).

For sourcing devices, TVS must be selected according to the voltage on the VBUS (that can be higher than 5 V):

- ESDA7P120-1U1M for 5 V VBUS
- ESDA13P70-1U1M for 9 V VBUS
- ESDA15P60-1U1M for 12 V VBUS
- ESDA17P50-1U1M for 15 V VBUS
- ESDA25P35-1U1M for 20 V VBUS

For sinking devices, TVS (ESDA25P35-1U1M) and an overvoltage protection (TCPP01-M12 or TCPP03-M20) are recommended to avoid destruction in case of defective adapter sourcing at maximum voltage.

14.2 Capacitors on CC lines

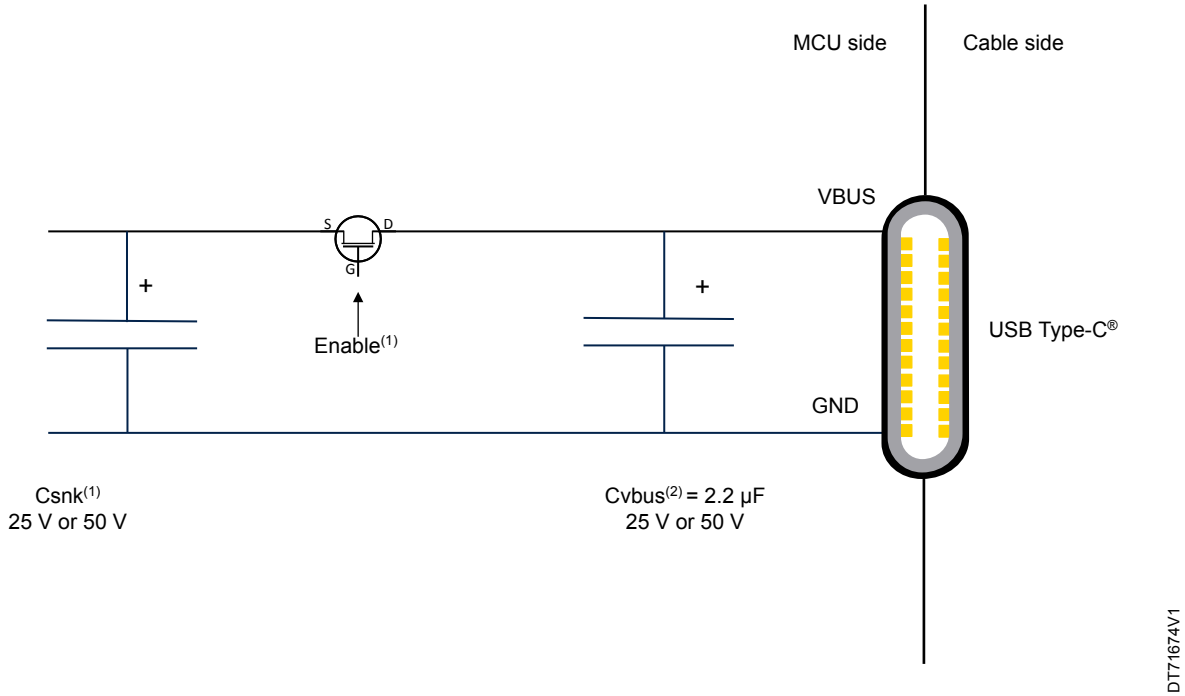
The USB PD specification allows CC receiver (cReceiver) capacitance in the range of 200 pF to 600 pF.

For noise filtering purposes, an extra 390 pF +/- 10% capacitance must be added on each CC line close to the Type-C connector. When a TCPP0x is used, these capacitors must be added between the TCPP0x and the Type-C connector, as close to the Type-C connector as possible.

14.3 Capacitors on VBUS line

14.3.1 Sink mode

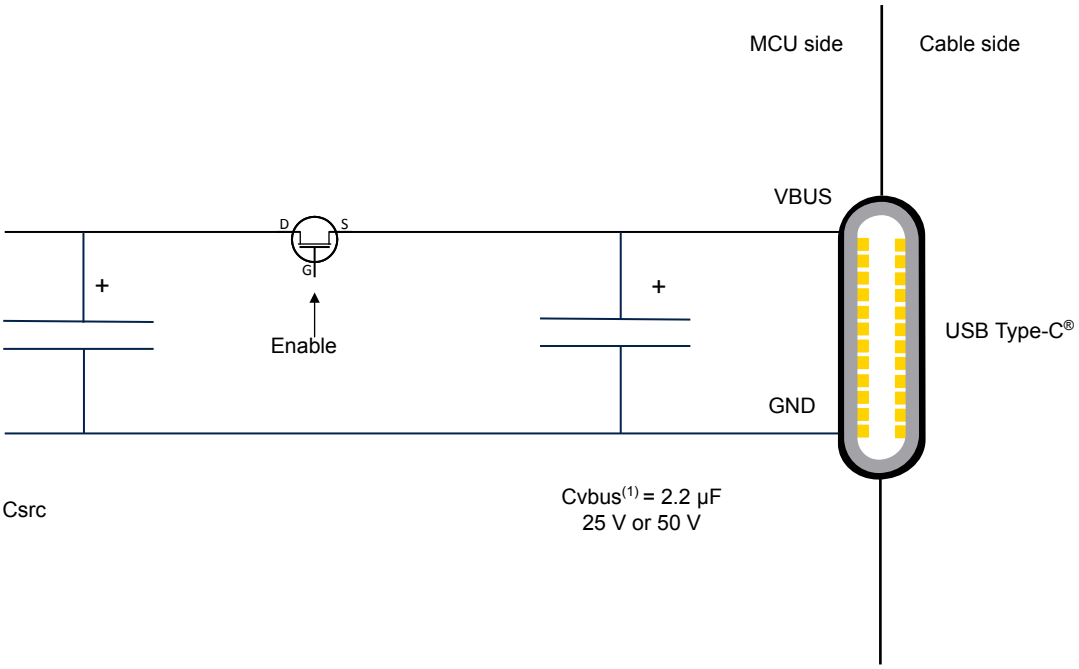
Figure 43. **Sink mode scheme**



Note:
1. *According to the Csnk capacitance value, consider the MOS rise time to comply with the USB inrush current (see Section 14.3.4 How to limit the inrush current in Sink mode).*
2. *Use Cvbus = 2.2 uF to comply with the cSnkBulk range.*

14.3.2 SRC mode

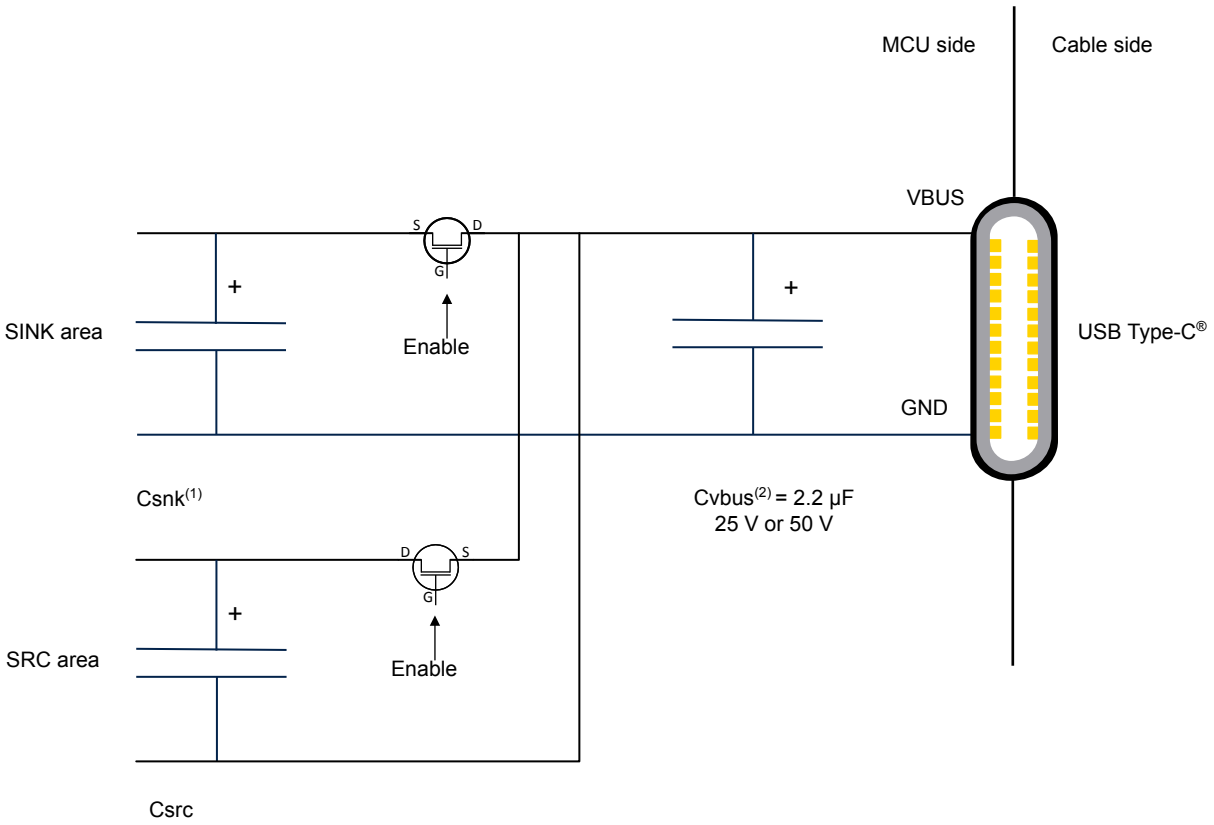
Figure 44. **SRC mode scheme**



Note: 1. Use Cvbus = 2.2 µF.

14.3.3 DRP mode

Figure 45. **DRP mode scheme**



Note:
1. *According to the Csnk capacitance value, the MOS rise time must comply with the USB inrush current (see Section 14.3.4 How to limit the inrush current in Sink mode).*
2. *Use Cvbus = 2.2µF.*

14.3.4 How to limit the inrush current in Sink mode

Regarding the function **Enable** for the Mos command, a capacitor Cdg can be added between Gate and Drain to limit the inrush current and OCP. 100pF for each 10µF is recommended (Csnk). See Figure 43. Sink mode scheme and Figure 45. DRP mode scheme, and consult the user manual [12] for more details.

14.4 TCPP01, TCPP02 and TCPP03 Type-C port protection devices

Two Type-C Power Delivery failure modes are identified:

- VBUS high voltage short circuit to the CC lines when a unplug is done with a poor mechanical quality connector. Over voltage protection is needed on the CC line. This use case appears only when Power Delivery is used.
- VBUS line compromised if a defective charger is stuck at a high voltage. Over-voltage protection is needed on the VBUS line. This use case can occur even when Power Delivery is not used.

A dedicated single TCPP01, TCPP02 or TCPP03 chip, can be used for system protection. They provide a cost-effective solution to protect low-voltage MCUs or other controllers performing USB Type-C Power Delivery management:

- *TCPP01-M12* for power sink protection
- *TCPP02-M18* for power source protection
- *TCPP03-M20* for protection of dual-role power scenarios.

The TCPP01-M12, TCPP02-M18, and TCPP03-M20 provide 20 V short-to-VBUS over-voltage and IEC ESD protection on CC lines, as well as programmable over-voltage protection with an NMOS gate driver for the VBUS line. They also integrate dead battery management, and can be completely turned off for battery-powered devices. A fault report is also generated.

The TCPP02-M18 and TCPP03-M20 also integrate a dual VBUS gate driver, and an I2C communication interface for dual-port applications.

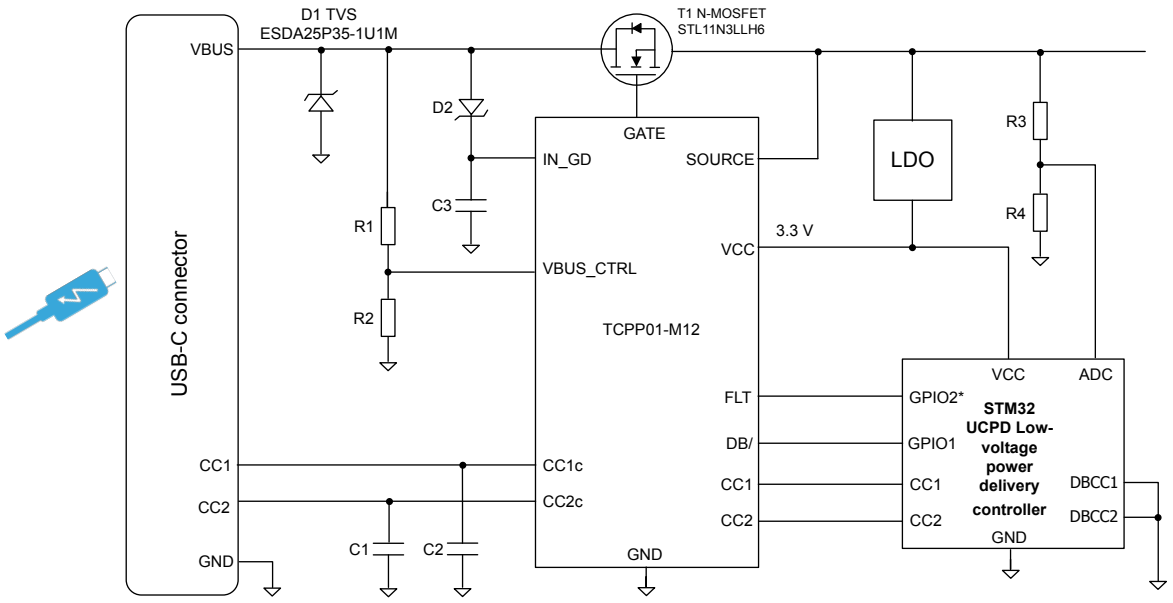
TVS is still required on VBUS (ESDA25P35-1U1M), and then only the maximum voltage is considered.

More details are given in the TCPP01, TCPP02 and TCPP03 data sheets [3], [4],and [5].

14.4.1 SNK or sink power applications

The following figure shows a sink application drawing all its power from the USB Type-C connector VBUS line.

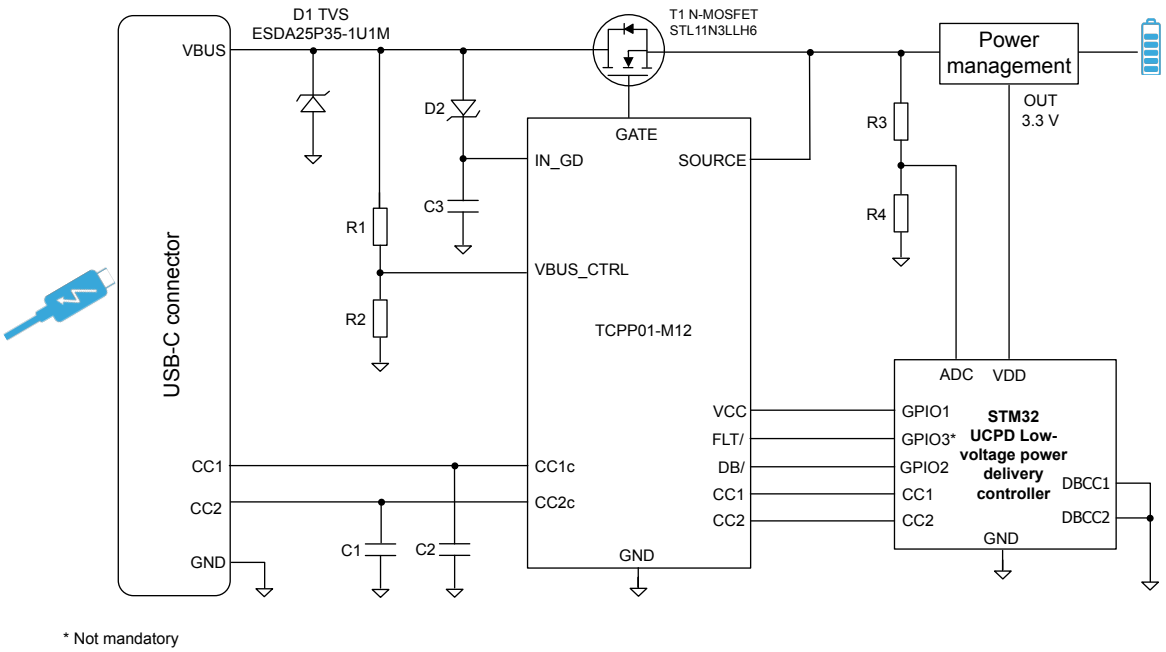
Figure 46. Entirely VBUS-powered sink



* Not mandatory

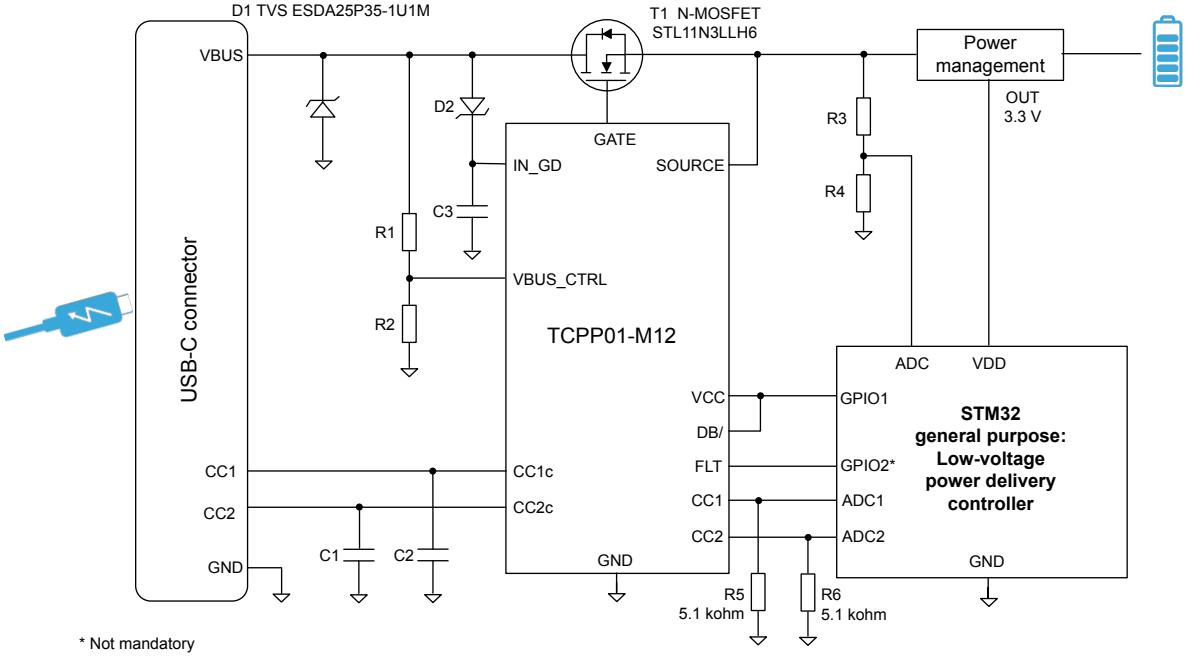
- FLT (FAULT) is an open-drain output pin.
- DB/ is a pull-down TCPP input. Connect it to 3.3 V if not managed by the MCU software.

Figure 47. Sink application with battery (PD3.0)



- FLT (FAULT) is an open-drain output pin.
- DB/ is a pull-down TCPP input. Connect it to 3.3 V if not managed by the MCU software.

Figure 48. 15 W sink application with battery



- FLT (FAULT) is an open-drain output pin, to leave open if not connected.
- When GPIO1 is low, TCPP01-M12 is OFF with zero current consumption.
- When GPIO1 is low, TCPP01-M12 is ON with ADC1 or ADC2 checking the source capability.

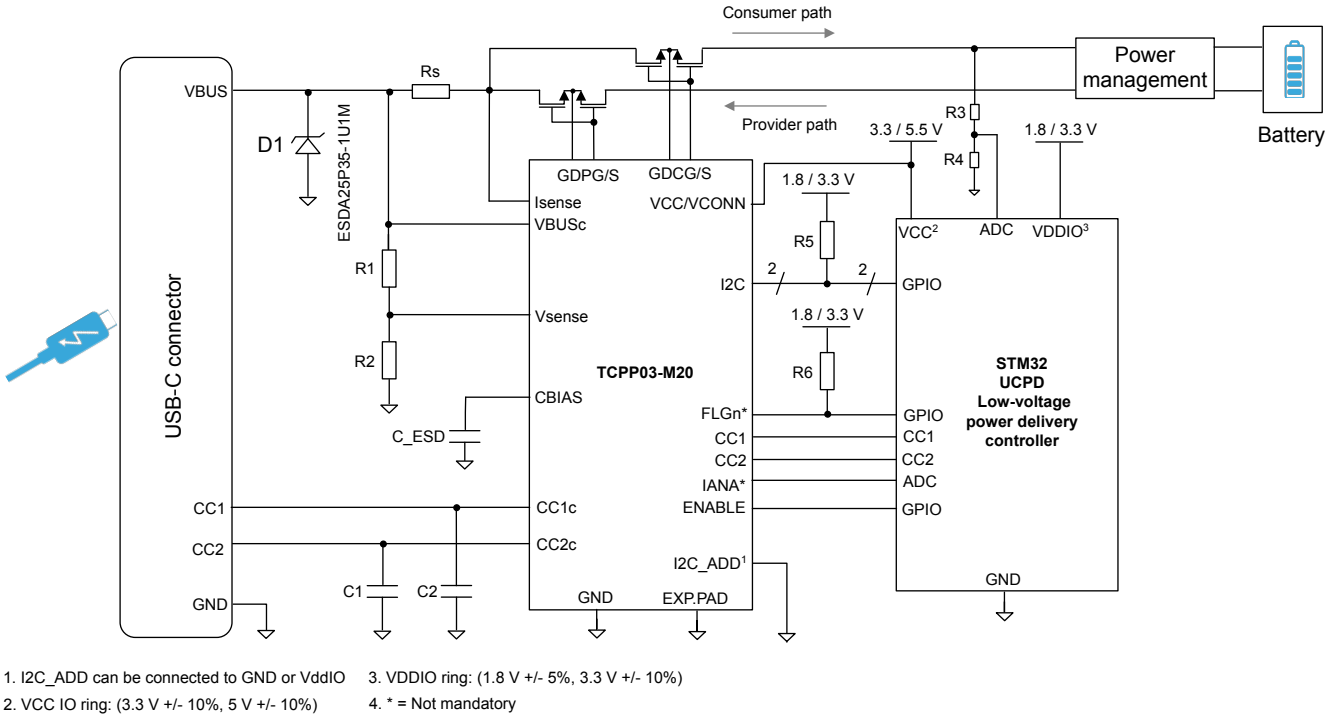
In dead battery condition, the following sequence applies:

1. TCPP01-M12 presents a DB clamp (1.1 V) on CC1 and CC2 lines.
2. The source detects the clamp presence and applies 5 V on VBUS.
3. N-MOSFET T1 is normally ON and the power management block is supplied with 5 V.
4. The MCU wakes-up, and applies 3.3 V on GPIO1 to wake up TCPP01-M12.
5. TCPP01-M12 releases the clamp on the CC1 and CC2 lines so that ADC1 or ADC2 can sense the SOURCE pin capability with the voltage across R5 or R6.

14.4.2 DRP or dual-role power applications

Figure 49 shows a DRP application using dedicated power management.

Figure 49. Battery DRP application example



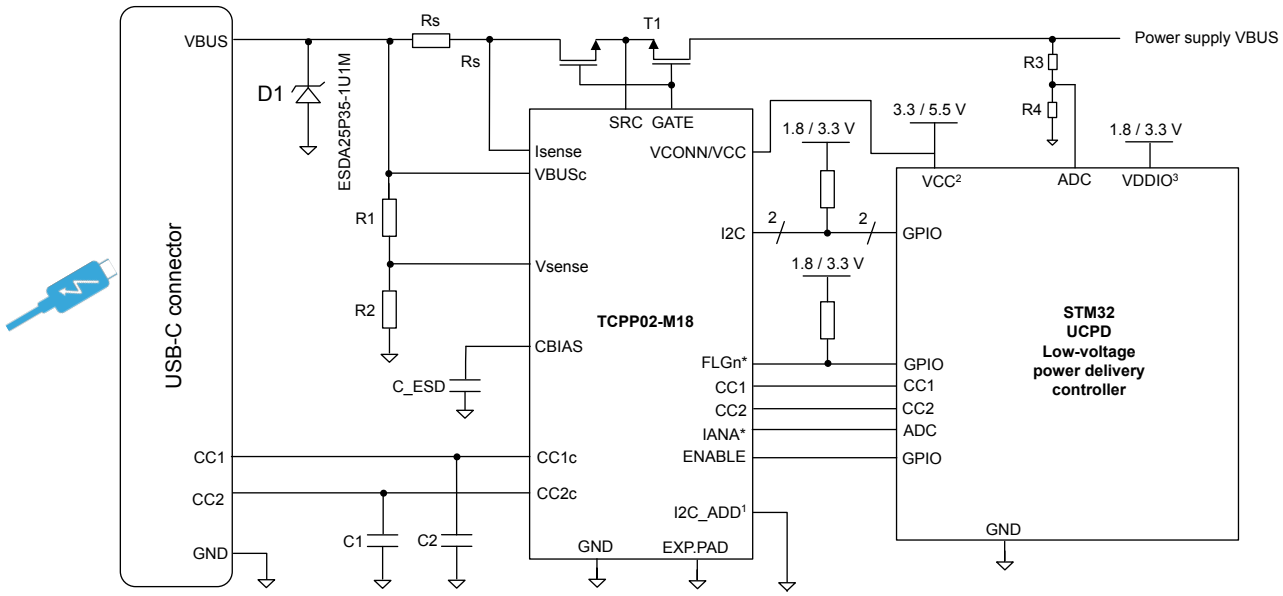
1. I2C_ADD can be connected to GND or VddIO
2. VCC IO ring: (3.3 V +/- 10%, 5 V +/- 10%)
3. VDDIO ring: (1.8 V +/- 5%, 3.3 V +/- 10%)
4. * = Not mandatory

Note: If the ENABLE pin of TCPP(02/03) is used for power on reset, then the rise time must be shorter than 50 microS. See the document [12] for more details.

14.4.3 SRC or source power applications

Figure 50 shows a SRC application using dedicated power management.

Figure 50. SRC application using dedicated power management



1. I2C_ADD (I2C address): can be connected to GND or VddIO
2. VCC IO ring: (3.3 V +/- 10%, 5 V +/- 10%)
3. VDDIO ring: (1.8 V +/- 5%, 3.3 V +/- 10%)
4. * = Not mandatory

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Note: If the ENABLE pin of TCPP(02/03) is used for power on reset, then the rise time must be shorter than 50 microS. See the document [13] for more details.

14.4.4 Handling dead battery condition

TCPP01

For the TCPP01 device, the DB/ (dead battery resistor management) pin is a pulled-down active-low TCPP01 input. The DB/ pin can either be connected to VCC or driven by an MCU GPIO.

As long as the DB/ input is low (connected to ground or left open and tied low through a built-in 5 kΩ pull-down resistor), the dead-battery resistors are connected and CC switches are opened (OFF state).

When the DB/ pin is tied to VCC, the DB resistors on the CC pins are disconnected and CC switches are closed (ON state).

DB/ usage (sink application):

- After system power-up, the DB/ pin must be kept low, which activates DB Rd of TCPP01.
- Once the DB Rd is enabled on STM32 CC pins, the DB/ pin must be set high.

TCPP03

The dead battery management is integrated in the chip. See the *Power Mode* chapter in the TCPP03 data sheet [5].

14.5 EMC considerations in USB HS cases

To decrease noise on VBUS due to D+/D- lines activities, a 100 pF capacitor can be added between VBUS and GND close to the Type-C connector.

14.6 VBUS inrush current considerations in Sink cases

To limit the inrush current on VBUS, an additional 100 pF capacitor (for every additional 10 µF decoupling capacitor on the application side) can be added between the drain and gate of the power switch MOS connected to the TCPP01 gate pin.

14.7 VBUS overshoot considerations in Sink cases

To limit overshoot on VBUS, a damping filter can be added between VBUS and GND close to the Type-C connector.

As an example: a 1 µF capacitor in parallel with a 4.7 µF capacitor in series with 1 Ω reduces the overshoot amplitude.

14.8 VBUS discharge

On SRC or Source Power application, extra discharge circuitry may be used. See Figure 25. Source architecture.

The VBUS discharge feature is integrated in the TCPP02 and TCPP03. See their respective datasheets [4], [5], for further information.

14.9 VBUS sensing detection

See chapter *VBUS sensing detection* in the *Introduction to USB hardware and PCB guidelines using STM32 MCUs* application note (AN4879).

15 Additional information

The USB Power Delivery protocol over CC lines is defined as an extension to both USB2.0 and USB3.1, and only applies to the use of the Type-C connector.

Protocol purpose

The purpose of this protocol is to negotiate the power capabilities and power requirements of the devices connected through a USB Type-C® cable, in order to safely deliver power from the power source device to the power sink device.

The protocol combined with the Type-C connection allows the increase of the maximum power delivery to 100 W (5 A at 20 V).

The Power Delivery role (source or sink) is dissociated from the upstream/downstream-facing port roles. For example, a USB device/hub (upstream-facing port) can deliver power to the USB host (downstream-facing port). During the initial connection, the UFP is the sink and the DFP is the source. Both role pairs (source/sink and UFP/DFP) can be swapped over the Type-C connection.

New Type-C cable additional pins

The new Type-C cable has two additional wires, CC1 and CC2, for configuration control.

Optionally, one of these pins can be configured as a VCONN supply to power an external accessory. In this case, the signalling function of the pin is not available.

Power Delivery port - pull-up/down resistors

A device acting as a Type-C port supporting Power Delivery protocol must pull the CC line(s) up or down:

- Power source: pull up with Rp equal to one of three specified values, depending on the power requirements of the sink
- Power sink: pull down with Rd equal to a specified value
- Dual-role power port: as power source or power sink, depending on its actual role.

System attach

Once a debounce period has elapsed, the system becomes attached:

- On CC, Power Delivery messaging can be used for communication over CC lines
  - power capabilities, for example beyond 5 V/3 A
  - power-role swaps
  - data role swaps (similar to HNP in OTG)
  - VCONN swap
- On VCONN: on seeing an Ra resistor a 5 V supply must be provided

Single Type-C port pins

- Source/sink/DRP port cases:
  - Two CC pins (CC1/CC2) allow for unknown orientation of the cable
- Cable and accessory cases:
  - Orientation is pre-determined
  - A single CC pin is needed

Dead battery support

Dead battery signalling capability of a Type-C power sink translates into exposing a pull-down resistor of a specified value or a voltage clamp to the CC lines when the power sink device is unpowered. It is interpreted as a request to receive VBUS. It thus facilitates the charging of equipment with a dead battery, and also powering one with no battery.

Type-C power source (such as a wall charger) **must not** provide dead battery signalling.

Revision history

Table 17. **Document revision history**

Date	Version	Changes
24-Apr-2019	1	Initial release.
26-Sep-2019	2	Updated: • Section Introduction • Section 1.2 Reference documents • Table 8. Fixed and programmable power supply current and cabling requirements • Figure 25. Source architecture • Figure 29. DRP with FRS VBUS = 5 V / 9 V / 15 V connections • Figure 38. Applying V_{CONN} on CC lines • Figure 46. Entirely VBUS-powered sink • Figure 47. Sink application with battery (PD3.0) • Section 14.4.1 SNK or sink power applications • Figure 48. 15 W sink application with battery Added: • Figure 8. USB Type-C Power Delivery block diagram and Figure 9. STM32G0 Discovery kit USB Type-C analyser • New Figure 27. DRP connections • New Figure 1 Removed Source and Source/Sink mode description subsections from Section 14.4 TCPP01, TCPP02 and TCPP03 Type-C port protection devices.
01-Sep-2020	3	Updated: • Section Introduction • Section 1.2 Reference documents • Section 5 Power profiles • Section 9 Product offer • Section 11 Type-C with Power Delivery using integrated UCPD peripheral, Section 11.3 Hardware overview • Section 12 Type-C with Power Delivery using a general-purpose peripheral, Section 12.2 Hardware overview • Section 13 Dedicated architecture proposals and solutions • Section 14 Recommendations
14-Sep-2021	4	Updated: • Section 1.2 Reference documents • Table 14. Source features • Section 13.5 Monitoring VBUS voltage and current and Figure 41 • Section 14.4 TCPP01, TCPP02 and TCPP03 Type-C port protection devices (and rearranged subsequent subsections). Added: • Section 13.6 Dual-role power port • Section 14.4.2 DRP or dual-role power applications • Section 14.6 VBUS inrush current considerations in Sink cases • Section 14.7 VBUS overshoot considerations in Sink cases • Section 14.8 VBUS discharge
12-Oct-2021	5	Updated: • Section Introduction
16-Mar-2022	6	Updated: • Figure 48. 15 W sink application with battery

Date	Version	Changes
		• Figure 49. Battery DRP application example • Figure 50. SRC application using dedicated power management
23-Jun-2023	7	Added: • Section 11.2 STM32 MPU software overview • Section 14.3 Capacitors on VBUS line • VBUS sensing detection Updated: • Section Introduction • Section 1.2 Reference documents • Section 11.1 STM32 MCU software overview

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